Errata Sheet and Guidelines for Arria V ES Devices

This errata sheet provides information about known device issues affecting Arria® V engineering sample (ES) devices, and guidelines for device usage.

ES devices are not intended to be used for volume production.

The programming file is not compatible between ES and production devices.

Device Errata for Arria V ES Devices

Table 1 lists the specific device issues and the affected Arria V ES devices.

Table 1. Device Issues (Part 1 of 2)

Issue	Affected Devices	Planned Fix
"Usermode High Icc" High Icc observed when entering Usermode.	All Arria V ES Devices	None
"Unused or Idle Transmitter Maximum Data Rate Degradation" Currently unused or idle transmitter's maximum data rate can degrade over a period.	All Arria V ES Devices	None
"Fractional PLL Clock Switchover" In certain instances, the fractional PLL starts with the backup clock.	All Arria V ES devices	Production Devices
"False Configuration Failure in Active Serial Multi-Device Configurations" In Active Serial (AS) multi-device configuration mode, the error checking for CONF_DONE release may not operate correctly.	All Arria V devices	None
"Requirements to Operate the CMU PLL Above 4 Gbps" Specific requirements must be met to operate the CMU PLL above 4 Gbps.	5AGXB3 ES	Production Devices
"Internal Temperature Sensing Diode Feature" Arria V ES devices will not support the Internal Temperature Sensing Diode feature.	All Arria V ES devices	Production Devices
"Variable Precision DSP Clock signals" There are only two clock signals available for variable precision DSP blocks.	5AGXB3 ES	Production Devices
"Low VOCM at Minimum VCCIO" The V_{OCM} falls out of the datasheet specification at minimum V_{CCIO}	5AGXB3 ES	Production Devices

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Table 1. Device Issues (Part 2 of 2)

Issue	Affected Devices	Planned Fix
"Error Detection CRC (EDCRC)" The full Error Detection CRC (EDCRC) feature will not be supported in ES devices	5AGXB3 ES	Production Devices
"Normal Compensation and Source Synchronous Compensation Mode Support in Fractional PLLs" Some fractional phase-locked loops (PLLs) do not support normal compensation and source synchronous compensation mode.	5AGXB3 ES	Production Devices

Usermode High Icc

When the affected device transitions to Usermode, high Icc is observed because of internal dataline contention.

Workaround

Use the following software workaround to prevent the Usermode high Icc issue:

- For the Error Detection Cyclic Redundancy Check (EDCRC) user, no workaround is needed, the EDCRC feature eliminates the high Icc issue.
- For the non-EDCRC user, a software workaround is needed and is available in the Quartus® II software version 12.1 release, or later.

Action Needed for Existing Designs (pre-Quartus II software version 12.1)

Different actions are needed when the existing design uses a different combination of EDCRC, Partial Reconfiguration (PR) and Configuration via Protocol (CvP) settings. Table 2 lists the actions needed for the different settings.

Table 2. Action for Existing Designs

Design	Action
EDCRC enabled.	None needed.
EDCRC disabled, AND PR & CvP features are not used.	Full recompilation is needed, using the Quartus II software version 12.1 or later release.
EDCRC disabled, but PR, CvP, or both are used.	Quartus II software version 12.1 or later releases require that you enable EDCRC, and recompile the design.

Unused or Idle Transmitter Maximum Data Rate Degradation

A currently unused or idle transmitter's maximum data rate can degrade over a period. The issue is caused by degradation in the local or central clock divider (used to drive the transmitter) being left idle over an extended period, with the transceiver's power supplies powered up.

The issue only impacts designs that will enable unused or idle transmit channels with idling clock dividers through a new programming file at a later date. The transmit channel in devices that do not power up the transceiver power supplies are not affected.

The idling clock divider can occur in three conditions:

1. Transmit channels in permanent reset
   a. Transmit channels that will be enabled later are instantiated in the current design, but with the PMA block or divider source clock (CMU PLL or fPLL) held in reset permanently.
2. Unused non-bonded transmit channels
   a. Non-bonded transmit channels that will be enabled later are not instantiated in the current design, resulting in an idling local clock divider.
3. Unused CMU PLL or fPLL for bonding
   a. CMU PLL or fPLL used for bonding that will be enabled later are not instantiated in the current design, resulting in an idling central clock divider.

To avoid this issue, ensure the clock dividers that will be enabled later are in the active state in the current programming file. Follow the implementation instructions in Table 3 to avoid this issue.

Table 3. Workaround Implementation Instructions

Scenario	Design Requirement	Future Design Change	Action
1	Fixed transceiver utilization design over device lifecycle (no change to design file)	Not applicable	Do nothing, not affected by issue.
2	Transceiver utilization design will change over device lifecycle	Enable transmit channel held in permanent reset	Leave transmitter `tx_analogreset` or `pll_powerdown` signals de-asserted. Keep `tx_digitalreset` signal asserted and transmits static `0x0` data.
3		Enable unused non-bonded transmit channel	Instantiate dummy **Transmit Only** channel in non-bonded mode on every transmit channel that will be enabled later. Share existing active clock resources (CMU PLL or fPLL and input reference clock) if available. Leave transmitter `tx_analogreset` or `pll_powerdown` signals de-asserted.
4		Enable unused CMU PLL or fPLL for bonding	Instantiate dummy **Transmit Only** channel in bonded mode with source PLL assigned to the CMU PLL or fPLL that will be enabled later for bonded configurations. Leave transmitter `tx_analogreset` or `pll_powerdown` signals de-asserted.

The dummy **Transmit Only** channel will increase transceiver power consumption in your design. Use the Early Power Estimator (EPE) tool or PowerPlay Power Analyzer (PPPA) in the Quartus II software to account for the power increase from the additional dummy channels.

Use the following general guidelines for reducing power consumed by the dummy **Transmit Only** channel:

- In Arria V GT devices, instantiate the dummy channel in PMA direct mode with Native PHY IP.
- In Arria V GX devices, keep the `tx_digitalreset` signal asserted in dummy channel to minimize PCS activity.
- Transmit the static `0x0` data over dummy channel.
- Configure the dummy channel with the lowest possible data rate.
- Set the VOD = 6 (minimum value) on the transmitter output pin for dummy channel.

Fractional PLL Clock Switchover

If you have enabled the Manual Fractional PLL Clock Switchover feature, and if both the reference and backup clocks are toggling prior to completion of the configuration, the fractional PLL starts with the backup clock.

Workaround

To avoid having the fractional PLL start with the backup clock, gate the reference and backup clocks until the part enters user mode (optionally indicated through `INIT_DONE`), or engage the clock switchover circuitry to switch to the reference clock (for example, toggling the fractional PLL's extclk switch input).

False Configuration Failure in Active Serial Multi-Device Configurations

In Active Serial (AS) multi-device configuration mode, the error checking for `CONF_DONE` release may not operate correctly. As a result, you may experience false configuration errors. The failure is indicated by the `CONF_DONE` going high followed by the `nSTATUS` going low and reconfiguration is initiated.

Workaround

To overcome this issue, perform both of the following:

1. Disable the `CONF_DONE` error checking in AS multi-device configuration mode:
   a. If you are using Quartus® II software version 12.0 or older, check the “Disable AS mode CONF_DONE error check” option. This option can be found in the “Advanced” button, under the Convert Programming File window.
   b. If you are using Quartus II version 12.0 SP1 or later, the error checking is disabled automatically for AS multi-device configuration POF file generation.
2. Enable the INIT_DONE pin option:
   a. To ensure a successful configuration, Altera recommends that you enable the `INIT_DONE` optional pin for devices in the configuration chain. On the board, route out the `INIT_DONE` pin separately for both the master and slave devices. Monitor the `INIT_DONE` status for each of the devices to ensure a successful transition into user-mode.

Other configuration modes (JTAG, Fast Passive Parallel (FPP), and Passive Serial (PS) (single and multi device configurations, and AS single device configurations) are not affected.

Requirements to Operate the CMU PLL Above 4 Gbps

To ensure proper CMU PLL operation when configured above 4 Gbps, you must adhere to all of the following requirements:

- Use the Quartus II software version 12.0 or later
- Connect the Transceiver Reconfiguration IP to the transceiver PHY IP
- Stabilize the input reference clock to the CMU PLL before releasing the transceiver PHY resets
- Manual control of the `pll_powerdown` and `rx_analogreset` ports are disabled by the Quartus II software. During power-up, the resets are completed automatically.

If your design requires dynamically reconfiguring the CMU PLL to a data rate above 4 Gbps, refer to the Arria V Support Solution for details.

Internal Temperature Sensing Diode Feature

Arria V ES devices will not support the Internal Temperature Sensing Diode feature. The Internal Temperature Sensing Diode feature is supported in Arria V production devices.

Variable Precision DSP Clock signals

There are only two clock signals available for variable precision DSP blocks in Arria V ES devices: `CLK0` and `CLK1`. Clock signal `CLK2` is not available. In the Quartus II software patch version 11.1 SP2, the use of `CLK2` for Variable Precision DSP blocks in Arria V ES devices is disabled.

If your design requires three clock signals per variable precision DSP block, contact Altera's mySupport for additional support.

Low V_{OCM} at Minimum V_{CCIO}

When V_{CCIO} goes below 2.5 V, the V_{OCM} of the LVDS transmitter buffer will fall below 1.125 V, which is out of datasheet specification. To avoid the impact to the LVDS interface, Altera recommends that you maintain the V_{CCIO} above 2.5 V.

Error Detection CRC (EDCRC)

The EDCRC feature is not supported, and is disabled automatically in the Quartus II software version 11.1 SP2 and later.

Normal Compensation and Source Synchronous Compensation Mode Support in Fractional PLLs

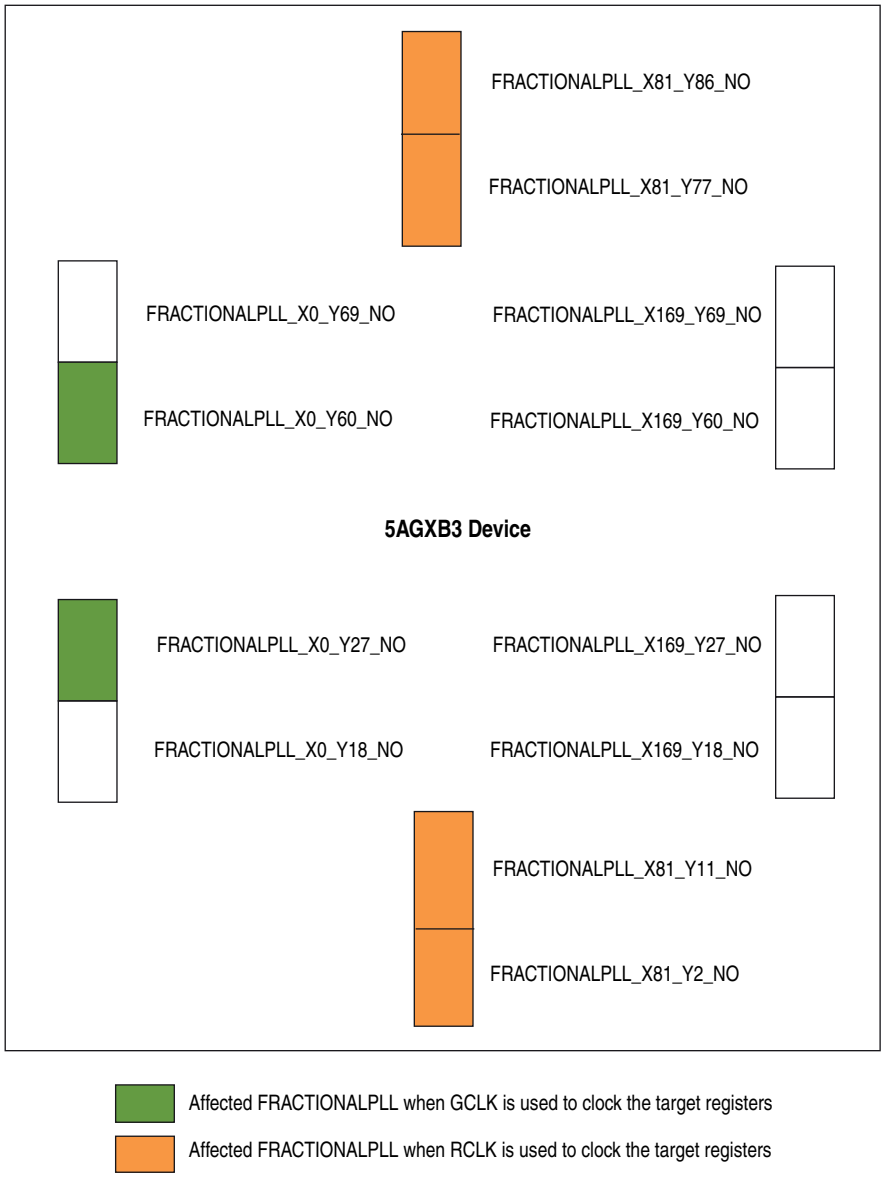
Some fractional PLLs in 5AGXB3 ES devices do not support normal compensation and source synchronous compensation mode. The LVDS compensation mode is not affected by this issue. Table 4 lists the affected fractional PLLs and configurations.

Table 4. Fractional PLL and the Affected Configurations

PLL Location	Affected Configuration for Normal and Source Synchronous Compensation
FRACTIONALPLL_X0_Y27_N0, FRACTIONALPLL_X0_Y60_N0	GCLK is used to clock the target registers
FRACTIONALPLL_X81_Y2_N0, FRACTIONALPLL_X81_Y11_N0, FRACTIONALPLL_X81_Y77_N0, FRACTIONALPLL_X81_Y86_N0	RCLK is used to clock the target registers

Figure 1 shows the fractional PLL locations for 5AGXB3 devices.

Figure 1. Fractional PLL Locations for 5AGXB3 Devices



Device Guidelines for Arria V ES Devices

The following section provides guidelines to follow when using Arria V ES devices.

VCC Power Separation

To improve noise immunity for the LVDS channels, you must separate the VCC core (VCC) and the VCC periphery (VCCP), as listed in Table 5, to two different rails and power layers on your PCB design. Place the VCCP at the closest layer to the FPGA and the VCC at the furthest layer from the FPGA.

The VCC and VCCP can share the same power supply with the ferrite filter added on the VCCP layer. Refer to the early power estimator (EPE) tool to estimate the current consumption of the VCC and VCCP.

The pins for the VCC and VCCP are listed in Table 5.

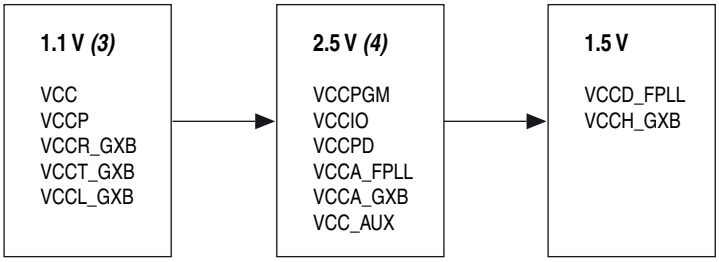
Table 5. VCC Pins for VCCP and VCC

Device	Package	VCCP	VCC
5AGXB3	F896 (31 mm) Flip Chip	L11, L15, L19, L20, L9, W11, W13, W17, W19, W21	M10, M14, M20, N11, N13, N15, N17, N19, N21, P10, P12, P14, P16, P18, P20, R11, R13, R15, R17, R19, R21, T10, T12, T14, T16, T18, T20, U11, U13, U15, U17, U19, U21, V10, V12, V14, V16, V18, V20
	F1152 (35 mm) Flip Chip	P18, R13, R21, T10, U25, V10, W25, Y12, Y19, Y22	R14, R15, R19, R23, R25, T12, T14, T16, T18, T20, T22, T24, U11, U12, U13, U15, U17, U19, U20, U21, U22, U23, V12, V14, V16, V18, V20, V22, V24, W13, W15, W17, W19, W21, W23, Y13, Y20
	F1517 (40mm) Flip Chip	AA21, AA25, AB15, U16, V13, V22, V25, V27, Y13, Y27	AA10, AA12, AA14, AA16, AA18, AA20, AA22, AA24, AA26, AB11, AB17, U10, U12, V11, V15, V17, V23, V29, W10, W12, W14, W16, W18, W20, W22, W24, W26, W28, Y11, Y15, Y17, Y19, Y21, Y23, Y25, Y29

Power-up Sequencing for Arria V ES Devices

To ensure the minimum current draw during configuration for Arria V ES devices, follow the power-up sequence recommendation as shown in Figure 2.

Figure 2. Power-up Sequencing *(1), (2)*



Notes to Figure 2:

(1) V_{CCBAT} can be powered up at any time.
(2) The power rails in each group must be ramped up to a minimum of 80% of their full rail before the next group starts.
(3) Power up V_{CCP}, V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCL_GXB} together with V_{CC}.
(4) Power up V_{CCPGM} first. V_{CCIO} and V_{CCPD} can be powered up together with V_{CCPGM} (if these supplies share a common plane or traces on the board), or in any sequence after V_{CCPGM}.

Document Revision History

Table 6 lists the revision history for this errata sheet.

Table 6. Document Revision History

Date	Version	Changes
December 2012	1.6	■ Added the "Usermode High Icc" section. ■ Added the "Unused or Idle Transmitter Maximum Data Rate Degradation"
September 2012	1.5	■ Updated "False Configuration Failure in Active Serial Multi-Device Configurations" section, Table 1.
September 2012	1.4	■ Added the "Fractional PLL Clock Switchover" section. ■ Added the "False Configuration Failure in Active Serial Multi-Device Configurations" section.
August 2012	1.3	■ Added the "Requirements to Operate the CMU PLL Above 4 Gbps" section.
June 2012	1.2	■ Added the "Internal Temperature Sensing Diode Feature" section.
February 2012	1.1	■ Added "Variable Precision DSP Clock signals" section. ■ Updated "VCC Power Separation" section. ■ Added "Power-up Sequencing for Arria V ES Devices" section. ■ Updated the "Normal Compensation and Source Synchronous Compensation Mode Support in Fractional PLLs" section, Figure 1, and Table 2.
December 2011	1.0	Initial release.