9. External Memory Interfaces

CII51009-3.1

Introduction

Improving data bandwidth is an important design consideration when trying to enhance system performance without complicating board design. Traditionally, doubling the data bandwidth of a system required either doubling the system frequency or doubling the number of data I/O pins. Both methods are undesirable because they complicate the overall system design and increase the number of I/O pins. Using double data rate (DDR) I/O pins to transmit and receive data doubles the data bandwidth while keeping I/O counts low. The DDR architecture uses both edges of a clock to transmit data, which facilitates data transmission at twice the rate of a single data rate (SDR) architecture using the same clock speed while maintaining the same number of I/O pins. DDR transmission should be used where fast data transmission is required for a broad range of applications such as networking, communications, storage, and image processing.

Cyclone® II devices support a broad range of external memory interfaces, such as SDR SDRAM, DDR SDRAM, DDR2 SDRAM, and QDRII SRAM. Dedicated clock delay control circuitry allows Cyclone II devices to interface with an external memory device at clock speeds up to 167 MHz/333 Mbps for DDR and DDR2 SDRAM devices and 167 MHz/667 Mbps for QDRII SRAM devices. Although Cyclone II devices also support SDR SDRAM, this chapter focuses on the implementations of a double data rate I/O interface using the hardware features available in Cyclone II devices and explains briefly how each memory standard uses the Cyclone II features.

The easiest way to interface to external memory devices is by using one of the Altera® external memory IP cores listed below.

- DDR2 SDRAM Controller MegaCore® Function
- DDR SDRAM Controller MegaCore Function
- QDRII SRAM Controller MegaCore Function

OpenCore® Plus evaluations of these cores are available for free to Quartus® II Web Edition software users. In addition, Altera software subscription customers now receive full licenses to these MegaCore functions as part of the IP-BASE suite.

External Memory Interface Standards

The following sections describe how to use Cyclone II device external memory interfacing features.

DDR & DDR2 SDRAM

DDR SDRAM is a memory architecture that transmits and receives data at twice the clock speed. These devices transfer data on both the rising and falling edge of the clock signal. DDR2 SDRAM is the second generation memory based on the DDR SDRAM architecture and is capable of data transfer rates of up to 533 Mbps. Cyclone II devices support DDR and DDR2 SDRAM at up to 333 Mbps.

Interface Pins

DDR and DDR2 SDRAM devices use interface pins such as data (DQ), data strobe (DQS), clock, command, and address pins to communicate with the memory controller. Data is sent and captured at twice the system clock rate by transferring data on the positive and negative edge of the clock. The commands and addresses use only one active (positive) edge of a clock.

DDR SDRAM uses single-ended data strobe DQS, while DDR2 SDRAM has the option to use differential data strobes DQS and DQS#. Cyclone II devices do not use the optional differential data strobes for DDR2 SDRAM interfaces. You can leave the DDR2 SDRAM memory DQS# pin unconnected, because only the shifted DQS signal from the clock delay control circuitry captures data. DDR and DDR2 SDRAM ×16 devices use two DQS pins, and each DQS pin is associated with eight DQ pins. However, this is not the same as the ×16/×18 mode in Cyclone II devices. You need to configure the Cyclone II devices to use two sets of pins in ×8 mode. Similarly, if your ×72 memory module uses nine DQS pins where each DQS pin is associated with eight DQ pins, configure the Cyclone II device to use nine sets of DQS/DQ groups in ×8 mode.

Connect the memory device's DQ and DQS pins to the Cyclone II DQ and DQS pins, respectively, as listed in the Cyclone II pin tables. DDR and DDR2 SDRAM also use active-high data mask (DM) pins for writes. DM pins are pre-assigned in pin outs for Cyclone II devices, and these are the preferred pins. However, you may connect the memory device's DM pins to any of the Cyclone II I/O pins in the same bank as the DQ pins of the FPGA. There is one DM pin per DQS/DQ group. If the DDR or DDR2 SDRAM device supports ECC, the design uses an extra DQS/DQ group for the ECC pins.

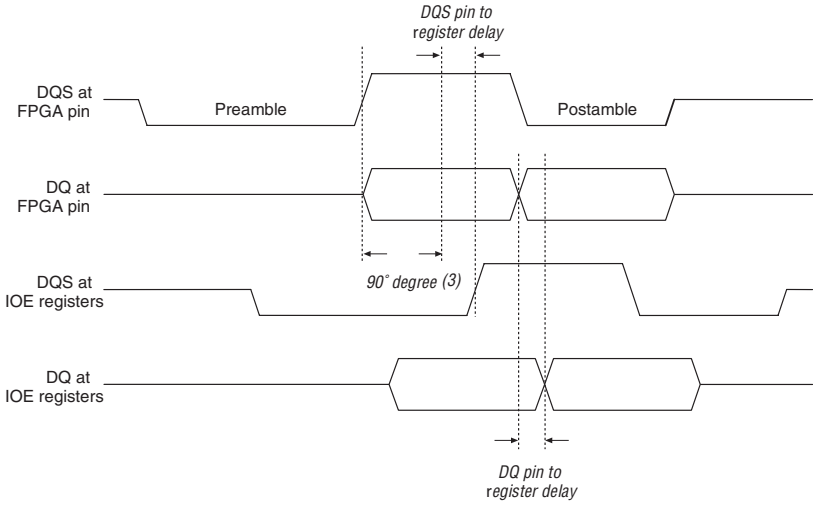
You can use any of the user I/O pins for commands and addresses. Because of the symmetrical setup and hold time for the command and address pins at the memory device, you may need to generate these signals from the negative edge of the system clock.

The clocks to the SDRAM device are called CK and CK#. Use any of the user I/O pins via the DDR registers to generate the CK and CK# signals to meet the t_{DQSS} requirements of the DDR SDRAM or DDR2 SDRAM device. The memory device's t_{DQSS} requires the positive edge of the write DQS signal to be within 25% of the positive edge of the DDR SDRAM and DDR2 SDRAM clock input. Because of strict skew requirements between CK and CK# signals, use adjacent pins to generate the clock pair. Surround the pair with buffer pins tied to V_{CC} and pins tied to ground for better noise immunity from other signals.

Read & Write Operation

When reading from the memory, DDR and DDR2 SDRAM devices send the data edge-aligned relative to the data strobe. To properly read the data, the data strobe must be center-aligned relative to the data inside the FPGA. Cyclone II devices feature clock delay control circuitry to shift the data strobe to the middle of the data window. Figure 9–1 shows an example of how the memory sends out the data and data strobe for a burst-of-two operation.

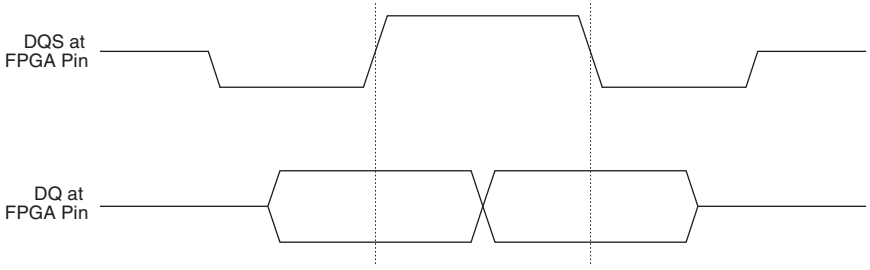
Figure 9–1. Example of a 90° Shift on the DQS Signal *Notes (1), (2)*



Notes to Figure 9–1:
(1) RLDRAM II and QDRII SRAM memory interfaces do not have preamble and postamble specifications.
(2) DDR2 SDRAM does not support a burst length of two.
(3) The phase shift required for your system should be based on your timing analysis and may not be 90°.

During write operations to a DDR or DDR2 SDRAM device, the FPGA must send the data strobe to the memory device center-aligned relative to the data. Cyclone II devices use a PLL to center-align the data strobe by generating a 0° phase-shifted system clock for the write data strobes and a –90° phase-shifted write clock for the write data pins for the DDR and DDR2 SDRAM. Figure 9–2 shows an example of the relationship between the data and data strobe during a burst-of-two write.

Figure 9–2. DQ & DQS Relationship During a DDR & DDR2 SDRAM Write



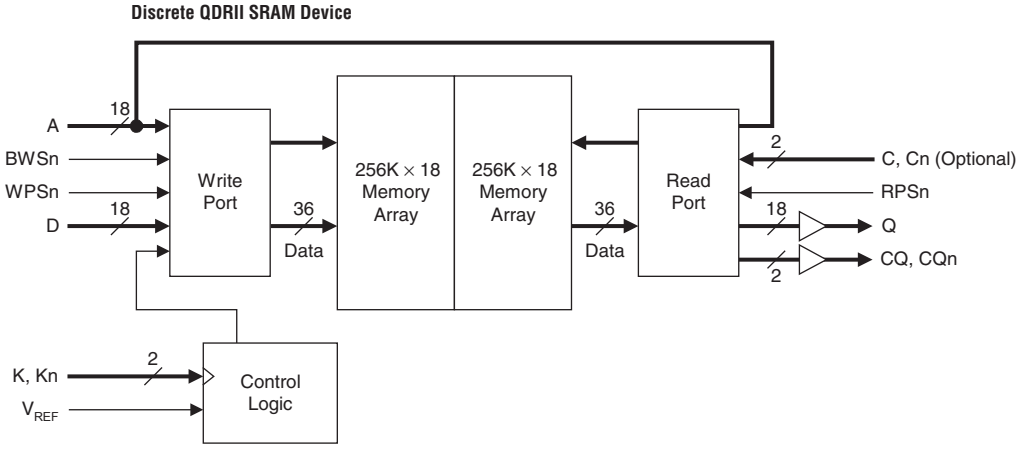
QDRII SRAM

QDRII SRAM is the second generation of QDR SRAM devices. QDRII SRAM devices, which can transfer four words per clock cycle, fulfill the requirements facing next-generation communications system designers. QDRII SRAM devices provide concurrent reads and writes, zero latency, increased data throughput, and allow simultaneous access to the same address location.

Interface Pins

QDRII SRAM devices use two separate, unidirectional data ports for read and write operations, enabling four times the data transfer compared to single data rate devices. QDRII SRAM devices use common control and address lines for read and write operations. Figure 9–3 shows the block diagram for QDRII SRAM burst-of-two architecture.

Figure 9–3. QDRII SRAM Block Diagram for Burst-of-Two Architecture



QDRII SRAM burst-of-two devices sample the read address on the rising edge of the clock and the write address on the falling edge of the clock. QDRII SRAM burst-of-four devices sample both read and write addresses on the clock's rising edge. Connect the memory device's Q ports (read data) to the Cyclone II DQ pins. You can use any of the Cyclone II device's user I/O pins in the top and bottom I/O banks for the D ports (write data), commands, and addresses. For maximum performance, Altera recommends connecting the D ports (write data) to the Cyclone II DQ pins, because the DQ pins are pre-assigned to ensure minimal skew.

QDRII SRAM devices use the following clock signals:

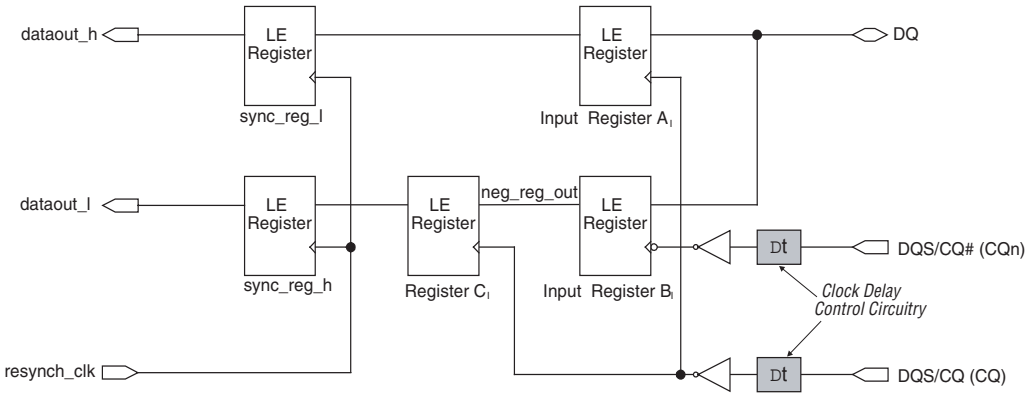
- Input clocks K and K#
- Optional output clocks C and C#
- Echo clocks CQ and CQn

Clocks C#, K#, and CQn are logical complements of clocks C, K, and CQ, respectively. Clocks C, C#, K, and K# are inputs to the QDRII SRAM, and clocks CQ and CQn are outputs from the QDRII SRAM. Cyclone II devices use single-clock mode for QDRII SRAM interfacing. The K and K# clocks are used for both read and write operations, and the C and C# clocks are unused.

You can generate C, C#, K, and K# clocks using any of the I/O registers via the DDR registers. Due to strict skew requirements between K and K# signals, use adjacent pins to generate the clock pair. Surround the pair with buffer pins tied to V_{CC} and pins tied to ground for better noise immunity from other signals.

In Cyclone II devices, another DQS pin implements the CQn pin in the QDRII SRAM memory interface. These pins are denoted by DQS/CQ# in the pin table. Connect CQ and CQn pins to the Cyclone II DQS/CQ and DQS/CQ# pins of the same DQ groups, respectively. You must configure the DQS/CQ and DQS/CQ# as bidirectional pins. However, because CQ and CQn pins are output-only pins from the memory device, the Cyclone II device's QDRII SRAM memory interface requires that you ground the DQS/CQ and DQS/CQ# output enable. To capture data presented by the memory device, connect the shifted CQ signal to register C_I and input register A_I. Connect the shifted CQn to input register B_I. Figure 9–4 shows the CQ and CQn connections for a QDRII SRAM read.

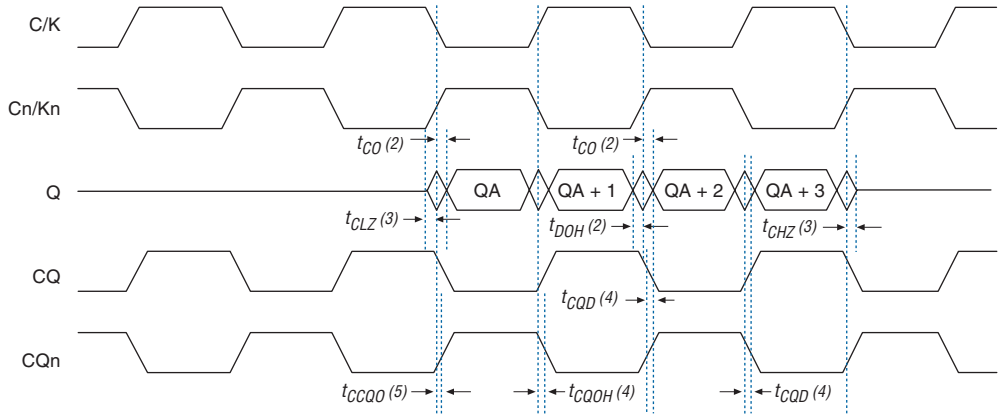
Figure 9–4. CQ & CQn Connection for QDRII SRAM Read



Read & Write Operation

Figure 9–5 shows the data and clock relationships in QDRII SRAM devices at the memory pins during reads. QDRII SRAM devices send data within t_{CO} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. Data is valid until t_{DOH} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. The CQ and CQn clocks are edge-aligned with the read data signal. These clocks accompany the read data for data capture in Cyclone II devices.

Figure 9–5. Data & Clock Relationship During a QDRII SRAM Report



Notes to Figure 9–5:

(1) The timing parameter nomenclature is based on the Cypress QDRII SRAM data sheet for CY7C1313V18.
(2) t_{CO} is the data clock-to-out time and t_{DOH} is the data output hold time between burst.
(3) t_{CLZ} and t_{CHZ} are bus turn-on and turn-off times, respectively.
(4) t_{CQD} is the skew between CQn and data edges.
(5) t_{CCQO} and t_{CQOH} are skew measurements between the C or C# clocks (or the K or K# clocks in single-clock mode) and the CQ or CQn clocks.

When writing to QDRII SRAM devices, the write clock generates the data while the K clock is 90° shifted from the write clock, creating a center-aligned arrangement.

Cyclone II DDR Memory Support Overview

Table 9–1 shows the external memory interfaces supported in Cyclone II devices.

Table 9–1. External Memory Support in Cyclone II Devices *Note (1)*

Memory Standard	I/O Standard	Maximum Bus Width	Maximum Clock Rate Supported (MHz)	Maximum Data Rate Supported (Mbps)
DDR SDRAM	SSTL-2 class I *(2)*	72	167	333 *(1)*
	SSTL-2 class II *(2)*	72	133	267 *(1)*
DDR2 SDRAM	SSTL-18 class I *(2)*	72	167	333 *(1)*
	SSTL-18 class II *(3)*	72	125	250 *(1)*
QDRII SRAM *(4)*	1.8-V HSTL class I *(2)*	36	167	667 *(1)*
	1.8-V HSTL class II *(3)*	36	100	400 *(1)*

Notes to Table 9–1:

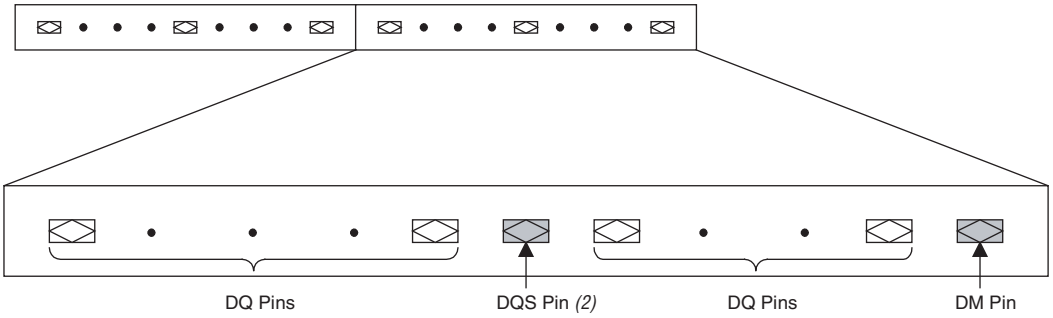
(1) The data rate is for designs using the clock delay control circuitry.
(2) These I/O standards are supported on all the I/O banks of the Cyclone II device.
(3) These I/O standards are supported only on the I/O banks on the top and bottom of the Cyclone II device.
(4) For maximum performance, Altera recommends using the 1.8-V HSTL I/O standard because of higher I/O drive strength. QDRII SRAM devices also support the 1.5-V HSTL I/O standard.

Cyclone II devices support the data strobe or read clock signal (DQS) used in DDR SDRAM with the clock delay control circuitry that can shift the incoming DQS signals to center them within the data window. To achieve DDR operation, the DDR input and output registers are implemented using the internal logic element (LE) registers. You should use the `altdqs` and `altdq` megafunctions in the Quartus II software to implement the DDR registers used for DQS and DQ signals, respectively.

DDR Memory Interface Pins

Cyclone II devices use data (DQ), data strobe (DQS), and clock pins to interface with external memory. Figure 9–6 shows the DQ and DQS pins in the ×8/×9 mode.

Figure 9–6. Cyclone II Device DQ & DQS Groups in ×8/×9 Mode *Notes (1), (3)*



Notes to Figure 9–6:

(1) Each DQ group consists of a DQS pin, a DM pin, and up to nine DQ pins.

(2) For the QDRII memory interface, other DQS pins implement the CQn pins. These pins are denoted by DQS/CQ# in the pin table.

(3) This is an idealized pin layout. For the actual pin layout, refer to the pin tables in the *PCB Layout Guidelines* section of the *Cyclone II Device Handbook, Volume 1*.

Data & Data Strobe Pins

Cyclone II data pins for the DDR memory interfaces are called DQ pins. Cyclone II devices can use either bidirectional data strobes or unidirectional read clocks. Depending on the external memory interface, either the memory device's read data strobes or read clocks feed the DQS pins.

In Cyclone II devices, all the I/O banks support DDR and DDR2 SDRAM and QDRII SRAM memory at up to 167 MHz. All the I/O banks support DQS signals with the DQ bus modes of ×8/×9 and ×16/×18. Cyclone II devices can support either bidirectional data strobes or unidirectional read clocks.

DDR2 and QDRII interfaces with class II I/O standard can only be implemented on the top and bottom I/O banks of the Cyclone II device.

In ×8 and ×16 modes, one DQS pin drives up to 8 or 16 DQ pins, respectively, within the group. In the ×9 and ×18 modes, a pair of DQS pins (CQ and CQ#) drives up to 9 or 18 DQ pins within the group to support one or two parity bits and the corresponding data bits. If the parity bits or any data bits are not used, the extra DQ pins can be used as regular user I/O pins. The ×9 and ×18 modes are used to support the QDRII memory interface. Table 9–2 shows the number of DQS/DQ groups supported in each Cyclone II density/package combination.

Table 9–2. Cyclone II DQS & DQ Bus Mode Support *Note (1)*

Device	Package	Number of ×8 Groups	Number of ×9 Groups *(5)*, *(6)*	Number of ×16 Groups	Number of ×18 Groups *(5)*, *(6)*
EP2C5	144-pin TQFP *(2)*	3	3	0	0
	208-pin PQFP	7 *(3)*	4	3	3
	256-pin FineLine BGA	8 *(3)*	4 *(7)*	4	4 *(7)*
EP2C8	144-pin TQFP *(2)*	3	3	0	0
	208-pin PQFP	7 *(3)*	4 *(7)*	3	3
	256-pin FineLine BGA®	8 *(3)*	4 *(7)*	4	4 *(7)*
EP2C15	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 *(4)*	8 *(8)*	8	8 *(8)*
EP2C20	240-pin PQFP	8	4	4	4
	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 *(4)*	8 *(8)*	8	8 *(8)*
EP2C35	484-pin FineLine BGA	16 *(4)*	8 *(8)*	8	8 *(8)*
	672-pin FineLine BGA	20 *(4)*	8 *(8)*	8	8 *(8)*
EP2C50	484-pin FineLine BGA	16 *(4)*	8 *(8)*	8	8 *(8)*
	672-pin FineLine BGA	20 *(4)*	8 *(8)*	8	8 *(8)*
EP2C70	672-pin FineLine BGA	20 *(4)*	8 *(8)*	8	8 *(8)*
	896-pin FineLine BGA	20 *(4)*	8 *(8)*	8	8 *(8)*

Notes to Table 9–2:

(1) Numbers are preliminary.
(2) EP2C5 and EP2C8 devices in the 144-pin TQFP package do not have any DQ pin groups in I/O bank 1.
(3) Because of available clock resources, only a total of 6 DQ/DQS groups can be implemented.
(4) Because of available clock resources, only a total of 14 DQ/DQS groups can be implemented.
(5) The ×9 DQS/DQ groups are also used as ×8 DQS/DQ groups. The ×18 DQS/DQ groups are also used as ×16 DQS/DQ groups.
(6) For QDRII implementation, if you connect the D ports (write data) to the Cyclone II DQ pins, the total available ×9 DQS /DQ and ×18 DQS/DQ groups are half of that shown in Table 9–2.
(7) Because of available clock resources, only a total of 3 DQ/DQS groups can be implemented.
(8) Because of available clock resources, only a total of 7 DQ/DQS groups can be implemented.

The DQS pins are listed in the Cyclone II pin tables as DQS[1..0]T, DQS[1..0]B, DQS[1..0]L, and DQS[1..0]R for the EP2C5 and EP2C8 devices and DQS[5..0]T, DQS[5..0]B, DQS[3..0]L, and DQS[3..0]R for the larger devices. The T denotes pins on the top of the device, the B denotes pins on the bottom of the device, the L denotes pins on the left of the device, and the R denotes pins on the right of the device. The corresponding DQ pins are marked as DQ[5..0]T[8..0], where [5..0] indicates which DQS group the pins belong to.

In the Cyclone II pinouts, the DQ groups with 9 DQ pins are also used in the ×8 mode with the corresponding DQS pins, leaving the unused DQ pin available as a regular I/O pin. The DQ groups that have 18 DQ pins are also used in the ×16 mode with the corresponding DQS pins, leaving the two unused DQ pins available as regular I/O pins. For example, DQ1T[8..0] can be used in the ×8 mode, provided it is used with DQS1T. The remaining unused DQ pin, DQ1T8, is available as a regular I/O pin.

When not used as DQ or DQS pins, these pins are available as regular I/O pins. Table 9–3 shows the number of DQS pins supported in each I/O bank in each Cyclone II device density.

Table 9–3. Available DQS Pins in Each I/O Bank & Each Device *Note (1)*

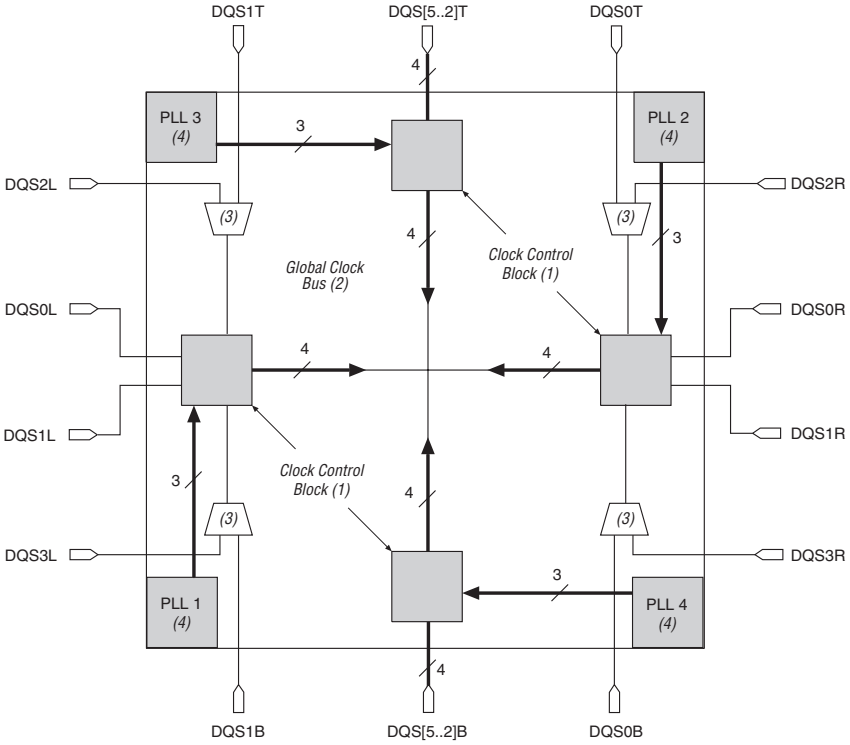
Device	Top I/O Bank	Bottom I/O Bank	Left I/O Bank	Right I/O Bank
EP2C5, EP2C8	DQS[1..0]T	DQS[1..0]B	DQS[1..0]L	DQS[1..0]R
EP2C15, EP2C20, EP2C35, EP2C50, EP2C70	DQS[5..0]B	DQS[5..0]T	DQS[3..0]L	DQS[3..0]R

Note to Table 9–3:
(1) Numbers are preliminary.

The DQ pin numbering is based on ×8/×9 mode. There are up to 8 DQS/DQ groups in ×8 mode or 4 DQS/DQ groups in ×9 mode in I/O banks for EP2C5 and EP2C8. For the larger devices, there are up to 20 DQS/DQ groups in ×8 mode or 8 DQS/DQ groups in ×9 mode. Although there are up to 20 DQS/DQ groups in the ×8 mode available in the larger Cyclone II devices, but because of the available clock resources in the Cyclone II devices, only 16 DQS/DQ groups can be utilized for the external memory interface. There is a total of 16 global clock buses available for routing DQS signals but 2 of them are needed for routing the –90° write clock and the system clock to the external memory devices. This reduces the global clock resources to 14 global clock buses for routing DQS signals. Incoming DQS signals are all routed to the clock control block, and are then routed to the global clock bus to clock the DDR LE registers. For EP2C5 and EP2C8 devices, the DQS signals are routed

directly to the clock control block. For the larger Cyclone II devices, the corner DQS signals are multiplexed before they are routed to the clock control block. When you use the corner DQS pins for DDR implementation, there is a degradation in the performance of the memory interface. The clock control block is used to select from a number of input clock sources, in this case either PLL clock outputs or DQS pins, to drive onto the global clock bus. Figure 9–7 shows the corner DQS signal mappings for EP2C15 through EP2C70 devices.

Figure 9–7. Corner DQS Signal Mapping for EP2C15–EP2C70 Devices



Notes to Figure 9–7:

(1) There are four control blocks on each side.
(2) There are a total of 16 global clocks available.
(3) Only one of the corner DQS pins in each corner can feed the clock control block at a time. The other DQS pins can be used as general purpose I/O pins.
(4) PLL resource can be lost if all DQS pins from one side are used at the same time.
(5) Top/bottom and side IOE have different timing.

For example, to implement a 72-bit wide SDRAM memory interface in Cyclone II devices, use 5 DQS/DQ groups in the top I/O bank and 4 DQS/DQ groups in the bottom I/O bank, or vice-versa. In this case, if DQS0T or DQS1T is used for the fifth DQS signal, the DQS2R or DQS2L pins become regular I/O pins and are unavailable for DQS signals in memory interface. For detailed information about the global clock network, refer to the *Global Clock Network & Phase Locked Loops* section in the *Cyclone II Architecture* chapter of the *Cyclone II Device Handbook*.

You must configure the DQ and DQS pins as bidirectional DDR pins on all the I/O banks of the device. Use the `altdq` and `altdqs` megafunctions to configure the DQ and DQS paths, respectively. If you only want to use the DQ or DQS pins as inputs, for instance in the QDRII memory interface where DQ and DQS are unidirectional read data and read clock, set the output enable of the DQ or DQS pins to ground. For further information, please refer to the section "QDRII SRAM" on page 9–5 of this handbook.

Clock, Command & Address Pins

You can use any of the user I/O pins on all the I/O banks (that support the external memory's I/O standard) of the device to generate clocks and command and address signals to the memory device.

Parity, DM & ECC Pins

You can use any of the DQ pins for the parity pins in Cyclone II devices. Cyclone II devices support parity in the ×8/×9 and ×16/×18 modes. There is one parity bit available per 8 bits of data pins.

The data mask (DM) pins are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal on the DM pin indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. In Cyclone II devices, the DM pins are pre-assigned in the device pin outs, and these are the preferred pins. Each group of DQS and DQ signals requires a DM pin. Similar to the DQ output signals, the DM signals are clocked by the –90° shifted clock.

Some DDR SDRAM and DDR2 SDRAM devices support error correction coding (ECC) or parity. Parity bit checking is a way to detect errors, but it has no correction capabilities. ECC can detect and automatically correct errors in data transmission. In 72-bit DDR SDRAM, there are 8 ECC pins on top of the 64 data pins. Connect the DDR and DDR2 SDRAM ECC pins to a Cyclone II device's DQS/DQ group. The memory controller needs extra logic to encode and decode the ECC data.

Phase Lock Loop (PLL)

When using the Cyclone II I/O banks to interface with the DDR memory, at least one PLL with two outputs is needed to generate the system clock and the write clock. The system clock generates the DQS write signals, commands, and addresses. The write clock shifts by –90° from the system clock and generates the DQ signals during writes.

Clock Delay Control

Clock delay control circuit on each DQS pin allows a phase shift that center-aligns the incoming DQS signals within the data window of their corresponding DQ data signals. The phase-shifted DQS signals drive the global clock network. This global DQS signal then clocks the DQ signals on internal LE registers. The clock delay control circuitry is used during the read operations where the DQS signals are acting as input clocks or strobes.

Figure 9–8 illustrates DDR SDRAM interfacing from the I/O pins through the dedicated circuitry to the logic array.

Figure 9–8. DDR SDRAM Interfacing

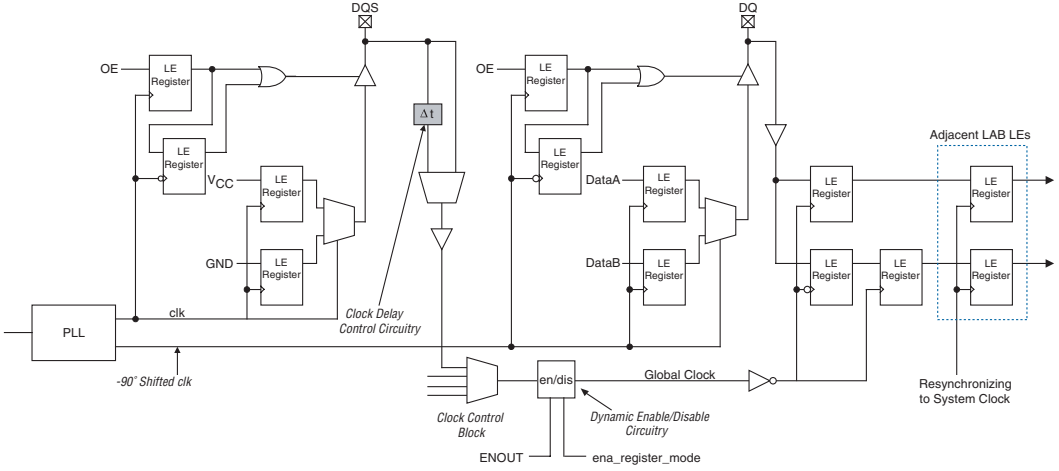


Figure 9–1 on page 9–4 shows an example where the DQS signal is shifted by 90°. The DQS signal goes through the 90° shift delay set by the clock delay control circuitry and global clock routing delay from the clock delay control circuitry to the DQ LE registers. The DQ signals only goes through routing delays from the DQ pin to the DQ LE registers. The delay

from DQS pin to the DQ LE register does not necessarily match the delay from the DQ pin to the DQ LE register. Therefore, you must adjust the clock delay control circuitry to compensate for this difference in delays.

DQS Postamble

For external memory interfaces that use a bidirectional read strobe, such as DDR and DDR2 SDRAM, the DQS signal is low before going to or coming from the high-impedance state (see Figure 9–1). The state where DQS is low just after high-impedance is called the preamble and the state where DQS is low just before it goes to high-impedance is called the postamble. There are preamble and postamble specifications for both read and write operations in DDR and DDR2 SDRAM. If the Cyclone II device or the DDR/DDR2 SDRAM device does not drive the DQ and DQS pins, the signals go to a high-impedance state. Because a pull-up resistor terminates both DQ and DQS to V_{TT} (1.25 V for SSTL-2 and 0.9 V for SSTL-18), the effective voltage on the high-impedance line is either 1.25 V or 0.9 V. According to the JEDEC JESD8-9 specification for SSTL-2 I/O standard and the JESD8-15A specification for SSTL-18 I/O standard, this is an indeterminate logic level, and the input buffer can interpret this as either a logic high or logic low. If there is any noise on the DQS line, the input buffer may interpret that noise as actual strobe edges.

Cyclone II devices have non-dedicated logic that can be configured to prevent a false edge trigger at the end of the DQS postamble. Each Cyclone II DQS signal is connected to postamble logic that consists of a D flip flop (see Figure 9–9). This register is clocked by the shifted DQS signal. Its input is connected to ground. The controller needs to include extra logic to tell the reset signal to release the preset signal on the falling DQS edge at the start of the postamble. This disables any glitches that happen right after the postamble. This postamble logic is automatically implemented by the Altera MegaCore DDR/DDR2 SDRAM Controller in the LE register as part of the open-source datapath.

Figure 9–9. Cyclone II DQS Postamble Circuitry Connection

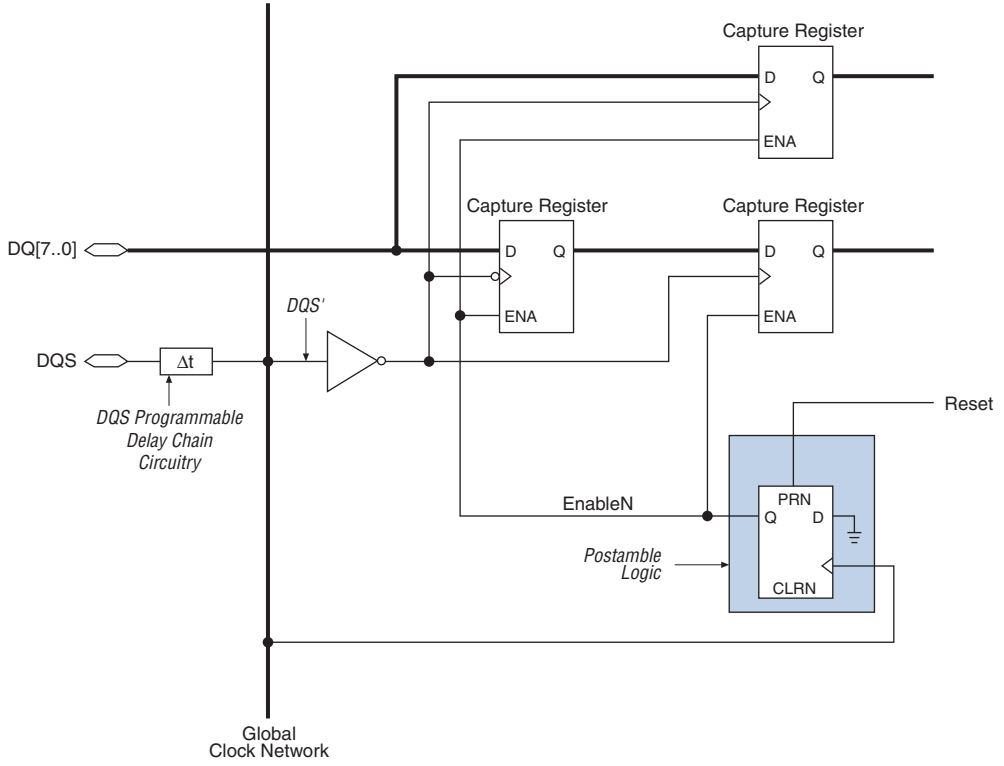
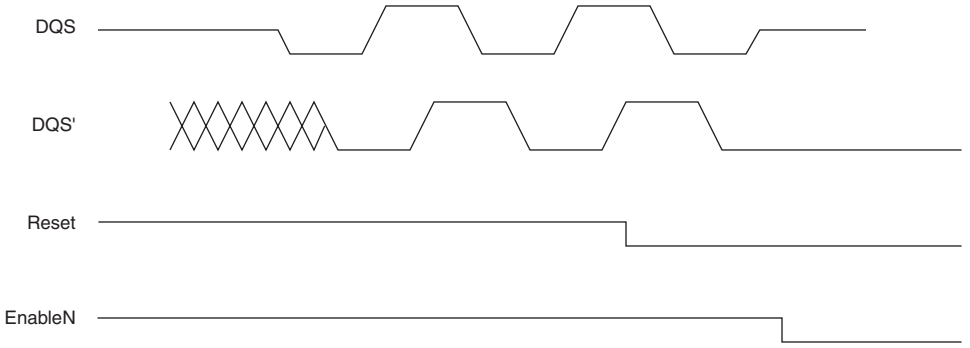


Figure 9–10 shows the timing waveform for Figure 9–9. When the postamble logic detects the falling DQS edge at the start of postamble, it sends out a signal to disable the capture registers to prevent any accidental latching.

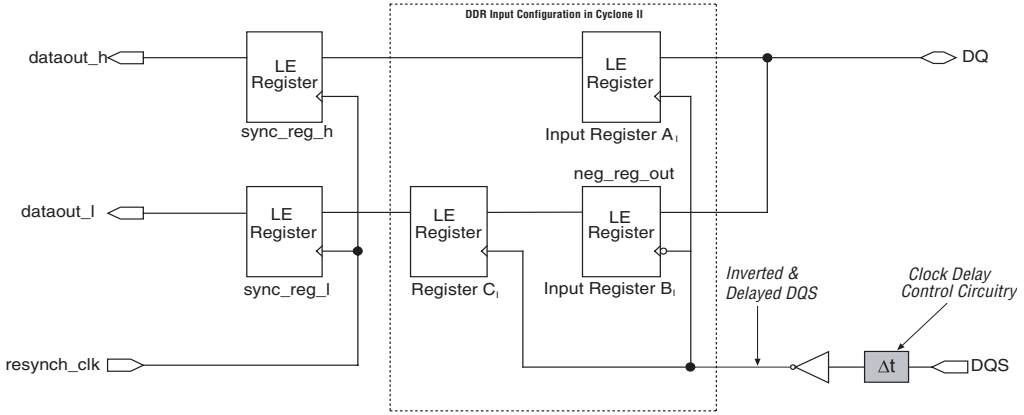
Figure 9–10. Cyclone II DQS Postamble Circuitry Control Timing Waveform



DDR Input Registers

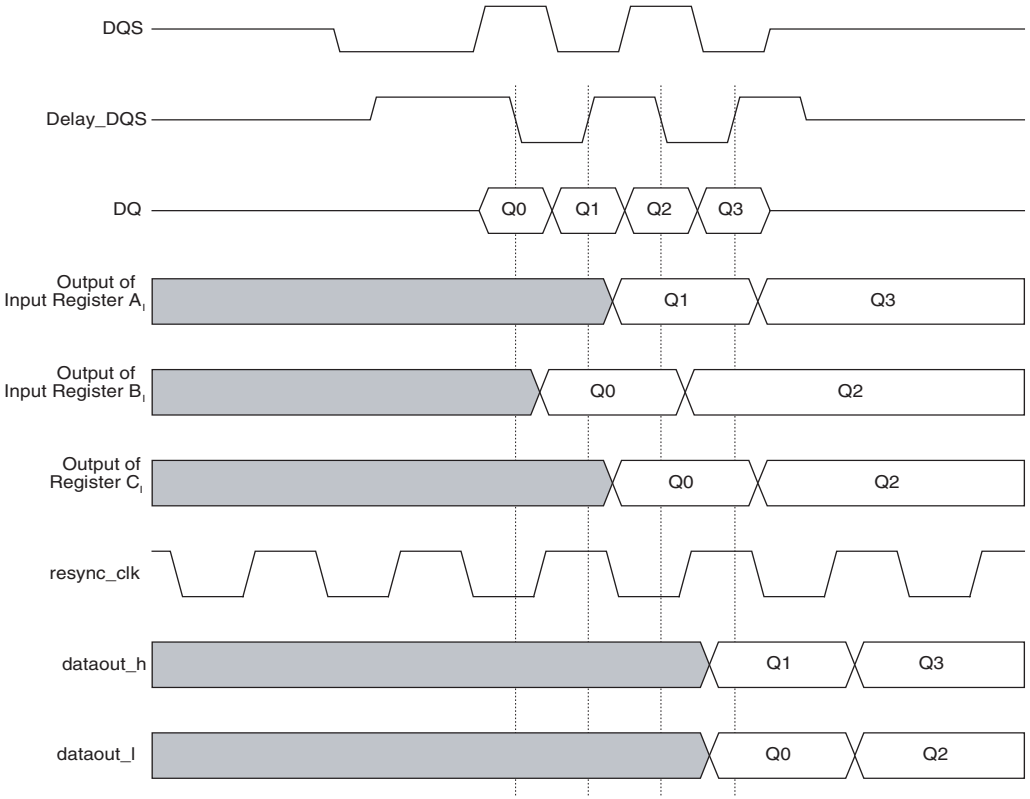
In Cyclone II devices, the DDR input registers are implemented with five internal LE registers located in the logic array block (LAB) adjacent to the DDR input pin (see Figure 9–11). The DDR data is fed to the first two registers, input register A_I and input register B_I. Input register B_I captures the DDR data present during the rising edge of the clock. Input register A_I captures the DDR data present during the falling edge of the clock. Register C_I aligns the data before it is transferred to the resynchronization registers.

Figure 9–11. DDR Input Implementation



Registers sync_reg_h and sync_reg_l synchronize the two data streams to the rising edge of the resynchronization clock. Figure 9–12 shows examples of functional waveforms from a double data rate input implementation.

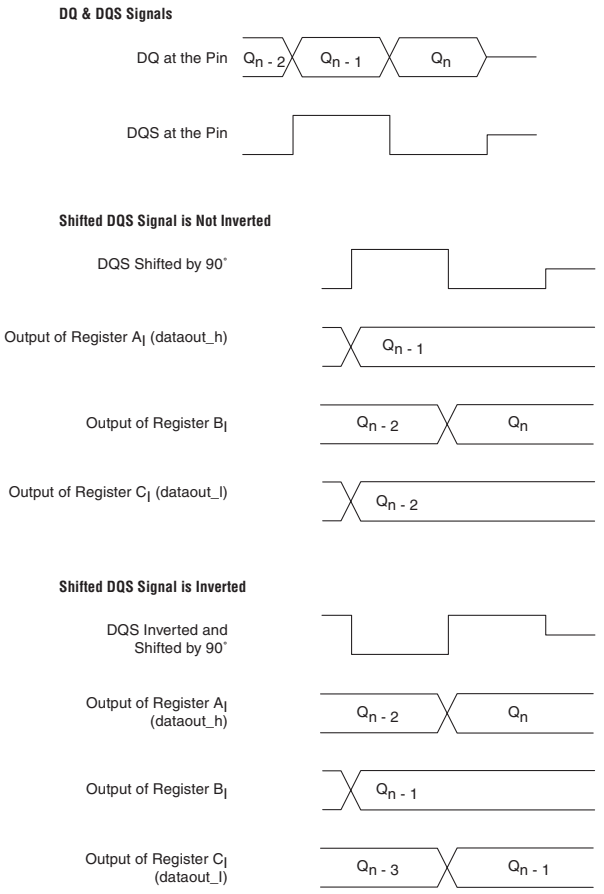
Figure 9–12. DDR Input Functional Waveforms



The Cyclone II DDR input registers require you to invert the incoming DQS signal to ensure proper data transfer. The altdq megafunction automatically adds the inverter on the clock port of the DQ signals. As shown in Figure 9–11, the inverted DQS signal's rising edge clocks register A_I, its falling edge clocks register B_I, and register C_I aligns the data clocked by register B_I with register A_I on the inverted DQS signal's rising edge. In a DDR memory read operation, the last data coincides with the falling edge of DQS signal. If you do not invert the DQS pin, you do not get this last data because the register does not latch until the next rising edge of the DQS signal.

Figure 9–13 shows waveforms of the circuit shown in Figure 9–11. The first set of waveforms in Figure 9–13 shows the edge-aligned relationship between the DQ and DQS signals at the Cyclone II device pins. The second set of waveforms in Figure 9–13 shows what happens if the shifted DQS signal is not inverted. In this case, the last data, Q_n, does not get latched into the logic array as DQS goes to tri-state after the read postamble time. The third set of waveforms in Figure 9–13 shows a proper read operation with the DQS signal inverted after the 90° shift. The last data, Q_n, does get latched. In this case the outputs of register A_I and register C_I, which correspond to `dataout_h` and `dataout_l` ports, are now switched because of the DQS inversion. Register A_I, register B_I, and register C_I refer to the nomenclature in Figure 9–11.

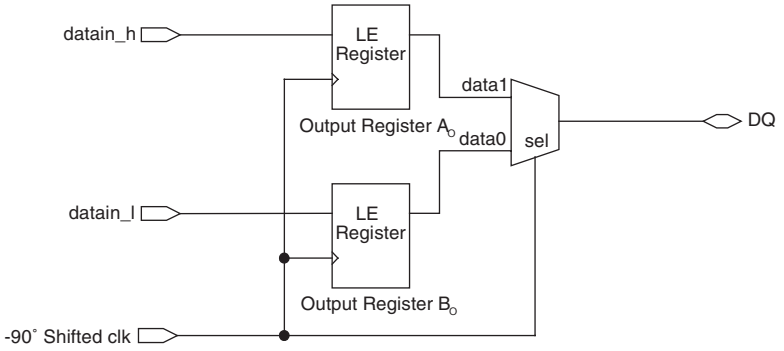
Figure 9–13. DQ Captures With Noninverted & Inverted Shifted DQS



DDR Output Registers

Figure 9–14 shows a schematic representation of DDR output implemented in a Cyclone II device. The DDR output logic is implemented using LEs in the LAB adjacent to the output pin. Two registers synchronize two serial data streams. The registered outputs are then multiplexed by the common clock to drive the DDR output pin at two times the data rate.

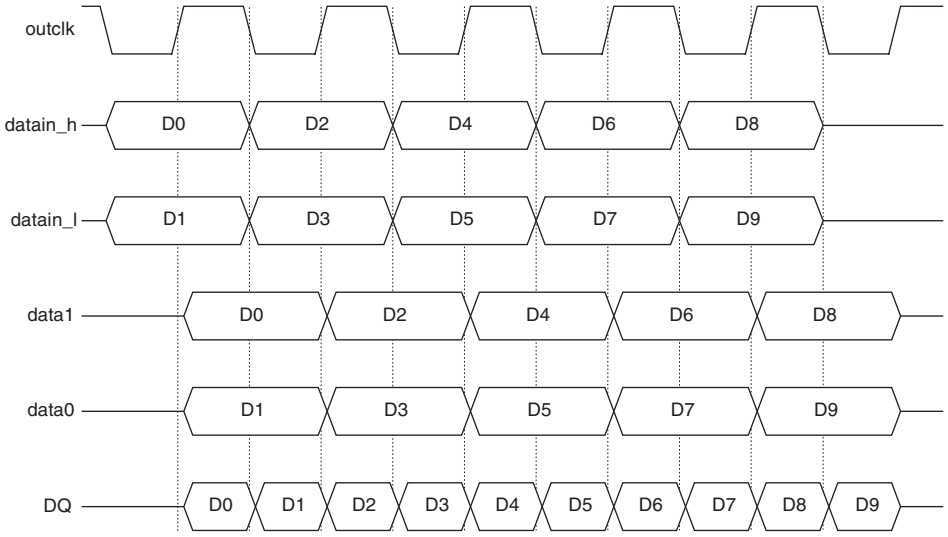
Figure 9–14. DDR Output Implementation for DDR Memory Interfaces



While the clock signal is logic-high, the output from output register A_O is driven onto the DDR output pin. While the clock signal is logic-low, the output from output register B_O is driven onto the DDR output pin. The DDR output pin can be any available user I/O pin. Altera recommends the use of `altdq` and `altdqs` megafunctions to implement this output logic. This automatically provides the required tight placement and routing constraints on the LE registers and the output multiplexer.

Figure 9–15 shows examples of functional waveforms from a DDR output implementation.

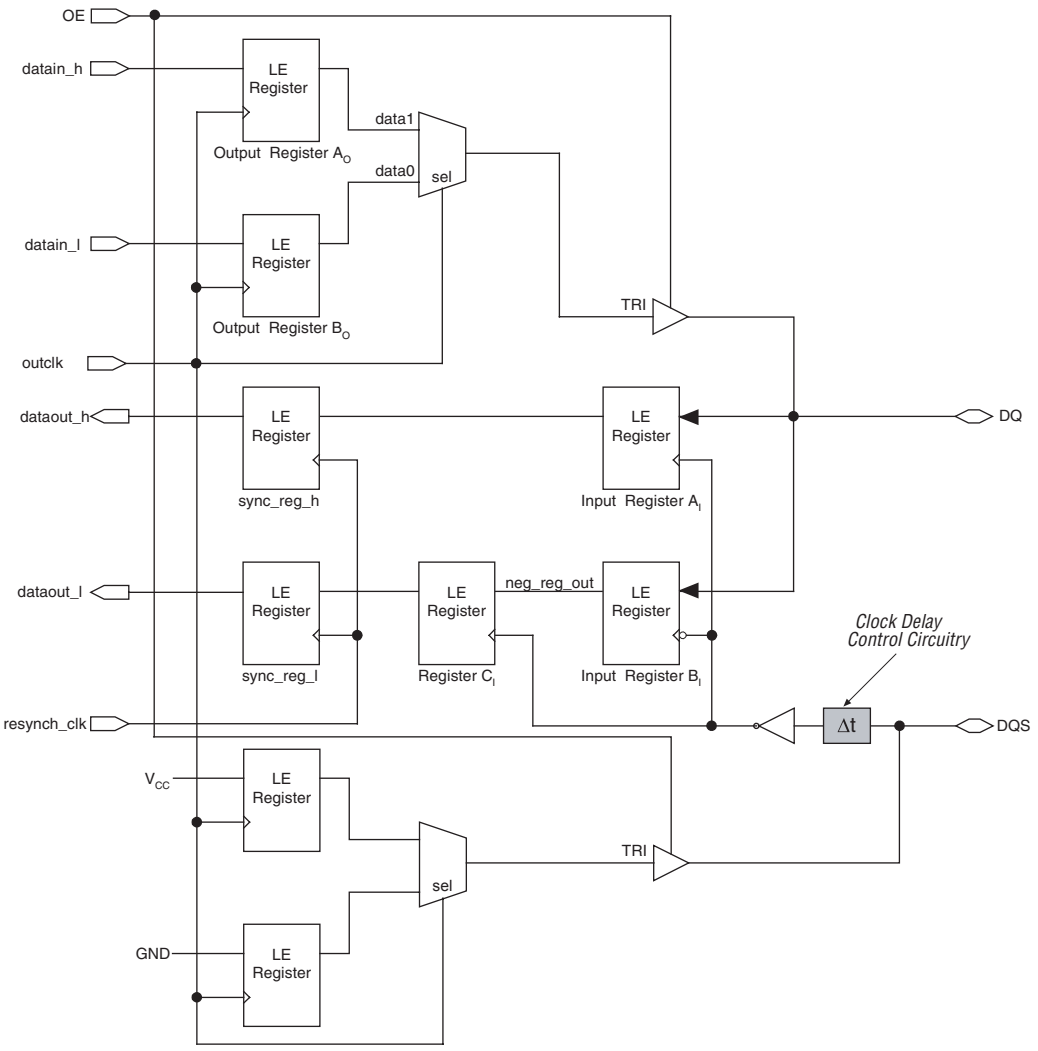
Figure 9–15. DDR Output Waveforms



Bidirectional DDR Registers

Figure 9–16 shows a bidirectional DDR interface constructed using the DDR input and DDR output examples described in the previous two sections. As with the DDR input and DDR output examples, the bidirectional DDR pin can be any available user I/O pin. The registers that implement DDR bidirectional logic are LEs in the LAB adjacent to that pin. The tri-state buffer controls when the device drives data onto the bidirectional DDR pin.

Figure 9–16. Bidirectional DDR Implementation for DDR Memory Interfaces *Note (1)*

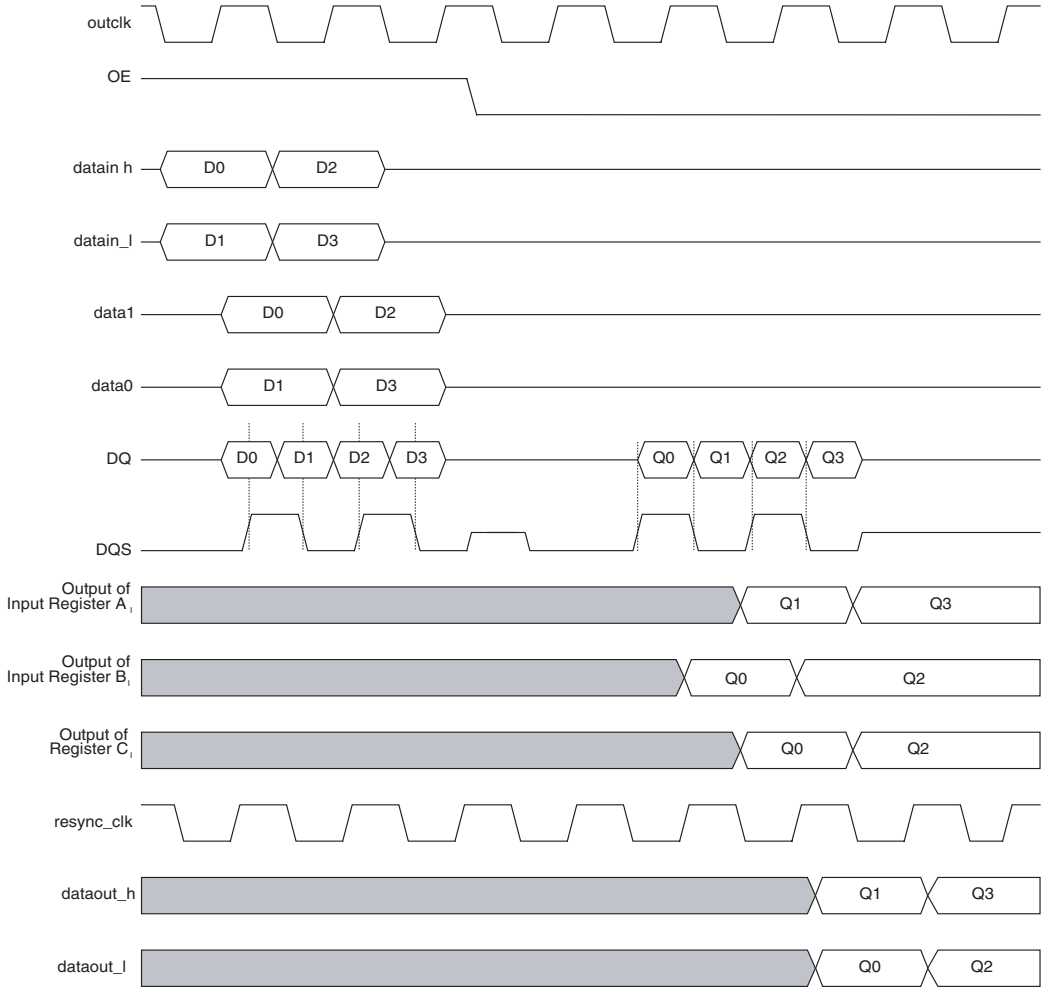


Note to Figure 9–16:

(1) You can use the `altdq` and `altdqs` megafunctions to generate the DQ and DQS signals.

Figure 9–17 shows example waveforms from a bidirectional DDR implementation.

Figure 9–17. DDR Bidirectional Waveforms



Conclusion

Cyclone II devices support SDR SDRAM, DDR SDRAM, DDR2 SDRAM, and QDRII SRAM external memories. Cyclone II devices feature high-speed interfaces that transfer data between external memory devices at up to 167 MHz/333 Mbps for DDR and DDR2 SDRAM devices and 167 MHz/667 Mbps for QDRII SRAM devices. The clock delay control circuitry allows you to fine tune the phase shift for the input clocks or strobes to properly align clock edges as needed to capture data.

Document Revision History

Table 9–4 shows the revision history for this document.

Table 9–4. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v3.1	• Added document revision history. • Added handpara note in "Data & Data Strobe Pins" section. • Updated "DDR Output Registers" section.	• Elaboration of DDR2 and QDRII interfaces supported by I/O bank included.
November 2005, v2.1	• Introduction • Updated Table 9–2. • Updated Figure 9–7.	
July 2005, v2.0	Updated Table 9–2.	
November 2004, v1.1	• Moved the "External Memory Interface Standards" section to follow the "Introduction" section. • Updated the "Data & Data Strobe Pins" section. • Updated Figures 9–11, 9–12, 9–15, 9–16, and 9–17.	
June 2004, v1.0	Added document to the Cyclone II Device Handbook.	