

The Cyclone® III device family (Cyclone III and Cyclone III LS devices) offers hot-socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove Cyclone III device family or a board in a system during system operation without causing undesirable effects to the running system bus or the board that is inserted into the system.

The hot-socketing feature removes some of the difficulties that you encounter when you use Cyclone III device family on a PCB that contains a mixture of 3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V devices. With the hot-socketing feature of Cyclone III device family, you no longer need to ensure a proper power up sequence for each device on the board.

Cyclone III device family hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also describes the power-on reset (POR) circuitry in Cyclone III device family. The POR circuitry keeps the devices in the reset state until the power supplies are in operating range.

This chapter contains the following sections:

- “Hot-Socketing Specifications” on page 10–1
- “Hot-Socketing Feature Implementation” on page 10–3
- “POR Circuitry” on page 10–3

Hot-Socketing Specifications

Cyclone III device family is a hot-socketing compliant without the need for any external components or special design requirements. Hot-socketing support in Cyclone III device family has the following advantages:

- You can drive the device before power-up without damaging the device.
- I/O pins remain tristated during power-up. The device does not drive out before or during power-up, therefore not affecting other buses in operation.

Devices Driven Before Power-Up

You can drive signals into I/O pins, dedicated input pins, and dedicated clock pins of Cyclone III device family before or during power-up or power down without damaging the device. The Cyclone III device family supports any power-up or power down sequence (V_{CCIO} , V_{CCINT}) to simplify system level design.

I/O Pins Remain Tristated During Power-Up

The output buffers of Cyclone III device family are turned off during system power up or power down. Cyclone III device family does not drive out until the device is configured and working in recommended operating conditions. The I/O pins are tristated until the device enters user mode with a weak pull-up resistor (R) to V_{CCIO} .

You can power-up or power down the V_{CCIO} , V_{CCA} , and V_{CCINT} pins in any sequence. The V_{CCIO} , V_{CCA} , and V_{CCINT} pins must have a monotonic rise to their steady state levels. The maximum power ramp rate is 3 ms for fast POR time and 50 ms for standard POR time. The minimum power ramp rate is 50 μ s. V_{CCIO} for all I/O banks must be powered up during device operation. All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time. V_{CCD_PLL} must always be connected to V_{CCINT} through a decoupling capacitor and ferrite bead. During hot-socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

Cyclone III device family meets the following hot-socketing specification:

- The hot-socketing DC specification is $|I_{IOPIN}| < 300 \mu\text{A}$
- The hot-socketing AC specification is $|I_{IOPIN}| < 8 \text{ mA}$ for the ramp rate of 10 ns or more

For ramp rates faster than 10 ns on I/O pins, $|I_{IOPIN}|$ is obtained with the equation $I = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate. The hot-socketing specification takes into account the pin capacitance but not board trace and external loading capacitance. You must consider additional or separate capacitance for trace, connector, and loading. I_{IOPIN} is the current for any user I/O pins on the device. The DC specification applies when all V_{CC} supplied to the device is stable in the powered-up or powered-down conditions.

A possible concern for semiconductor devices in general regarding hot-socketing is the potential for latch up. Latch up can occur when electrical subsystems are hot-socketed into an active system. During hot-socketing, the signal pins may be connected and driven by the active system before the power supply can provide current to the V_{CC} of the device and ground planes. This condition can lead to latch up and cause a low-impedance path from V_{CC} to ground in the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

The design of the I/O buffers and hot-socketing circuitry ensures that Cyclone III device family are immune to latch up during hot-socketing.



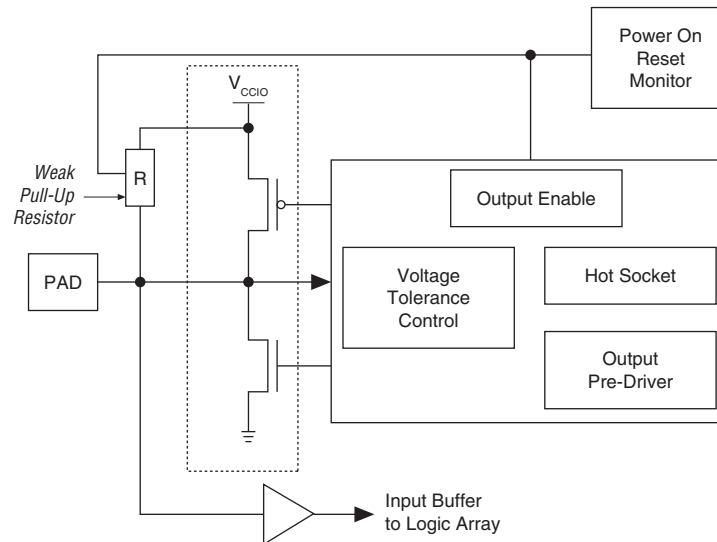
For more information about the hot-socketing specification, refer to the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters and the *Hot-Socketing and Power-Sequencing Feature and Testing for Altera Devices* white paper.

Hot-Socketing Feature Implementation


Each I/O pin has the circuitry shown in Figure 10-1. The hot-socketing circuit does not include CONF_DONE, nCEO, and nSTATUS pins to ensure that they are able to operate during configuration. Thus, it is expected behavior for these pins to drive out during power up and power down sequences.

Figure 10-1 shows the hot-socketing circuit block diagram for Cyclone III device family.

Figure 10-1. Hot-socketing Circuit Block Diagram for Cyclone III Device Family



The POR circuit monitors the voltage level of power supplies and keeps the I/O pins tristated until the device is in user mode. The weak pull-up resistor (R) in Cyclone III device family I/O element (IOE) keeps the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} , V_{CC} , and V_{CCA} supplies are powered up, and it prevents the I/O pins from driving out when the device is not in user mode.

 Altera uses GND as reference for hot-socketing operation and I/O buffer designs. To ensure proper operation, Altera recommends connecting the GND between boards before connecting the power supplies. This prevents the GND on your board from being pulled up inadvertently by a path to power through other components on your board. A pulled up GND can otherwise cause an out-of-specification I/O voltage or current condition with the Altera® device.

POR Circuitry

Cyclone III device family contains POR circuitry to keep the device in a reset state until the power supply voltage levels have stabilized during power up. During POR, all user I/O pins are tristated until the V_{CC} reaches the recommended operating levels. In addition, the POR circuitry also ensures the V_{CCIO} level of I/O banks 1, 6, 7, and 8 that contains configuration pins reach an acceptable level before configuration is triggered.

The POR circuit of the Cyclone III device monitors the V_{CCINT} , V_{CCIO} (banks 1, 6, 7, and 8), and V_{CCA} pins during power-on. The enhanced POR circuit of the Cyclone III LS device includes monitoring V_{CCBAT} to ensure that V_{CCBAT} is always at the minimum requirement voltage level.

 The V_{CCBAT} power supply is the new design security feature power supply introduced for Cyclone III LS devices only. Cyclone III devices do not have V_{CCBAT} power supply.

After Cyclone III device family enters user mode, the POR circuit continues to monitor the V_{CCINT} or V_{CCA} pins so that a brown-out condition during user mode is detected. If the V_{CCINT} or V_{CCA} voltage sags below the POR trip point during user mode, the POR circuit resets the device. If the V_{CCIO} voltage sags during user mode, the POR circuit does not reset the device.

In some applications, it is necessary for a device to wake up very quickly to begin operation. Cyclone III device family offers the Fast-On feature to support fast wake-up time applications. For Cyclone III device family, the $MSEL[3..0]$ pin settings determine the POR time (t_{POR}) of the device. Fast POR ranges from 3 ms to 9 ms, while standard POR ranges from 50 ms to 200 ms.

If you cannot meet the maximum V_{CC} ramp time requirement, use an external component to hold $nCONFIG$ low until the power supplies have reached their minimum recommend operating levels. Otherwise, the device may not properly configure and enter user mode.

 For more information about the $MSEL[3..0]$ pin settings, refer to the *Configuration, Design Security, and Remote System Upgrades in the Cyclone III Device Family* chapter.

 For more information about the V_{CCBAT} pin connection, refer to the *Cyclone III Device Family Pin Connection Guidelines*.

Document Revision History

Table 10-1 lists the revision history for this document.

Table 10-1. Document Revision History (Part 1 of 2)

Date	Version	Changes
July 2012	3.4	Updated tolerance control circuit voltage level in the “Hot-Socketing Feature Implementation” section.
December 2011	3.3	<ul style="list-style-type: none"> ■ Updated “POR Circuitry” on page 10-3. ■ Updated hyperlinks. ■ Minor text edits.
December 2009	3.2	Minor changes to the text.
July 2009	3.1	Made minor correction to the part number.
June 2009	3.0	<ul style="list-style-type: none"> ■ Updated chapter part number. ■ Updated “I/O Pins Remain Tristated During Power-Up” on page 10-2. ■ Updated “Hot-Socketing Feature Implementation” on page 10-3. ■ Updated “POR Circuitry” on page 10-4.

Table 10–1. Document Revision History (Part 2 of 2)

Date	Version	Changes
October 2008	1.2	<ul style="list-style-type: none">■ Updated chapter to new template.■ Added handnote to the “Cyclone III Hot-Socketing Specifications” section.
July 2007	1.1	<ul style="list-style-type: none">■ Updated “I/O Pins Remain Tri-stated During Power-Up” section.■ Updated Figure 10–3.■ Added chapter TOC and “Referenced Documents” section.
March 2007	1.0	Initial release.

