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1 Intel® High Level Synthesis (HLS) Compiler Getting Started Guide

The Intel® High Level Synthesis (HLS) Compiler is part of Intel Quartus® Prime design software. The Intel HLS Compiler synthesizes a C++ function into an RTL implementation that is optimized for Intel FPGA products. The compiler is sometimes referred to as the i++ compiler, reflecting the name of the compiler command.

The *Intel High Level Synthesis Compiler Getting Started Guide* describes the procedures to set up the Intel HLS Compiler and to run an HLS design example.

1.1 Intel High Level Synthesis Compiler Prerequisites

To install the Intel HLS Compiler, install Intel Quartus Prime Standard Edition software or the Intel Quartus Prime Pro Edition software. The Intel HLS Compiler is installed as part of the Intel Quartus Prime software installation, but it requires additional software to use. For detailed instructions for installing Intel Quartus Prime software, including system requirements, prerequisites, and licensing requirements, see *Intel FPGA Software Installation and Licensing.*
Additional Software Requirements

The Intel HLS Compiler requires the following additional software:

- **C++ compiler:**
  - *Linux C++ compiler*  
    GCC compiler and C++ Libraries version 4.4.7
    *Important:* Newer versions of the GCC compiler are not supported.
  - *Windows C++ compiler*  
    Microsoft Visual Studio 2010 Professional
    *Important:* Newer versions of Microsoft Visual Studio are not supported.

- **Mentor Graphics* ModelSim* software:**
  You can install either of the following editions of ModelSim from the Intel Quartus Prime software installer:
  - ModelSim - Intel FPGA Edition
  - ModelSim - Intel FPGA Starter Edition
  You can also use your own independently obtained and licensed version of Mentor Graphics ModelSim software.
  For version information on all supported ModelSim software, refer to the "EDA Interface Information" section in one of the following documents:

Related Links

- Supported Operating Systems
- Mentor Graphics Website
- EDA Interface Information - Quartus Prime Standard Edition Software
- EDA Interface Information - Quartus Prime Pro Edition Software

1.2 Initializing the Intel HLS Compiler Environment

Before you can compile your component with the Intel HLS Compiler i++ command, a number of environment variables must be set for the i++ command to run successfully.

The Intel HLS Compiler environment initialization script applies only to the environment variable settings in your *current* terminal or command prompt session. You must initialize the Intel HLS Compiler environment each time that you start a terminal or command prompt session to develop your design.

To set the environment variables permanently, follow your operating system's standard procedure for making persistent changes to environment variable settings. Review the output of the environment initialization script to determine the environment variables to set permanently.
To initialize your current terminal or command prompt session so that you can run the Intel HLS Compiler:

- On Linux systems, initialize your environment as follows:
  a. In your terminal session, change directories to the hls directory in your Intel Quartus Prime installation directory.
     For example, `/home/<username>/intelFPGA_pro/17.1/hls`
  b. Run the following command from the hls directory to set the environment variables for the i++ command in the current terminal session:
     ```
     source init_hls.sh
     ```
     The command prints out the modified environment variable settings.
     The environment initialization script shows the environment variables that it set, and you can now run the i++ command from this terminal session.

- On Windows systems, initialize your environment as follows:
  a. In your command prompt session, change directories to the hls directory in your Intel Quartus Prime installation directory.
     For example, `C:\intelFPGA_pro\17.1\hls`
  b. Run the following command from the hls directory to set the environment variables for the i++ command in the current terminal session:
     ```
     init_hls.bat
     ```
     The command prints out the modified environment variable settings.
     The environment initialization script shows the environment variables that it set, and you can now run the i++ command from this command prompt session.
2 High Level Synthesis (HLS) Design Examples and Tutorials

The Intel High Level Synthesis (HLS) Compiler includes design examples and tutorials to provide you with example implementations and demonstrate ways to model or code your components to get the best results from the Intel HLS Compiler for your design.

High Level Synthesis Design Examples

The high level synthesis (HLS) design examples give you a quick way to see how various algorithms can be effectively implemented to get the best results from the Intel HLS Compiler.

You can find the HLS design examples in the following location:

```
<quartus_installdir>/hls/examples/<design_example_name>
```

Where `<quartus_installdir>` is the directory where you installed the Intel Quartus Prime Design Suite. For example, `/home/<username>/intelFPGA_pro/17.1` or `C:\intelFPGA_pro\17.1`.

For instructions on running the examples, see the following sections:
- Running a High Level Synthesis (HLS) Design Example (Linux) on page 8
- Running a High Level Synthesis (HLS) Design Example (Windows) on page 9

### Table 1. HLS design examples

<table>
<thead>
<tr>
<th>Focus area</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear algebra</td>
<td>QRD</td>
<td>Uses the Modified Gram-Schmidt algorithm for QR factorization of a matrix.</td>
</tr>
<tr>
<td>Signal processing</td>
<td>interp_decim_filter</td>
<td>Implements a simple and efficient interpolation/decimation filter.</td>
</tr>
<tr>
<td>Simple design</td>
<td>counter</td>
<td>Implements a simple and efficient 32-bit counter component.</td>
</tr>
<tr>
<td>Video processing</td>
<td>YUV2RGB</td>
<td>Implements a basic YUV422 to RGB888 color space conversion.</td>
</tr>
<tr>
<td>Video processing</td>
<td>image_downsample</td>
<td>Implements an image downsampling algorithm to scale an image to a smaller size using bilinear interpolation.</td>
</tr>
</tbody>
</table>

HLS Design Tutorials

The HLS design tutorials show you important concepts to know when programming for the Intel HLS Compiler as well demonstrating good coding practices.

You can find the HLS design tutorials in the following location:

```
<quartus_installdir>/hls/examples/tutorials/<tutorial_name>
```

Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

*Other names and brands may be claimed as the property of others.
Where `<quartus_installdir>` is the directory where you installed the Intel Quartus Prime Design Suite. For example, `/home/<username>/intelFPGA_pro/17.1/hls` or `C:\intelFPGA_pro\17.1\hls`.

Each tutorial has a README file that gives you details about what the tutorial covers and instructions on how to run the tutorial.

### Table 2. HLS design tutorials

<table>
<thead>
<tr>
<th>Focus area</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arbitrary precision</td>
<td><code>ac_fixed_constructor</code></td>
<td>Demonstrates the use of the <code>ac_fixed</code> constructor where you can get a better QoR by using minor variations in coding style.</td>
</tr>
<tr>
<td>types</td>
<td><code>ac_fixed_math_library</code></td>
<td>Demonstrates the use of the Intel HLS Compiler <code>ac_fixed_math</code> fixed point math library functions.</td>
</tr>
<tr>
<td></td>
<td><code>ac_int_basic_ops</code></td>
<td>Demonstrates the operators available for the <code>ac_int</code> class.</td>
</tr>
<tr>
<td></td>
<td><code>ac_int_overflow</code></td>
<td>Demonstrates the usage of the <code>DEBUG_AC_INT_WARNING</code> and <code>DEBUG_AC_INT_ERROR</code> keywords to help detect overflow during emulation runtime.</td>
</tr>
<tr>
<td>Component memories</td>
<td><code>bank_bits</code></td>
<td>Demonstrates how to control component internal memory architecture for parallel memory access by enforcing which address bits are used for banking.</td>
</tr>
<tr>
<td></td>
<td><code>depth_wise_merge</code></td>
<td>Demonstrates how to improve resource utilization by implementing two logical memories as a single physical memory with a depth equal to the sum of the depths of the two original memories.</td>
</tr>
<tr>
<td></td>
<td><code>static_var_init</code></td>
<td>Demonstrates the <code>hls_init_on_power</code> and <code>hls_init_on_reset</code> flags for static variables and their impact on area and latency.</td>
</tr>
<tr>
<td></td>
<td><code>width_wise_merge</code></td>
<td>Demonstrates how to improve resource utilization by implementing two logical memories as a single physical memory with a width equal to the sum of the widths of the two original memories.</td>
</tr>
<tr>
<td>Interfaces</td>
<td><code>explicit_streams_buffer</code></td>
<td>Demonstrates how to use explicit <code>stream_in</code> and <code>stream_out</code> interfaces in the component and testbench.</td>
</tr>
<tr>
<td></td>
<td><code>explicit_streams_packet</code></td>
<td>Demonstrates how to use the <code>usesPackets</code>, <code>usesValid</code>, and <code>usesReady</code> stream template parameters.</td>
</tr>
<tr>
<td></td>
<td><code>mm_master_testbench_operators</code></td>
<td>Demonstrates how to invoke a component at different indices of an Avalon Memory Mapped (MM) Master (<code>mm_master</code> class) interface.</td>
</tr>
<tr>
<td></td>
<td><code>mm_slaves</code></td>
<td>Demonstrates how to create Avalon-MM Slave interfaces (slave registers and slave memories).</td>
</tr>
<tr>
<td></td>
<td><code>multiple_stream_call_sites</code></td>
<td>Demonstrates the benefits of using multiple stream call sites.</td>
</tr>
<tr>
<td></td>
<td><code>pointer-mm_master</code></td>
<td>Demonstrates how to create Avalon-MM Master interfaces and control their parameters.</td>
</tr>
<tr>
<td>Best practices</td>
<td><code>const-global</code></td>
<td>Demonstrates the performance and resource utilization improvements of using <code>const</code> qualified global variables.</td>
</tr>
<tr>
<td></td>
<td><code>floating_point_ops</code></td>
<td>Demonstrates the impact of <code>--fpc</code> and <code>--fp-relaxed</code> flags in <code>i++</code> on floating point operations.</td>
</tr>
<tr>
<td>Focus area</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>--------------------</td>
<td>---------------------------</td>
<td>-----------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td></td>
<td>integer_promotion</td>
<td>Demonstrates how integer promotion rules can influence the behavior of a C or C++ program.</td>
</tr>
<tr>
<td></td>
<td>loop_memory_dependency</td>
<td>Demonstrates breaking loop carried dependencies using the ivdep pragma.</td>
</tr>
<tr>
<td></td>
<td>parameter_aliasing</td>
<td>Demonstrates the use of the restrict keyword on component arguments.</td>
</tr>
<tr>
<td></td>
<td>resource_sharing_filter</td>
<td>Demonstrates the following versions of a 32-tap finite impulse response (FIR) filter design:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• optimized-for-throughput variant</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• optimized-for-area variant</td>
</tr>
<tr>
<td></td>
<td>shift_register</td>
<td>Demonstrates the recommended coding style for implementing shift registers.</td>
</tr>
<tr>
<td></td>
<td>single_vs_double_precision_math</td>
<td>Demonstrates the effect of using single precision literals and functions instead of double precision literals and functions.</td>
</tr>
<tr>
<td></td>
<td>struct_interface</td>
<td>Demonstrates how to use ac_int to implement interfaces with no padding bits.</td>
</tr>
<tr>
<td></td>
<td>swap_vs_copy</td>
<td>Demonstrates the impact of using deep copying with registers on the performance and resource utilization of a component design.</td>
</tr>
<tr>
<td>Usability</td>
<td>compiler_interoperability</td>
<td>Demonstrates how to use testbench code compiled with the native compilers for Linux (GCC) or Windows (Microsoft Visual Studio) along with code compile by the i++ command.</td>
</tr>
<tr>
<td></td>
<td>enqueue_call</td>
<td>Demonstrates how to run components asynchronously in the testbench using enqueue functionality.</td>
</tr>
<tr>
<td></td>
<td>qsys_2xclock</td>
<td>Demonstrates the recommended clock and reset generation for a component with a clock2x input.</td>
</tr>
<tr>
<td></td>
<td>qsys_stitching</td>
<td>Demonstrates how to combine multiple components to function as a single cohesive design.</td>
</tr>
</tbody>
</table>

### 2.1 Running a High Level Synthesis (HLS) Design Example (Linux)

To run an HLS design example, first compile your source code to an x86-64 binary executable and then to a simulated hardware executable.

1. Start a terminal session and initialize the Intel HLS Compiler environment.
   For instructions how to initialize the environment, see Initializing the Intel HLS Compiler Environment on page 4.

2. Navigate to the `<quartus_installdir>/hls/examples/<design_example_name>` directory, where `<quartus_installdir>` is the directory where you installed Intel Quartus Prime software.
   For example, `/home/<username>/intelFPGA_pro/17.1`.

3. Run the make `test-x86-64` command to compile the C++ source code to an x86-64 binary executable and then run the generated executable on the CPU. Expected outcome after you run the `make test-x86-64` command:
• The console displays the command it uses to generate the binary (for example, `i++ -march=x86-64 -o test-x86-64 <source_files>`).

• The HLS compiler creates an executable file (for example, `test-x86-64`) in the current working directory.

• The console displays the output of the executable to signify a successful execution.

4. Run the `make test-fpga` command. The command compiles the C++ source code to a hardware executable and then runs a simulation of the generated HDL. Expected outcome after you run the `make test-fpga` command:

• The console displays the command it uses to generate the testbench binary and the contents of the project directory (for example, `i++ -march="<FPGA_family_or_part_number>" -o test-fpga <source_files>`).

• The HLS compiler creates a `.prj` directory (for example, `test-fpga.prj`) in the current working directory.

• The console displays the output of the executable to signify a successful execution.

2.2 Running a High Level Synthesis (HLS) Design Example (Windows)

To run an HLS design example, first compile your source code to an x86-64 binary executable and then to a simulated hardware executable.

1. Start a terminal session and initialize the Intel HLS Compiler environment.
   For instructions how to initialize the environment, see Initializing the Intel HLS Compiler Environment on page 4.

2. Navigate to the `<quartus_installdir>/hls/examples/<design_example_name>` directory, where `<quartus_installdir>` is the directory where you installed Intel Quartus Prime software.
   For example, `C:\intelFPGA_pro\17.1`.

3. Run the `build.bat test-x86-64` command to compile the C++ source code to an x86-64 binary executable and then run the generated executable on the CPU. Expected outcome after you run the `build.bat test-x86-64` command:

• The console displays the command it uses to generate the binary (for example, `i++ -march=x86-64 -o test-x86-64 <source_files>`).

• The HLS compiler creates an executable file (for example, `test-x86-64`) in the current working directory.

• The console displays the output of the executable to signify a successful execution.

4. Run the `build.bat test-fpga` command. The command compiles the C++ source code to a hardware executable and then runs a simulation of the generated HDL. Expected outcome after you run the `build.bat test-fpga` command:
• The console displays the command it uses to generate the testbench binary and the contents of the project directory (for example, `i++ -march="<FPGA_family_or_part_number>" -o test-fpga <source_files>`).

• The HLS compiler creates a .prj directory (for example, `test-fpga.prj`) in the current working directory.

• The console displays the output of the executable to signify a successful execution.
3 Troubleshooting the Setup of the Intel HLS Compiler

This section provides information that can help you troubleshoot problems you might encounter when setting up the HLS compiler.

Intel HLS Compiler Licensing Issues on page 11

3.1 Intel HLS Compiler Licensing Issues

The Intel High Level Synthesis (HLS) Compiler is licensed as part of your Intel Quartus Prime license. However, the Intel HLS Compiler depends on ModelSim software. In some cases, you might encounter problems with the licensing for this software.

Intel HLS Compiler Licensing Error Messages on page 11
LM_LICENSE_FILE Environment Variable on page 11

3.1.1 Intel HLS Compiler Licensing Error Messages

The HLS compiler issues error messages if it cannot locate the license for the installed version of ModelSim software.

If the HLS compiler fails to locate the ModelSim software license, it issues the following error message when you compile your design to the FPGA architecture:

```
$ i++ -march="<FPGA_family_or_part_number>" --component dut program.cpp
HLS Elaborate cosim testbench. FAILED.
See ./a.prj/a.log for details.
Error: Missing simulator license. Either:
1) Ensure you have a valid ModelSim license
2) Use the --simulator none flag to skip the verification flow
```

Common causes for these errors include:

- Missing, expired, or invalid licenses
- Incorrect license server name in the license.dat file
- Unspecified or incorrectly-specified license location

Note: The running speed of the HLS compiler might decrease if the compiler has to search the network for missing or corrupted licenses. If this problem occurs, correct the license file or license location accordingly.

3.1.2 LM_LICENSE_FILE Environment Variable

Intel and third-party software use the LM_LICENSE_FILE environment variable to specify the locations of license files or license servers. For example, both the Intel Quartus Prime software and the ModelSim software use the LM_LICENSE_FILE variable to specify the locations of their licenses.
Note: The time it takes for your development machine to communicate with the license server directly affects compilation time. If your LM_LICENSE_FILE environment variable setting includes paths to many license servers, or if the license server is hosted in a distant locale, you will notice a significant increase in compilation time.

On Linux or UNIX systems, insert a colon (:) after each license file or license server location that you append to the LM_LICENSE_FILE environment variable.

On Windows systems, insert a semicolon (;) after each license file or license server location that you append to the LM_LICENSE_FILE environment variable.

Note: When modifying the LM_LICENSE_FILE setting to include the locations of your software licenses, do not remove any existing license locations appended to the variable.

3.1.2.1 ModelSim Software License-Specific Considerations

When setting up the ModelSim software license, you need to append the license location to the LM_LICENSE_FILE environment variable. However, you can also append the location of the ModelSim software license to the MGLS_LICENSE_FILE environment variable.

For Mentor Graphics applications, including the ModelSim software, you can specify the paths to license files and license servers in five different locations. If you specify paths to license files or license servers in multiple locations, the following search order is used to find the first valid path:

- MGLS_LICENSE_FILE environment variable you set in the user environment
- MGLS_LICENSE_FILE environment variable you set in the registry
- LM_LICENSE_FILE environment variable you set in the environment
- LM_LICENSE_FILE environment variable you set in the registry
- <path to FLEXlm>\license.dat, where <path to FLEXlm> is the default location of the FLEXlm license file.

When you install a Mentor Graphics product license on a computer, the MGLS_LICENSE_FILE environment variable settings take precedence over the LM_LICENSE_FILE environment variable settings. If you set both environment variables, set LM_LICENSE_FILE to point to the ModelSim license server and set MGLS_LICENSE_FILE to only point to the license server for other Mentor Graphics applications. If you only use the MGLS_LICENSE_FILE environment variable, ensure that the ModelSim license server and the license servers for other Mentor Graphics applications are on the same machine.
### A Document Revision History

#### Table 3. Revision History of the Intel High Level Synthesis Compiler Getting Started Guide

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| November 2017 | 2017.11.06 | • The Intel High Level Synthesis (HLS) Compiler is now part of Intel Quartus Prime Design Suite, resulting in the following changes:  
  — Revised to document to reflect that you now get the Intel HLS Compiler by installing Intel Quartus Prime software.  
  — Removed most licensing information. Licensing the Intel HLS Compiler is now covered by your Intel Quartus Prime Design Suite licensing. Some third-party software required by the HLS compiler might continue to require additional licensing.  
  — Removed information about overriding compilers.  
  — Revised prerequisites to reflect only additional prerequisites required by the HLS compiler.  
  — Revised path information to reflect the new file system locations of the Intel HLS Compiler files.  
  • Renamed the following tutorials:  
    — The explicit_streams tutorial is now called explicit_streams_buffer.  
    — The explicit_streams_2 tutorial is now called explicit_streams_packets_ready_valid. |
| June 2017    | 2017.06.23 | • Minor changes and corrections.                                                                                                                                                                           |
| June 2017    | 2017.06.09 | • Updated High Level Synthesis (HLS) Design Examples and Tutorials on page 6 with information about new examples.  
  • Revised Overriding the Default GCC Compiler for Intel HLS Compiler.                                                                                                 |
| March 2017   | 2017.03.14 | • Removed bit operations (3DES) from list of supplied design examples.                                                                                                                                 |
| March 2017   | 2017.03.01 | • Added installation of required packages and libraries needed for Linux                                                                                                                                    |
| February 2017| 2017.02.03 | • Changed success message in Quick Start sections to PASSED.  
  • Added HLS Design Examples and Tutorials section.  
  • Moved Running an HLS Design Example on Linux and Running an HLS Design Example on Windows to HLS Design Examples and Tutorials. |
| November 2016| 2016.11.30 | • In HLS Compiler Prerequisites, updated software requirements to note that the HLS compiler supports all ModelSim software editions that the Intel Quartus Prime software supports.  
  • In HLS Compiler Quick Start, added a note that you must run the init_hls script each time you start a shell or terminal to develop your design.  
  • In HLS Compiler Quick Start, separated the Linux and Windows instructions.  
  • In Running an HLS Design Example, separated the Linux and Windows instructions.  
  For Linux, run the make command; for Windows, run the build.bat command.  
  • Changed the test_x86-64 command option to test-x86-64. |

*Other names and brands may be claimed as the property of others.*
<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| September 2016 | 2016.09.12 | • Changed the `test_fpga` command option to `test-fpga`.
• Removed the instruction to run the `make test_qii` command for Linux and the `build.bat test_qii` command for Windows because it is no longer necessary.
• In *HLS Licensing Error Messages*, updated the error message you will see if the HLS compiler fails to locate the ModelSim software license. |
|              |         | Initial release.                                                                                                                                                     |