10. Hot Socketing and Power-On Reset in Stratix III Devices

SIII51010-1.7

This chapter describes information about hot-socketing specifications, power-on reset (POR) requirements, and their implementation in Stratix® III devices.

Stratix III devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a Stratix III device or a board in a system during system operation without causing undesirable effects to the running system bus or board that is inserted into the system.

The hot socketing feature also removes some of the difficulty when you use Stratix III devices on PCBs that contain a mixture of 3.3-, 3.0-, 2.5-, 1.8-, 1.5-, and 1.2-V devices. With the Stratix III hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Stratix III hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- I/O buffers non-intrusive to system buses during hot insertion

This section also describes the POR circuitry in Stratix III devices. POR circuitry keeps the devices in the reset state until the power supplies are within operating range.

Stratix III Hot-Socketing Specifications

Stratix III devices are hot-socketing compliant without the need for external components or special design requirements. Hot socketing support in Stratix III devices has the following advantages:

- You can drive the device before power-up without damaging it.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby not affecting other buses in operation.
- You can insert a Stratix III device into or remove it from a powered-up system board without damaging or interfering with normal system/board operation.

Stratix III Devices Can Be Driven Before Power Up

You can drive signals into I/O pins, dedicated input pins, and dedicated clock pins of Stratix III devices before or during power up or power down without damaging the device. Stratix III devices support power up or power down of the power supplies in any sequence in order to simplify system-level design.

I/O Pins Remain Tri-Stated During Power Up

A device that does not support hot socketing can interrupt system operation or cause contention by driving out before or during power up. In a hot-socketing situation, the Stratix III device's output buffers are turned off during system power up or power down. Also, the Stratix III device does not drive out until the device is configured and working within recommended operating conditions.

Insertion or Removal of a Stratix III Device from a Powered-Up System

Devices that do not support hot socketing can short power supplies when powered up through the device signal pins. This irregular power up can damage both the driving and driven devices and can disrupt card power up.

You can insert a Stratix III device into or remove it from a powered-up system board without damaging the system board or interfering with its operation.

You can power up or power down the core voltage supplies (V_{CC}, V_{CCL}, V_{CCPT}, V_{CCA_PLL}, and V_{CCD_PLL}), V_{CCIO}, V_{CCPMG}, V_{CC_CLKIN}, and V_{CCPD} supplies in any sequence and at any time between them. The individual power supply ramp-up and ramp-down rates can range from 50 µs to 12 ms or 100 ms depending on the PORSEL setting. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

For more information about the hot socketing specification, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter and the *Hot-Socketing and Power-Sequencing Feature and Testing for Altera Devices White Paper*.

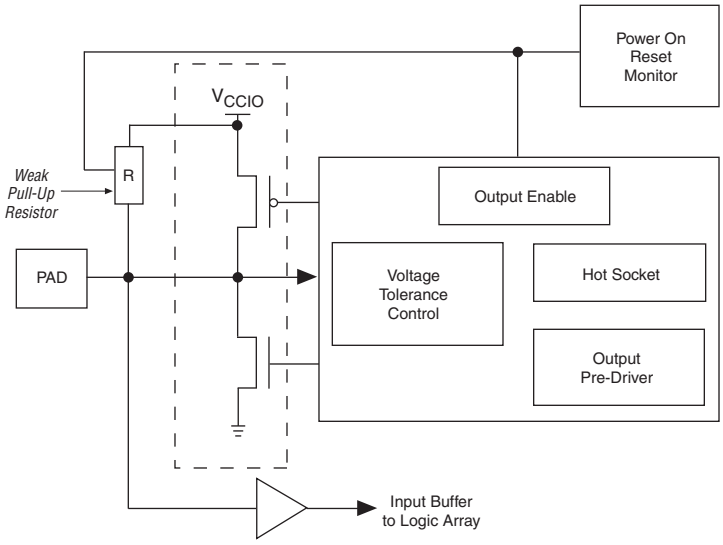
A possible concern regarding hot socketing is the potential for "latch-up". Nevertheless, Stratix III devices are immune to latch-up when hot socketing. Latch-up can occur when electrical subsystems are hot socketed into an active system. During hot socketing, the signal pins can be connected and driven by the active system before the power supply can provide current to the device's power and ground planes. This condition can lead to latch-up and cause a low-impedance path from power to ground within the device. As a result, the device draws a large amount of current, possibly causing electrical damage.

Hot-Socketing Feature Implementation in Stratix III Devices

The hot-socketing feature turns off the output buffer during power up and power down of the V_{CC}, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies. The hot-socketing circuitry generates an internal `HOTSCKT` signal when the V_{CC}, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies are below the threshold voltage. Hot-socketing circuitry is designed to prevent excess I/O leakage during power up. When the voltage ramps up very slowly, it is still relatively low, even after the POR signal is released and the configuration is completed. The `CONF_DONE`, `nCEO`, and `nSTATUS` pins fail to respond, as the output buffer cannot flip from the state set by the hot-socketing circuit at this low voltage. Therefore, the hot-socketing circuit has been removed on these configuration pins to make sure that they are able to operate during configuration. Thus, it is expected behavior for these pins to drive out during power-up and power-down sequences.

Figure 10–1 shows the Stratix III device's I/O pin circuitry.

Figure 10–1. Hot-Socketing Circuitry for Stratix III Devices

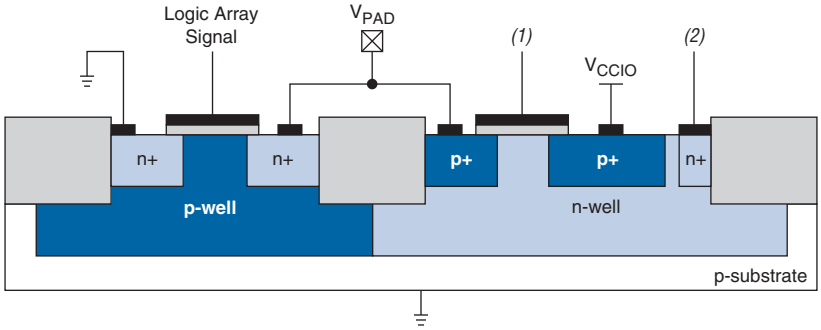


The POR circuit monitors the voltage level of power supplies (V_{CC}, V_{CCL}, V_{CCPD}, V_{CCPGM} and V_{CCPT}) and keeps the I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) in the Stratix III input/output element (IOE) keeps the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO}, V_{CC}, V_{CCPD}, and/or V_{CCPGM} supplies are powered, and it prevents the I/O pins from driving out when the device is not in user mode.

Altera uses GND as reference for hot-socketing operation and I/O buffer designs. To ensure proper operation, you must connect the GND between boards before connecting the power supplies. This will prevent the GND on your board from being pulled up inadvertently by a path to power through other components on your board. A pulled up GND could otherwise cause an out-of-specification I/O voltage or current condition with the Altera device.

Figure 10–2 shows a transistor-level cross section of the Stratix III device I/O buffers. This design prevents leakage current from I/O pins to the V_{CCIO} supply when V_{CCIO} is powered before the other voltage supplies or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

Figure 10–2. Transistor Level Diagram of a Stratix III Device I/O Buffers



Notes to Figure 10–2:

(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.
(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

Power-On Reset Circuitry

When power is applied to a Stratix III device, a POR event occurs when all the power supplies reach the recommended operating range within a certain period of time (specified as a maximum power supply ramp time; t_{RAMP}). Hot socketing feature in Stratix III allows the required power supplies to be powered up in any sequence and at any time between them with each individual power supply must reach the recommended operating range within t_{RAMP}.

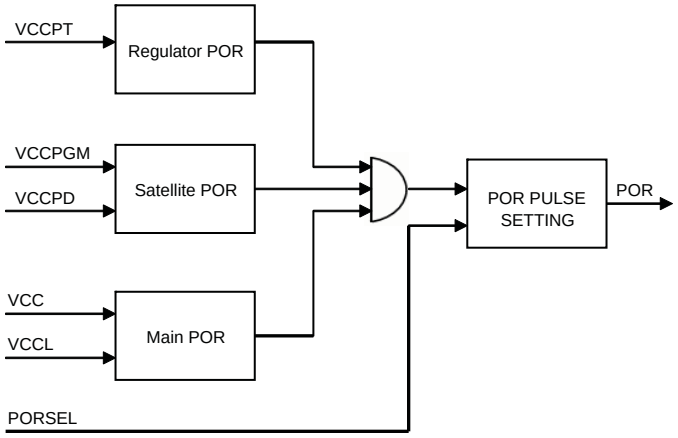
For maximum power supplies ramp-up time for Stratix III Devices, refer Table 10–1.

Stratix III devices provide a dedicated input pin (PORSEL) to select a POR delay time during power up. When the PORSEL pin is connected to ground, the POR delay time is 100 ms. When the PORSEL pin is set to high, the POR delay time is 12 ms.

The POR block consists of a regulator POR, satellite POR, and main POR to check the power supply levels for proper device configuration. The satellite POR monitors V_{CCPD} and V_{CCPGM} power supplies that are used in the configuration buffers for device programming. The POR block also checks for functionality of I/O level shifters powered by V_{CCPD} and V_{CCPGM} during power-up mode. The main POR checks the V_{CC} and V_{CCL} supplies used in core. The internal configuration memory supply, which is used during device configuration, is checked by the regulator POR block and is gated in the main POR block for the final POR trip. A simplified block diagram of the POR block is shown in Figure 10–3.

All configuration-related dedicated and dual function I/O pins must be powered by V_{CCPGM}.

Figure 10–3. Simplified POR Block Diagram



The ramp-up time specification for Stratix III devices is listed in Table 10–1.

Table 10–1. Power Supplies Ramp-Up Time (t_{RAMP}) Requirements

Power Supply	PORSEL setting	Ramp-up Time	
		Minimum	Maximum
V_{CCPT}	HIGH	50 µs	5 ms
	GND	50 µs	5 ms
V_{CC}, V_{CCL}, V_{CCPD}, V_{CCPGM}, V_{CCIO}, V_{CCA_PLL}, V_{CCD_PLL}, V_{CC_CLKIN}	HIGH	50 µs	12 ms
	GND	50 µs	100 ms

Power-On Reset Specifications

The POR circuit monitors the power supplies listed in Table 10–2.

Table 10–2. Power Supplies Monitored by the POR Circuitry

Power Supply	Description	Setting (V)
V_{CC}	I/O registers power supply	1.1
V_{CCL}	Selectable core voltage power supply	0.9, 1.1
V_{CCPT}	Power supply for the programmable power technology	2.5
V_{CCPD}	I/O pre-driver power supply	2.5, 3.0, 3.3
V_{CCPGM}	Configuration pins power supply	1.8, 2.5, 3.0, 3.3

To ensure proper device operation, all power supplies listed in Table 10–2 are required to be powered up at all times during device operation.

The POR circuit does not monitor the power supplies listed in Table 10–3.

Table 10–3. Power Supplies That Are Not Monitored by the POR Circuitry

Voltage Supply	Description	Setting (V)
V_{CCIO}	I/O power supply	1.2, 1.5, 1.8, 2.5, 3.0, 3.3
V_{CCA_PLL}	PLL analog global power supply	2.5
V_{CCD_PLL}	PLL digital power supply	1.1
V_{CC_CLKIN}	PLL differential clock input power supply (top and bottom I/O banks only)	2.5
V_{CCBAT}	Battery back-up power supply for design security volatile key storage	1.0 – 3.3 *(1)*

Note to Table 10–3:

(1) The nominal voltage for V_{CCBAT} is 3.0-V.

During power up, all power supplies listed in Table 10–2 and Table 10–3 are required to monotonically reach their full-rail values within t_{RAMP}.

The POR specification is designed to ensure that all the circuits in the Stratix III device are at certain known states during power up.

The POR signal pulse width is programmable using the PORSEL input pin. When PORSEL is set to low, the POR signal pulse width is set to 100 ms. A POR pulse width of 100 ms allows serial flash devices with 65 ms to 100 ms internal POR delay to be powered up and ready to receive the nSTATUS signal from Stratix III. When the PORSEL is set to high, the POR signal pulse width is set to 12 ms. A POR pulse width of 12 ms allows time for power supplies to ramp-up to full rail.

For more information about the POR specification, refer to the *DC and Switching Characteristics* chapter.

Chapter Revision History

Table 10–4 lists the revision history for this chapter.

Table 10–4. Chapter Revision History

Date	Version	Changes Made
March 2010	1.7	■ Updated for the Quartus II software version 9.1 SP2 release. ■ Minor text edits.
February 2009	1.6	■ Updated "Hot Socketing Feature Implementation in Stratix III Devices" section. ■ Removed "Referenced Documents" section.
October 2008	1.5	■ Updated Table 10–3. ■ Updated "Insertion or Removal of a Stratix III Device from a Powered-Up System" and "Power-On Reset Circuitry" sections. ■ Updated Figure 10–3. ■ Added Table 10–1. ■ Updated New Document Format.
July 2008	1.4	Updated Table 10–2.
May 2008	1.3	■ Updated "Insertion or Removal of a Stratix III Device from a Powered-Up System", "Hot Socketing Feature Implementation in Stratix III Devices", and "Power-On Reset Circuitry" sections. ■ Updated "Power-On Reset Specifications" section tables.
October 2007	1.2	■ Added section "Referenced Documents". ■ Added live links for references.
May 2007	1.1	All instances of VCCR changed to VCCPT in text, and in Figure 10–3, and Table 10–1.
November 2006	1.0	Initial Release.