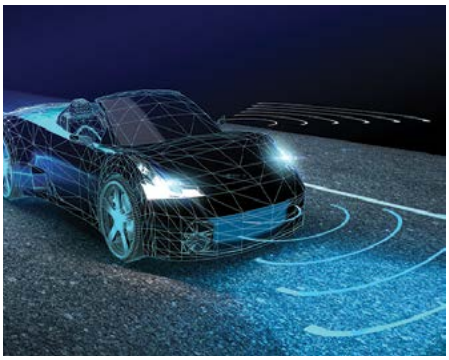
PRODUCT BRIEF

Intel® Arria® 10 GX FPGA: Automotive Grade



Intel's automotive-grade Arria® 10 GX FPGAs deliver over 60% higher performance at up to 40% lower power than prior-generation midrange FPGAs†, and include variable-precision digital signal processing (DSP) support with hardened floating point. Intel's Arria 10 GX FPGAs are the ideal companion to accelerate Intel's high-performance CPUs for autonomous driving applications, such as increasing throughput or reducing latency for machine learning based object classifications, sensor data aggregation and fusion, and many others.

DSP Flexibility for Machine Learning

- **Support for multiple precision types** – the three modes available for Arria 10 GX DSP blocks: standard-precision fixed point, high-precision fixed point, and single-precision floating point allow a flexible implementation of algorithms requirements
- **Architectural innovation** – designers can implement algorithms in floating point with similar performance as fixed point without compromising power, area, or logic density
- **High performance** – industry-first implementation of IEEE 754 single-precision hardened floating point DSP on FPGA enabling developers to design to the strictest requirements

Performance and Power

- **Energy-efficient floating-point calculations** – 25 GFLOPS/watt, reducing the overall system power envelope while maintaining high performance for workload acceleration
- **Programmable Power Technology** – reducing device power in lower performance circuits while delivering the highest performance where needed
- **Tailored performance** – enabling efficient processing of large data sets through building processing architectures that are customized for the application

Synergy with Intel CPUs

- **Packaged solutions for autonomous driving** – common intellectual property (IP) cores and joint development platforms for maximum synergy with Intel® CPUs and FPGAs now available
- **High-level design flow** – OpenCL™ support enables software engineers to easily access the high performance offered by Intel FPGAs

Product Table

PRODUCT LINE		GX 160	GX 220	GX 270	GX 320	GX 480	GX 570	GX 660
Resources	Part number reference	10AX016	10AX022	10AX027	10AX032	10AX048	10AX057	10AX066
	Logic elements (K)	160	220	270	320	480	570	660
	M20K blocks	440	588	750	891	1,438	1,800	2,131
	M20K memory (Mb)	9	11	15	17	28	35	42
	MLAB counts	1,680	2,932	3,922	4,582	7,046	8,153	9,260
	MLAB memory (Mb)	1	1.8	2.4	2.8	4.3	5	5.7
	18x19 multipliers	312	382	1,660	1,970	2,736	3,046	3,376
Maximum I/O Pins, and Architectural Features	Max I/Os	288	288	384	384	492	492	492
	Max transceivers	12	12	24	24	24	24	24
	fPLLs	6	6	8	8	12	16	16
	I/O PLLs	6	6	8	8	12	16	16
	PCI Express* hardened IP blocks (x8)	1	1	2	2	2	2	2
Package Options[1] and I/O Pins[2]: General-Purpose I/O Count, High-Voltage I/O Count, LVDS Pairs[3], and Transceiver Count								
U19	U484 pin (19 mm)	192, 48, 72, 6	192, 48, 72, 6					
F29	F780 pin (29 mm)	288, 48, 120, 12	288, 48, 120, 12	360, 48, 156, 12	360, 48, 156, 12	360, 48, 156, 12		
F34	F1152 pin (35 mm)			384, 48, 168, 24	384, 48, 168, 24	492, 48, 222, 24	492, 48, 222, 24	492, 48, 222, 24

Notes:
1. All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.
2. A subset of pins for each package are used for 3.3 V and 2.5 V interfaces.
3. Each LVDS pair can be configured as either a differential input or a differential output.

192, 48, 72, 6 Numbers indicate GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

Indicates pin migration.

Package information is preliminary and subject to change.

For more information, visit www.altera.com/automotive