Simplifying Your Wireless Infrastructure Product Life Cycle

Wireless End Market Solutions from Altera

With a programmable logic device (PLD) in your wireless design, you can easily accommodate a fast development cycle, as well as power, board space, and cost constraints. Flexible and future-proof, a single PLD solution can simply do all of the heavy lifting that would otherwise require several digital signal processing (DSP) devices.

Altera offers a portfolio of programmable wireless solutions, many with integrated transceivers, that help you design your wireless infrastructure applications with agility and for volume right from the beginning. The portfolio includes an exclusive combination of:

- High-performance, low-power, scalable silicon
- Low-latency intellectual property (IP)
- Productivity-enhancing tools, including development boards

The Altera Programmable Device Portfolio

Device	Benefits
Stratix® FPGA series	High performance, high density, low power consumption, high memory bandwidth, signal integrity, DSP circuitry, integrated transceivers
Arria® II FPGA series	Cost-optimized, lowest power FPGAs with transceivers up to 6.375 Gbps
Cyclone® FPGA series	Low cost, with dedicated DSP circuitry, integrated transceivers
MAX® CPLD series	Low cost, low power, instant-on and non-volatile single chip solution
HardCopy® ASIC series	High performance and low power with seamless, risk-free migration from FPGAs to structured ASICs, integrated transceivers

Design for Volume and with Agility

With our Stratix V FPGAs, you get the highest bandwidth and unprecedented levels of integration that enable a roadmap to single-chip baseband and RF solutions. You can prototype your design on Stratix V FPGAs, and then migrate it to HardCopy V ASICs for the lowest-cost-per-channel design. Both come with integrated transceiver variants.

Providing power and cost savings without sacrificing performance, along with a low-cost integrated transceiver option, the Cyclone IV FPGA family is ideal for low-cost, small form factor wireless applications. With the Arria II FPGA series, you get the processing bandwidth, 6.375-Gbps transceivers with predictable latency, low power, and flexibility for emerging wireless infrastructure designs.

A wide variety of IP and reference designs, software development tools, and development boards from Altera and our wireless ecosystem partners will help you design with agility. The IP and reference designs cover a wide variety of wireless standards, including WiMAX, Long-Term Evolution (LTE), and W-CDMA. They are also highly optimized for Altera® silicon. With these resources, you can focus on solution differentiation.

Where Altera Can Help

Application	IP	Reference Designs	
WiMAX channel card	• Fast Fourier transform (FFT)/inverse FFT (IFFT) • Reed-Solomon • Viterbi • Turbo cores • Low-density parity check (LDPC) cores	• Scalable orthogonal frequency division multiplexing access (OFDMA) engine • Ranging • Channel estimation • Channel equalization • Symbol mapper/demapper	
LTE channel card	• 3GPP Turbo encoder • 3GPP Turbo decoder	• Discrete Fourier transform (DFT)/ inverse DFT (IDFT) • 1536 FFT/IFFT • Symbol demapper (SDM) • Descrambler • Rate de-matching (RDM) • Transport block CRC • PUSCH uplink bit rate chain	• 24K FFT for RACH detection • FFT/IFFT compiler • 2x2 MMSE MIMO equalisation • Channel estimation • Zadoff-Chu sequence generation • Uplink symbol rate chain • Crest factor reduction • Matrix decomposition
Digital radio	• Finite impulse response (FIR) compiler • Numerically controlled oscillator (NCO) compiler • Open Base Station Architecture Initiative (OBSAI) RP3-01 • Common Public Radio Interface (CPRI) • JESD204A	• Digital predistortion • Crest factor reduction • Digital upconverter • Digital downconverter	

Customers Often Ask Us...

How can an FPGA improve system performance?

Systems architected with FPGA coprocessors can offload a DSP processor, efficiently executing the computationally intensive blocks of DSP algorithms to boost system-level performance. Altera offers an industry-leading software development flow that allows designers to quickly create coprocessor designs and integrate them into the overall system.

Why would an FPGA be more advantageous than an ASIC, with its lower power and costs?

Flexibility is a key requirement in the constantly evolving wireless infrastructure landscape. ASIC design, with its high NRE costs and long lead times, is difficult to justify in this scenario. By using Altera FPGAs, you can choose to have flexibility in the initial stages of your product life cycle, followed by a risk-free migration to low-cost, low-power, and high-performance HardCopy ASIC technology during the mature, higher-volume phase of the product life cycle.

Want to Dig Deeper?

Visit us at **www.altera.com/wireless** and find pages with the following information:

- WiMAX basestation solutions
- LTE basestation solutions
- Enabling wireless technologies
- 3G infrastructure solutions
- Wireless reference designs

Want to Know More?

If you've got wireless system design questions or ideas to share, please contact your local Altera FAE or sales representative, visit **www.altera.com/wireless**, or send us an email at **wireless@altera.com**.

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