

# Cyclone IV Product Table

Resources	Product Line	Cyclone IV GX FPGAs <sup>1</sup>						Cyclone IV E FPGAs <sup>1</sup>										
		EP4CGX15	EP4CGX22	EEP4CGX30	EP4CGX50	EP4CGX75	EP4CGX110	EP4CGX150	EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40	EP4CE55	EP4CE75	EP4CE115	
LEs (K)		14	21	29	50	74	109	150	6	10	15	22	29	40	56	75	114	
M9K memory blocks		60	84	120	278	462	666	720	30	46	56	66	66	126	260	305	432	
Embedded memory (Kb)		540	756	1,080	2,502	4,158	5,490	6,480	270	414	504	594	594	1,134	2,340	2,745	3,888	
18 x 18 multipliers		0	40	80	140	198	280	360	15	23	56	66	66	116	154	200	266	
Global clock networks		20	20	20	30	30	30	30	10	10	20	20	20	20	20	20	20	
PLLs		3	4	4	8	8	8	8	2	2	4	4	4	4	4	4	4	
Clocks, Maximum I/O Pins, and Architectural Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3																
	I/O standards supported	LVTTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12																
	Emulated LVDS channels	9	40	40	73	73	139	139	66	66	137	52	224	160	178	230		
	LVDS channels, 840 Mbps (receive/transmit)	7/7	14/14	14/14	49/49	49/49	59/59	59/59	-	-	-	-	-	-	-	-	-	-
	Transceiver count <sup>2</sup> (2.5 Gbps/3.124 Gbps)	2/0	2, 0 / 4, 0	4, 0 / 0, 4 <sup>3</sup>	0, 8	0, 8	0, 8	0, 8	-	-	-	-	-	-	-	-	-	-
	PCIe hardened IP blocks (Base specification, Rev 1.1, 2.0, and so on)	1	1	1	1	1	1	1	-	-	-	-	-	-	-	-	-	-
	Memory devices supported	DDR2, DDR, SDR																
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count																		
E144 pin <sup>4</sup> (22 mm, 0.5 mm pitch)	-	-	-	-	-	-	-	-	91	91	81	79	-	-	-	-	-	
M164 pin (8 mm, 0.5 mm pitch)	-	-	-	-	-	-	-	-	-	-	74	-	-	-	-	-	-	
U256 pin (14 mm, 0.8 mm pitch)	-	-	-	-	-	-	-	-	179	179	165	153	-	-	-	-	-	
U484 pin (19 mm, 0.8 mm pitch)	-	-	-	-	-	-	-	-	-	-	-	-	-	328	324	292	-	
F169 pin (14 mm, 1.0 mm pitch)	72	72	72	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
	2	2	2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
F256 pin (17 mm, 1.0 mm pitch)	-	-	-	-	-	-	-	-	179	179	165	153	-	-	-	-	-	
F324 pin (19 mm, 1.0 mm pitch)	-	150	150	-	-	-	-	-	-	-	-	-	193	193	-	-	-	
	-	4	4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
F484 pin (23 mm, 1.0 mm pitch)	-	-	290	290	290	270	270	-	-	343	-	328	328	324	292	280	-	
	-	-	4	4	4	4	4	-	-	-	-	-	-	-	-	-	-	
F672 pin (27 mm, 1.0 mm pitch)	-	-	-	310	310	393	393	-	-	-	-	-	-	-	-	-	-	
	-	-	-	8	8	8	8	-	-	-	-	-	-	-	-	-	-	
F780 pin (29 mm, 1.0 mm pitch)	-	-	-	-	-	-	-	-	-	-	-	-	532	532	374	426	528	
F896 pin (31 mm, 1.0 mm pitch)	-	-	-	-	-	475	475	-	-	-	-	-	-	-	-	-	-	
	-	-	-	-	-	8	8	-	-	-	-	-	-	-	-	-	-	

Notes:

- All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit [www.altera.com](http://www.altera.com).
- Transceiver performance varies by product line and package offering.
- EP4CGX30 supports 3.125 Gbps transceivers only in F484 package option.
- Enhanced thin quad flat pack (EQFP).

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Values on top indicate available user I/O pins; values at the bottom indicate the 2.5 Gbps or 3.125 Gbps transceiver count.

Pin migration (same Vcc, GND, ISP, and input pins). User I/Os may be less than labelled for pin migration.