Stratix® 10

INTEL® STRATIX® 10 PRODUCT TABLE

	PRODUCT LINE	GX 400 SX 400	GX 650 SX 650	GX 850 SX 850	GX 1100 SX 1100	GX 1650 SX 1650	GX 2100 SX 2100	GX 2500 SX 2500	GX 2800 SX 2800	GX 4500 SX 4500	GX 5500 SX 5500
Resources	Logic elements (LEs)[1]	378,000	612,000	841,000	1,092,000	1,624,000	2,005,000	2,422,000	2,753,000	4,463,000	5,510,000
	Adaptive logic modules (ALMs)	128,160	207,360	284,960	370,080	550,540	679,680	821,150	933,120	1,512,820	1,867,680
	ALM registers	512,640	829,440	1,139,840	1,480,320	2,202,160	2,718,720	3,284,600	3,732,480	6,051,280	7,470,720
	Hyper-Registers from Intel® HyperFlex™ FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric									
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees									
	M20K memory blocks	1,537	2,489	3,477	4,401	5,851	6,501	9,963	11,721	7,033	7,033
	M20K memory size (Mb)	30	49	68	86	114	127	195	229	137	137
	MLAB memory size (Mb)	2	3	4	6	8	11	13	15	23	29
	Variable-precision digital signal processing (DSP) blocks	648	1,152	2,016	2,520	3,145	3,744	5,011	5,760	1,980	1,980
	18 x 19 multipliers	1,296	2,304	4,032	5,040	6,290	7,488	10,022	11,520	3,960	3,960
	Peak fixed-point performance (TMACS)[2]	2.6	4.6	8.1	10.1	12.6	15.0	20.0	23.0	7.9	7.9
	Peak floating-point performance (TFLOPS)[3]	1.0	1.8	3.2	4.0	5.0	6.0	8.0	9.2	3.2	3.2
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection									
	Hard processor system[4]	Quad-core 64 bit ARM* Cortex*-A53 up to 1.5 GHz with 32 KB I/D cache, NEON* coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I²C x5, general-purpose timers x7, watchdog timer x4									
	Maximum user I/O pins	392	400	736	736	704	704	1160	1160	1640	1640
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	192	192	360	360	336	336	576	576	816	816
	Total full duplex transceiver count	24	48	48	48	96	96	96	96	24	24
	GXT full duplex transceiver count (up to 30 Gbps)	16	32	32	32	64	64	64	64	16	16
	GX full duplex transceiver count (up to 17.4 Gbps)	8	16	16	16	32	32	32	32	8	8
	PCI Express* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)	1	2	2	2	4	4	4	4	1	1
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys									
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count[5]											
F1152 pin (35 mm x 35 mm, 1.0 mm pitch)		392,8,192,24	392,8,192,24	–	–	–	–	–	–	–	–
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)		–	400,16,192,48	–	–	–	–	–	–	–	–
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)		–	–	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	–	–
F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch)		–	–	736,16,360,48	736,16,360,48	–	–	–	–	–	–
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)		–	–	–	–	704,32,336,96	704,32,336,96	704,32,336,96	704,32,336,96	–	–
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	–	–	–	–	–	1160,8,576,24	1160,8,576,24	1640,8,816,24	1640,8,816,24

Notes:
1. LE counts valid in comparing across Intel FPGA devices, and are conservative vs. competing FPGAs.
2. Fixed-point performance assumes the use of pre-adder.
3. Floating-point performance is IEEE 754 compliant single precision.
4. Quad-core ARM Cortex-A53 hard processor system only available in Stratix 10 SX SoCs.
5. A subset of pins for each package are used for high-voltage, 3.0 V and 2.5 V interfaces.
6. All data is preliminary, and may be subject to change without prior notice.

392,8,192,24 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

Indicates pin migration path.

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PRODUCT LINE	SX 400	SX 650	SX 850	SX 1100	SX 1650	SX 2100	SX 2500	SX 2800	SX 4500	SX 5500
Processor	Quad-core 64 bit ARM Cortex-A53 MPCore* processor									
Maximum processor frequency	1.5 GHz[1]									
Processor cache and co-processors	• L1 instruction cache (32 KB) • L1 data cache (32 KB) with error correction code (ECC) • Level 2 cache (1 MB) with ECC • Floating-point unit (FPU) single and double precision • ARM NEON media engine • ARM CoreSight* debug and trace technology • System Memory Management Unit (SMMU) • Cache Coherency Unit (CCU)									
Scratch pad RAM	256 KB									
HPS DDR memory	DDR4, DDR3, and LP DDR3 (Up to 64 bit with ECC)									
Direct memory access (DMA) controller	8 channels									
EMAC	3X 10/100/1000 Ethernet media access controller (EMAC) with integrated DMA									
USB on-the-go (OTG) controller	2X USB OTG with integrated DMA									
UART controller	2X UART 16550 compatible									
Serial peripheral interface (SPI) controller	4X SPI									
I^2C controller	5X I^2C									
Quad SPI flash controller	1X SIO, DIO, QIO SPI flash supported									
SD/SDIO/MMC controller	1X eMMC 4.5 with DMA and CE-ATA support									
NAND flash controller	• 1X ONFI 1.0 or later • 8 and 16 bit support									
General-purpose timers	4X									
Software-programmable general-purpose I/Os (GPIOs)	Maximum 48 GPIOs									
HPS DDR Shared I/O	3X 48 - May be assigned to HPS for HPS DDR access									
Direct I/Os	48 I/Os to connect HPS peripherals directly to I/O									
Watchdog timers	4X									
Security	Secure device manager, Advanced Encryption Standard (AES) AES-256/SHA-256 bitsream encryption/authentication, PUF, ECDSA 256/384 boot code authentication, side channel attack protection									

Notes:
1. With overdrive feature.

Gen-1023-1.5