



INTEL® STRATIX® 10 TX PRODUCT TABLE

| PRODUCT LINE | | TX 1650 | | TX 2100 | | TX 2500 | | | TX 2800 | | | | | | | | | | | | |
|---|--|---|--|--------------------|--|--------------------|--|--------------------|------------------|--------------------|------------------|--------------------|--|---------------------|--|--------------------|--|--------------------|--|---------------------|--|
| Resources | Logic elements (LEs) ¹ | 1,679,000 | | 2,073,000 | | 2,422,000 | | | 2,753,000 | | | | | | | | | | | | |
| | Adaptive logic modules (ALMs) | 569,200 | | 702,720 | | 821,150 | | | 933,120 | | | | | | | | | | | | |
| | ALM registers | 2,276,800 | | 2,810,880 | | 3,284,600 | | | 3,732,480 | | | | | | | | | | | | |
| | Hyper-Registers from Intel® Hyperflex™ FPGA architecture | Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric | | | | | | | | | | | | | | | | | | | |
| | Programmable clock trees synthesizable | Hundreds of synthesizable clock trees | | | | | | | | | | | | | | | | | | | |
| | eSRAM memory blocks | 2 | | 2 | | - | | | - | | | | | | | | | | | | |
| | eSRAM memory size (Mb) | 90 | | 90 | | - | | | - | | | | | | | | | | | | |
| | M20K memory blocks | 6,162 | | 6,847 | | 9,963 | | | 11,721 | | | | | | | | | | | | |
| | M20K memory size (Mb) | 120 | | 134 | | 195 | | | 229 | | | | | | | | | | | | |
| | MLAB memory size (Mb) | 9 | | 11 | | 13 | | | 15 | | | | | | | | | | | | |
| | Variable-precision digital signal processing (DSP) blocks | 3,326 | | 3,960 | | 5,011 | | | 5,760 | | | | | | | | | | | | |
| | 18 x 19 multipliers | 6,652 | | 7,920 | | 10,022 | | | 11,520 | | | | | | | | | | | | |
| | Peak fixed-point performance (TMACS) ² | 13.3 | | 15.8 | | 20.0 | | | 23.0 | | | | | | | | | | | | |
| | Peak floating-point performance (TFLOPS) ³ | 5.3 | | 6.3 | | 8.0 | | | 9.2 | | | | | | | | | | | | |
| I/O and Architectural Features | Secure device manager | AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection | | | | | | | | | | | | | | | | | | | |
| | Hard processor system | Quad-core 64-bit ARM® Cortex®-A53 up to 1.5 GHz with 32KB I/D cache, NEON® coprocessor, 1 MB L2 Cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I ² C x5, general purpose timers x7, watchdog timer x4 | | | | | | | | | | | | | | | | | | | |
| | Maximum user I/O pins | 544 | | 440 | | 544 | | 440 | | 296 | | 544 | | 440 | | 296 | | | | | |
| | Maximum LVDS pairs 1.6 Gbps (RX or TX) | 264 | | 216 | | 264 | | 216 | | 144 | | 264 | | 216 | | 144 | | | | | |
| | Total full duplex transceiver count | 72 | | 96 | | 72 | | 96 | | 144 | | 72 | | 96 | | 144 | | | | | |
| | GXE transceiver count - PAM-4 (up to 58 Gbps) or NRZ (up to 30 Gbps) | 12 PAM-4 24 NRZ | | 36 PAM-4 72 NRZ | | 12 PAM-4 24 NRZ | | 36 PAM-4 72 NRZ | | 12 PAM-4 24 NRZ | | 36 PAM-4 72 NRZ | | 60 PAM-4 120 NRZ | | 12 PAM-4 24 NRZ | | 36 PAM-4 72 NRZ | | 60 PAM-4 120 NRZ | |
| | GXT transceiver count - NRZ (up to 28.3 Gbps) | 32 | | 16 | | 32 | | 16 | | 32 | | 16 | | 16 | | 32 | | 16 | | 16 | |
| | GX transceiver count - NRZ (up to 17.4 Gbps) | 16 | | 8 | | 16 | | 8 | | 16 | | 8 | | 8 | | 16 | | 8 | | 8 | |
| | PCI Express* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16) | 2 | | 1 | | 2 | | 1 | | 2 | | 1 | | 1 | | 2 | | 1 | | 1 | |
| | 100G Ethernet MAC (no FEC) hard IP blocks | 2 | | 1 | | 2 | | 1 | | 2 | | 1 | | 1 | | 2 | | 1 | | 1 | |
| | 100G Ethernet MAC + FEC hard IP blocks | 4 | | 12 | | 4 | | 12 | | 4 | | 12 | | 20 | | 4 | | 12 | | 20 | |
| | Memory devices supported | DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLD RAM II, RLD RAM 3, HMC, MoSys | | | | | | | | | | | | | | | | | | | |
| | Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O count, LVDS pairs, GXE (E-Tile) Transceiver Count, and GXT+GX (H-Tile) Transceiver Count ⁴ | | | | | | | | | | | | | | | | | | | | |
| F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch) | | 544,16,264,24,48 | | 544,16,264,24,48 | | 544,16,264,24,48 | | | 544,16,264,24,48 | | 544,16,264,24,48 | | | | | | | | | | |
| F2397 pin (50 mm x 50 mm, 1.0 mm pitch) | | 440,8,216,72,24 | | 440,8,216,72,24 | | 440,8,216,72,24 | | | 440,8,216,72,24 | | 440,8,216,72,24 | | | | | | | | | | |
| F2912 pin (55 mm x 55 mm, 1.0 mm pitch) | | - | | - | | 296,8,144,120,24 | | | 296,8,144,120,24 | | 296,8,144,120,24 | | | | | | | | | | |

Notes:

- LE counts valid in comparing across Intel FPGA devices, and are conservative vs. competing FPGAs.
- Fixed-point performance assumes the use of pre-adder.
- Floating-point performance is IEEE 754 compliant single precision.
- A subset of pins for each package are used for high-voltage, 3.0 V and 2.5 V interfaces.
- All data is preliminary, and may be subject to change without prior notice.

544,16,264,24,48 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, GXE (E-Tile) transceiver count, and GXT+GX (H-Tile) transceiver count

Indicates pin migration path.



INTEL STRATIX 10 TX PRODUCT TABLE

| PRODUCT LINE | TX 2500 | TX 2800 |
|--|--|---------|
| Processor | Quad-core 64 bit ARM Cortex-A53 MPCore* processor | |
| Maximum processor frequency | 1.5 GHz ¹ | |
| Processor cache and co-processors | <ul style="list-style-type: none"> • L1 instruction cache (32 KB) • L1 data cache (32 KB) with error correction code (ECC) • Level 2 cache (1 MB) with ECC • Floating-point unit (FPU) single and double precision • ARM NEON media engine • ARM CoreSight* debug and trace technology • System Memory Management Unit (SMMU) • Cache Coherency Unit (CCU) | |
| Scratch pad RAM | 256 KB | |
| HPS DDR memory | DDR4, DDR3, and LP DDR3 (Up to 64 bit with ECC) | |
| Direct memory access (DMA) controller | 8 channels | |
| EMAC | 3X 10/100/1000 Ethernet media access controller (EMAC) with integrated DMA | |
| USB on-the-go (OTG) controller | 2X USB OTG with integrated DMA | |
| UART controller | 2X UART 16550 compatible | |
| Serial peripheral interface (SPI) controller | 4X SPI | |
| I ² C controller | 5X I ² C | |
| Quad SPI flash controller | 1X SIO, DIO, QIO SPI flash supported | |
| SD/SDIO/MMC controller | 1X eMMC 4.5 with DMA and CE-ATA support | |
| NAND flash controller | <ul style="list-style-type: none"> • 1X ONFI 1.0 or later • 8 and 16 bit support | |
| General-purpose timers | 4X | |
| Software-programmable general-purpose I/Os (GPIOs) | Maximum 48 GPIOs | |
| HPS DDR Shared I/O | 3X 48 - May be assigned to HPS for HPS DDR access | |
| Direct I/Os | 48 I/Os to connect HPS peripherals directly to I/O | |
| Watchdog timers | 4X | |
| Security | Secure device manager, Advanced Encryption Standard (AES) AES-256/SHA-256 bitsream encryption/authentication, PUF, ECDSA 256/384 boot code authentication, side channel attack protection | |

Notes:

1. With overdrive feature.