



# Quartus Prime Pro Edition Software and Device Support Release Notes

***RN-01082-16.1.0***  
***2016.11.07***

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# 1 Quartus Prime Pro Edition Software and Device Support Release Notes Version 16.1

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This document provides late-breaking information about the Intel® Quartus® Prime Pro Edition software release version 16.1.

For information about operating system support, refer to the `readme.txt` file in your `intelFPGA_pro/<version number>/quartus` directory.

## Related Links

[Quartus Prime Standard Edition Software and Device Support Release Notes Version 16.1](#)

## 1.1 New Features and Enhancements

The Quartus Prime Pro Edition software release version 16.1 includes the following new features and enhancements:

- Intel branding in Quartus Prime software user interfaces, installation, and legal texts.
- Improved Quartus Prime Programmer GUI that accepts `.flash` files.  
For more information on this enhancement, contact [support](#).
- Support for additional `nios2-flash-programmer` command-line options in `quartus_pgm`.
- Partial Reconfiguration design flow for Arria® 10 designs.
- Qsys Pro system integration tool that offers the following capabilities:
  - Isolated and independent regeneration of all systems, subsystems, and IP.
  - Incremental regeneration of modified IP RTL only.
  - Ability to insert generic, blackbox components as placeholders that you can then customize by importing specific RTL.
  - Ability to record a design footprint consisting of interfaces, properties, and ports for team-based designs.
  - Support for IP-XACT format.
  - `qsys-validate` command-line utility that validates footprint consistency between systems and IP.
  - `qsys-archive` command-line utility that creates a `.zip` file containing all referenced Qsys Pro and IP variant files in a system.
- Updated Nios II Software Build Tools (SBT) to support Qsys Pro, which eliminates the dependency on the Quartus Prime Pro Edition software for the software simulation flow and uses the standard customer IP simulation flow.



- Incremental optimization flow that allows you to incrementally invoke each Fitter stage (that is, plan, place, route, and finalize).
- Early Place stage in the incremental optimization flow with timing analysis that correlates to final timing results in a predictable way. You can also view a representation of not fully legalized placements in the Chip Planner.
- Improved routing visualization in the Chip Planner that provides additional feedback for creating routing regions.
- **Report Design Partitions** task in the Chip Planner that generates a tree of reports (one report per design partition).
- **Report Design Partitions Advanced...** task in the Chip Planner that allows you to select the partition and generate partition routing.
- **Assignments View** tab in the Design Partitions Window of the Chip Planner that shows the settings for the next compilation.
- **Compilation View** tab in the Design Partitions Window of the Chip Planner that shows the results from the last compilation.
- Partition ports visualization for Partial Reconfiguration partitions in the Chip Planner that eases connectivity analysis and assists you in setting constraints. Chip Planner's improved routing visualization capability is a beta feature in the Quartus Prime software version 16.0.
- Redesigned interface for the LogicLock Plus Region that provides support for placement and routing regions and full integration with the Chip Planner.
- Improved handling of multi-rectangle LogicLock regions.
- Improved compilation dashboard that allows you to start your compilation from the Fitter's Plan stage if you have previously run Analysis and Synthesis. You no longer have to rerun Analysis and Synthesis after making a change to a Fitter setting. In addition, reports for completed snapshots are available while the remainder of the compilation flow is running.
- Faster compilation time using `quartus_syn` compared to `quartus_map`.
- The `quartus_fit --post_route=route_fixup` command that allows you to fix hold failures after routing.  
For more information on this enhancement, contact [support](#).
- Support for in-HDL SignalTap II Logic Analyzer that provides compilation support for the SignalTap II Logic Analyzer IP that is instantiated in user-designed HDL. It also allows the generation of SignalTap II file for SignalTap II instantiations after compilation.

## 1.2 Operating System Support

Information about OS support for the Quartus Prime Design Suite® is available on the Operating System Support page of the Altera website.

### Related Links

[Operating System Support](#)



## 1.3 Memory Recommendations

A full installation of the Quartus Prime software requires up to 24 GB of available disk space.

Intel recommends that your system be configured to provide virtual memory equal to the recommended physical RAM that is required to process your design.

*Note:* Peak virtual memory may exceed these recommendations. These recommendations are based on the amount of physical memory required to achieve runtime within 10% of that achieved on hardware with an infinite amount of RAM.

**Table 1. Memory Requirements for Processing Designs**

These requirements are the same for both Windows and Linux installations.

Family	Device	Recommended Physical RAM
Arria 10	10AT115, 10AX115	48 GB
	10AX090	44 GB
	10AS066, 10AX066	32 GB
	10AS057, 10AX057	30 GB
	10AS048, 10AX048	28 GB
	10AX032, 10AS032	24 GB
	10AX027, 10AS027	22 GB
	10AX022, 10AS022	20 GB
	10AX016, 10AS016	18 GB

## 1.4 Changes in Device Support

**Table 2. Device Support Not Fixed**

Description	Workaround
N/A	N/A

### Related Links

[Knowledge Base](#)

For more information about known device issues and workarounds.

## 1.5 Changes to Software Behavior

This section documents instances in which the behavior and default settings of the Quartus Prime Pro Edition software have been changed from earlier releases of the Quartus Prime Pro Edition software.

Refer to the Quartus Prime Default Settings File (.qdf), *<Quartus Prime installation directory>/quartus/bin/assignment\_defaults.qdf*, for a list of all the default assignment settings for the latest version of the Quartus Prime software.



### Talkback feature is removed in the Quartus Prime software

The Talkback feature has been removed from the Quartus Prime software GUI and installation. Any feature that previously required Talkback will now work without restrictions.

### Migration of a design between Quartus Prime Pro Edition software and Quartus Prime Standard Edition software, and vice versa, is not supported

The two software editions use different Quartus Prime project databases and assignments. You cannot open a design that you created in the Quartus Prime Pro Edition software in the Quartus Prime Standard Edition software. For more information on migrating a design to the Quartus Prime Pro Edition software, refer to the [Migrating to Quartus Prime Pro Edition](#) section of the *Quartus Prime Pro Edition Handbook* software.

### Quartus Prime Standard Edition software and Quartus Prime Pro Edition software have different system integration tools

Quartus Prime Standard Edition software has the Qsys system integration tool. Quartus Prime Pro Edition software has the Qsys Pro system integration tool. Qsys Pro differs from Qsys in the following manner:

- Qsys Pro is designed to support large and complex systems with more hierarchical design flows.
- Qsys Pro uses stand-alone IP to generate `.ip` files instead of `.qsys` files.
- Qsys Pro requires both the `.qsys` file and the individual `.ip` files to compile a system.

### LogicLock Plus regions in the Quartus Prime Pro Edition software are different from LogicLock regions in the Quartus Prime Standard Edition software

LogicLock Plus regions allow you to create more floorplan styles with new routing regions and support hierarchical design flows. LogicLock Plus regions include pins by default; you must select the **Core-Only** option to exclude pins to avoid no-fit errors.

### Quartus Prime Standard Edition software and Quartus Prime Pro Edition software have different design partition support

Design Partition assignments for the Quartus Prime Incremental Compilation flows in the Quartus Prime Standard Edition software are not supported in the Quartus Prime Pro Edition software.

### The `get_partition_info` command is no longer supported

The `get_partition_info` command in the Static Timing Analysis (STA) Tcl package is no longer supported in the Quartus Prime Pro Edition software.

### CTLE Triggered Adaptation Mode is no longer supported for Arria 10 devices

In the Transceiver Toolkit, the pull-down menu of the **Equalization Control** tab offers both continuous time-linear equalization (CTLE) **Triggered Adaptation** and **Manual** modes. You can only use CTLE in **Manual** mode for Arria 10 devices.



**Names of certain Quartus Prime command options have changed**

For quartus\_cdb:

- --import\_block is now --import\_partition
- --export\_block is now --export\_partition

For Tcl commands:

- design::import\_block is now design::import\_partition
- design::export\_block is now design::export\_partition

**1.6 Device Support and Pin-Out Status**

All production devices currently have full compilation, simulation, timing analysis, and programming support.

**1.7 Timing and Power Models**

**Table 3. Timing and Power Model Status**

Device Family	Device	Timing Model Status	Power Model Status
Arria 10	10AX016, 10AS016, 10AX022, 10AS022, 10AX027, 10AS027, 10AX032, 10AS032,	Final – 16.1 <sup>1</sup>	Preliminary
	10AX048, 10AS048	Final – 16.0.2	
	10AX057, 10AS057, 10AX066, 10AS066, 10AX090	Final – 16.0.1	Final – 16.0.1
	10AX115, 10AT115	Final – 16.0	Final – 16.0

**Related Links**

[System Design with Advance FPGA Timing Models](#)

**1.8 IBIS Models**

**Table 4. IBIS Model Status for the Quartus Prime Pro Edition Software Release Version 16.1**

Beginning in the Quartus Prime Pro Edition software version 16.0, device families will have IBIS model statuses that are either Advance, Preliminary, or Final.

Device Family	IBIS Model Status
Arria 10	Final – 16.1

<sup>1</sup> Timing models are preliminary for 10AX16-32/10AS16-32 fastest speed grade (-1), and final for medium and slow speed grades.



## 1.9 EDA Interface Information

**Table 5. Synthesis Tools Supporting the Quartus Prime Pro Edition Software Release Version 16.1**

Synthesis Tools <sup>2</sup>	Version
Mentor Graphics® Precision	2016a
Synopsys® Synplify, Synplify Pro, and Synplify Premier	2.15.06.09

**Table 6. Simulation Tools Supporting the Quartus Prime Pro Edition Software Release Version 16.1**

Simulation Tools	Version	Gate-Level Simulation Support
Aldec Active-HDL	10.3(Windows only)	Yes
Aldec Riviera-PRO	2015.10	Yes
Cadence Incisive Enterprise Simulator (IES)	14.20 (Linux only)	Yes
Mentor Graphics® ModelSim® PE	10.4d	Yes
Mentor Graphics ModelSim SE	10.4d	Yes
Mentor Graphics ModelSim-Intel FPGA Edition	10.5b	Yes
Mentor Graphics Questa®	10.4d	Yes
Synopsys VCS and VCS MX	2014.12-SP1 (Linux only)	Yes

### OS support for Mentor Graphics ModelSim-Intel FPGA Edition version 10.5b (requires 32-bit libraries)

- Windows 7 SP1 (64-bit)
- Windows 8.0 (64-bit)
- Windows 10 (64-bit)
- Windows Server 2008 R2 SP1(64-bit)
- Red Hat Enterprise Linux 5.10 (64-bit)
- Red Hat Enterprise Linux 6.5 (64-bit)
- Red Hat Enterprise Linux 7.2 (64-bit)

## 1.10 Antivirus Verification

The Quartus Prime software release version 16.1 has been verified virus free using the following software:

- 
- 2 EDA Synthesis tools that support the Quartus Prime software version 16.1 will be released by vendors shortly after the release of the Quartus Prime software. Contact your vendor account manager for details.





### Antivirus Verification Software for Windows

McAfee Agent Version: 5.0.1.516  
 McAfee VirusScan Enterprise + AntiSpyware Enterprise Version: 8.8.0 (8.8.0.1445)  
 Scan Engine Version (32 bit): 5800.7501  
 Scan Engine Version (64 bit): 5800.7501  
 DAT Version: 8319.0000

## 1.11 Latest Known Quartus Prime Software Issues

Information about known issues that affect the Quartus Prime software version 16.1 is available on the Knowledge Base webpage .

### Known Software Issues Affecting the Quartus Prime Software Version 16.1

You can find known issue information for previous versions of the Quartus Prime software on the Knowledge Base webpage.

Information about known software issues that affect previous versions of the Quartus II software is available on the Quartus Prime and Quartus II Software Support webpage.

Information about issues affecting the Intel FPGA IP Library is available in the *Intel FPGA IP Release Notes*.

### Related Links

- [Knowledge Base](#)
- [Quartus Prime and Quartus II Software Support](#)
- [Intel FPGA IP Release Notes](#)

## 1.12 Document Revision History

**Table 7. Quartus Prime Software Release Version 16.1 Document Revision History**

Date	Version	Changes
November 2016	16.1.0	Initial release.