Quartus II Software Version 11.1 Release Notes

This document provides late-breaking information about the following areas of the Altera® Quartus® II software version 11.1.

For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<*version number*>/quartus directory**. For information about device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the *Quartus II Version 11.1 Device Support Release Notes*. For the latest information about the MegaCore® IP Library, refer to the *MegaCore IP Library Release Notes and Errata*.

New Features & Enhancements

The Quartus II software version 11.1 includes the following new features and enhancements:

- Qsys and the MegaWizard Plug-In Manager generate scripts to help you set up your simulation environment for third-party simulators.
- The Tasks window now includes flows for gate-level and register transfer level (RTL) simulation.
- The Quartus II software version 11.1 allows you to create parameters in a Qsys system. The parameters that you create in a system appear when you use a Qsys system as a subcomponent of another Qsys system.
- Advanced Microcontroller Bus Architecture Advanced eXtensible Interface (AMBA AXI) support in Qsys is a beta feature. For details about the limitations of AXI beta support in Qsys version 11.1, refer to the AXI Support page on the Altera Wiki.

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- The Transceiver Toolkit includes the following improvements:
  - Stratix V device support including support for eye contour graphs
  - Enhanced performance, enabling you to skip poor-performing tests quickly
  - Automatic design loading with the System Console
- On the Help menu, you can click **Feedback** to provide feedback, report an issue, and make suggestions about the usability of the Quartus II software.
- Quartus II Help can be used with the following browsers:
  - Local Quartus II Help (Help on a local drive installed by the Altera Installer) is fully compatible with Microsoft Internet Explorer 8, Mozilla Firefox 7.0, and Safari 5 running on Windows 7 operating systems. You can view the Quartus II Help in Google Chrome; however, you cannot open a Chrome browser from the Quartus II GUI. You must start Chrome with the `--allow-file-access-from-files flag` and then navigate to *<quartus installation directory>***/common/help/master.htm**.
  - Local Quartus II Help is fully compatible with Mozilla Firefox 3.6 running on Linux 32-bit systems.
  - Quartus II Web Help (hosted at http://quartushelp.altera.com/current) is fully compatible with Microsoft Internet Explorer 8, Mozilla Firefox 7.0, Safari 5, and Google Chrome.

  Some Help features require you to disable pop-up blocking.

EDA Interface Information

The Quartus II software version 11.1 supports the following EDA tools:

Synthesis Tools	Version	NativeLink Support
Synopsys Synplify, Synplify Pro, and Synplify Premier	E-2011.03	✓
Mentor Graphics® Precision RTL Synthesis	2011a	✓
Mentor Graphics LeonardoSpectrum™	2011a	✓
Mentor Graphics DK Design Suite	5.0 SP5	✓
Simulation Tools	**Version**	**NativeLink Support**
Mentor Graphics ModelSim®	10.0b	✓
Mentor Graphics ModelSim-Altera	10.0c	✓
Mentor Graphics ModelSim-Altera Starter Edition	10.0c	✓
Mentor Graphics QuestaSim	10.0b	✓
Cadence NC-Sim	10.2 (Linux only)	—
Synopsys VCS / VCS MX	2011.03 (Linux only)	✓
Aldec Active-HDL	8.3-SP1 (Windows only)	✓

Aldec Riviera-PRO	2011.06	✓
Formal Verification Tools (Equivalence Checking)	**Version**	**NativeLink Support**
Cadence Encounter Conformal	8.1	—
Chip Level Static Timing Analysis	**Version**	**NativeLink Support**
Synopsys PrimeTime	Z-2007.06	✓
Board Level Static Timing Analysis	**Version**	**NativeLink Support**
Mentor Graphics TAU	—	—
Board Level Symbol/Pin-out Management	**Version**	**NativeLink Support**
Mentor Graphics I/O Designer	—	—

Changes to Software Behavior

This section documents instances in which the behavior and default settings of the Quartus II software have been changed from earlier releases of the software.

Refer to the Quartus II Default Settings File (**.qdf**), *<Quartus II installation directory>***/quartus/bin/assignment_defaults.qdf**, for a list of all the default assignment settings for the latest version of the Quartus II software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
Version 11.1	
If you generate an ALTLVDS_RX megafunction created with the Quartus II software version 9.1SP2 or earlier with the Quartus II software version 10.1 or later, the megafunction is not generated correctly.	In the Quartus II software version 9.1SP2 and earlier, the net name of the megafunction was lowercase. In the Quartus II software version 10.1 and later, the net name is uppercase. If you import an ALTLVDS_RX megafunction from the Quartus II software version 9.1SP2 or earlier to the Quartus II software version 10.1 or later, change all instances of `altlvds_rx` to `ALTLVDS_RX` in your project files.
If you generate an ALTLVDS_TX megafunction created with the Quartus II software version 9.1SP2 or earlier with the Quartus II software version 10.1 or later, the megafunction is not generated correctly.	In the Quartus II software version 9.1SP2 and earlier, the net name of this megafunction was lowercase. In the Quartus II software version 10.1 and later, the net name is uppercase. If you import an ALTLVDS_TX megafunction from the Quartus II software version 9.1SP2 or earlier to the Quartus II software version 10.1 or later, change all instances of `altlvds_tx` to `ALTLVDS_TX` in your project files.

Description	Workaround
The Quartus II software no longer supports the FAT32 file system. On Windows machines, the Quartus II software is supported only on the NTFS file system. If you attempt to install the Quartus II software version 11.1 to a FAT32 file system, installation fails with the error: `Permission denied.`	If your file system is FAT32, you can convert it to NTFS with the `convert` command. For more information, type `help convert` at a Windows command prompt.
Altera functional simulation libraries no longer provide VHDL 1076-1987 functional simulation models.	Use VHDL 1976-1993 or later.

Known Issues & Workarounds

For more information about known software issues, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-index.jsp

General Quartus II Software Issues

This section provides information about the following known issues that affect the Quartus II Software:

- Error (199055): Can't generate files for Synopsys PrimeTime timing analysis tool because VHDL format is not supported if the TimeQuest Timing Analyzer is selected as the timing analysis tool in the current device family
- Error (20004): Family name "Cyclone IV GX" is illegal
- PHY IP can fail timing due to negative recovery slack
- Dialog boxes that open or select files can be very slow to open in Quartus Programmer
- Internal Error: The periphery placer encountered a problem due to difficult routing constraints. Please try changing the seed to work around this.
- Error (134004): The file <file name>.ppf could not be found
- Error (272006): MGL_INTERNAL_ERROR: Port object altiobuf_out
- Internal Error: Sub-system: ACVQM, File: /quartus/ace/acvq/acvqm/acvqm_command_manager.cpp, Line: 3208 mapper != NULL
- Simulating an Avalon MM master or slave BFM with msim_setup.tcl in ModelSim leads to errors
- Internal Error: Sub-system: A2T, File: /quartus/tsm/a2t/a2t_tgx_visitor.cpp, Line: 7484 Should not have this block in this netlist!

Error (199055): Can't generate files for Synopsys PrimeTime timing analysis tool because VHDL format is not supported if the TimeQuest Timing Analyzer is selected as the timing analysis tool in the current device family

Description

Generation of a VHDL netlist for Synopsys PrimeTime is not supported. If you attempt to generate a netlist for Synopsys PrimeTime from VHDL, generation fails with the error:

```
Error (199055): Can't generate files for Synopsys PrimeTime timing analysis tool because VHDL format is not supported if the TimeQuest Timing Analyzer is selected as the timing analysis tool in the current device family
```

Workaround

Use Verilog HDL.

Error (20004): Family name "Cyclone IV GX" is illegal

Description

Generation of CPRI, Ethernet 10G MAC, DDR2 SDRAM Controller with UniPHY, DDR3 SDRAM Controller with UniPHY, QDR II and QDR II+ SRAM Controller with UniPHY, and RLDRAM II Controller with UniPHY megafunctions might fail if you have not installed Cyclone IV GX device support. During generation, the MegaWizard Plug-In Manager displays a message similar to the following:

```
Error: Error (20004): Family name "Cyclone IV GX" is illegal
```

Workaround

Install Cyclone IV GX device support.

PHY IP can fail timing due to negative recovery slack

Description

Designs that target Arria V, Cyclone V, or Stratix V devices and that include a PHY IP megafunction can fail timing due to negative recovery slack caused by long clock routing to the global clock.

Workaround

In the **More Fitter Settings** dialog box, turn off **Auto Global Register Control Signals**.

Dialog boxes that open or select files can be very slow to open in Quartus Programmer

Description

Dialog boxes that open or select files (such as **Open**, **Open Project**, **Save As**) can be very slow to open in Quartus Programmer.

Workaround

You can speed up these dialog boxes by adding to your **quartus.ini** file the following line:

```
use_native_windows_file_dialogs=on
```

This line speeds up the dialog boxes, but reduces their functionality.

Internal Error: The periphery placer encountered a problem due to difficult routing constraints. Please try changing the seed to work around this.

Description

Under rare circumstances, designs that use many global clocking resources could cause the Quartus II Fitter to exit with the following internal error message:

```
Internal Error: The periphery placer encountered a problem due to difficult routing constraints. Please try changing the seed to work around this.
```

Workaround

In the **Fitter Settings** dialog box, change the **Seed** value and run compilation again.

Error (134004): The file <file name>.ppf could not be found

Description

Some megafunctions cannot be created or imported with the Pin Planner. Attempting to create or import an unsupported megafunction with the **Create/Import Megafunction** command fails with the error:

```
Error (134004): The file <file name>.ppf could not be found
```

Workaround

<none>

Error (272006): MGL_INTERNAL_ERROR: Port object altiobuf_out

Description

ALTIOBUF megafunctions targeting Arria V or Cyclone V devices that are configured **As an output buffer** or **As a bidirectional buffer** and that **Use series and parallel termination controls** have incorrect `width_stc` and `width_ptc` port widths. The port widths of these ports in the generated megafunction is `14`; they should be `16`. During compilation, Analysis & Synthesis fails with errors similar to the following:

```
Error (272006): MGL_INTERNAL_ERROR: Port object
altiobuf_out|stratixv_io_obuf inst obufa|parallelterminationcontrol of
width  16 is being assigned the port altiobuf_out|paralleltermination-
control of width 14 which is illegal, as port widths dont match nor are
multiples.
```

```
Error (272006): MGL_INTERNAL_ERROR: Port object
altiobuf_out|stratixv_io_obuf inst obufa|seriesterminationcontrol of
width  16 is being assigned the port altiobuf_out|seriesterminationcon-
trol of width 14 which is illegal, as port widths dont match nor are
multiples.
```

Workaround

Edit the generated ALTIOBUF wrapper file so that the widths of the `width_stc` and `width_ptc` variables are `16`.

Internal Error: Sub-system: ACVQM, File: /quartus/ace/acvq/acvqm/acvqm_command_manager.cpp, Line: 3208 mapper != NULL

Description

If you run **Report HSSI Block Connectivity** in the Chip Planner without a project open, the Chip Planner abnormally exits with an error similar to the following:

```
Internal Error: Sub-system: ACVQM, File: /quar-
tus/ace/acvq/acvqm/acvqm_command_manager.cpp, Line: 3208 mapper != NULL
```

Workaround

The Report HSSI Block Connectivity feature is beta for evaluation purposes only in the Quartus II software version 11.1. Do not run **Report HSSI Block Connectivity** without first opening a project.

Simulating an Avalon MM master or slave BFM with msim_setup.tcl in ModelSim leads to errors

Description

If you attempt to simulate an Altera Avalon Memory-Mapped (MM) Master bus functional model (BFM), or an Altera Avalon MM Slave BFM using the generated ModelSim script **msim_setup.tcl**, ModelSim may issue error messages similar to the following:

```
Error: test_module.sv(2): Could not find the package (avalon_mm_pkg).
```

```
Error: (vsim-8386) ./test_module.sv(75): An enum variable may only be
assigned the same enum typed variable or one of its values.
```

Workaround

Perform one to the following steps:

- At a command prompt, run "`ip-make-simscript --spd=<generated_spd_file> --compile-to-work`" to regenerate the ModelSim simulation script that compiles all component into a single work library, or
- Manually modify the **msim_setup.tcl** script to compile all files into a single work library.

Internal Error: Sub-system: A2T, File: /quartus/tsm/a2t/a2t_tgx_visitor.cpp, Line: 7484 Should not have this block in this netlist!

Description

If your design contains a HardCopy one-time-programmable (OTC) block and at least one physical synthesis option is enabled in the Quartus II software, Analysis & Synthesis fails with an error similar to the following:

```
Internal Error: Sub-system: A2T, File: /quar-
tus/tsm/a2t/a2t_tgx_visitor.cpp, Line: 7484 Should not have this block
in this netlist!
```

Workaround

If your design contains a HardCopy OTC block, do not enable any physical synthesis options; if any physical systhesis options are enabled, do not use a HardCopy OTC block in your design.

Platform-Specific Issues

This section provides information about the following known issues that affect the Quartus II software when it is running on specific operating systems:

- Error:Error in CNX file format.

Error:Error in CNX file format.

Description

The 32-bit implementation of the Quartus II software versions 11.0 and 11.1 running Linux operating systems cannot open the following megafunctions in the MegaWizard Plug-In Manager:

- ALTDDIO_BIDIR
- ALTDDIO_IN
- ALTDDIO_OUT
- ALTDQ
- ALTLVDS_RX
- ALTLVDS_TX
- RAM initializer

Attempting to open any of these megafunctions fails with the error:

```
Error:Error in CNX file format.
```

Workaround

Use the 64-bit implementation of the Quartus II software.

Device Family Issues

This section provides information about the following known issues that affect designs that target specific device families in the Quartus II Software:

Arria II Known Issues

The following known issue affects designs that target the Arria II device family:

- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the Arria II device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_aii_ki

Arria V Known Issues

The following known issues affect designs that target the Arria V device family:

- Incremental compilation is not available for designs that target the Arria V device family.
- Error (175001): Could not place pin rx_in[0] in a design that targets the Arria V device family
- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the Arria V device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_av_ki

Arria GX Known Issues

The following known issue affects designs that target the Arria GX device family:

- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the Arria GX device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_agx_ki

Cyclone II Known Issues

The following known issue affects designs that target the Cyclone II device family:

- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the Cyclone II device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_cii_ki

Cyclone III Known Issues

The following known issue affects designs that target the Cyclone III device family:

- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the Cyclone III device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_ciii_ki

Cyclone IV Known Issues

The following known issue affects designs that target the Cyclone IV device family:

- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the Cyclone IV device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_civ_ki

Cyclone V Known Issues

The following known issues affect designs that target the Cyclone V device family:

- Quartus II logic options MAX_GLOBAL_CLOCKS_ALLOWED and MAX_CLOCKS_ALLOWED cannot be used with Cyclone V devices
- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the Cyclone V device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_cv_ki

HardCopy II Known Issues

The following known issue affects designs that target the HardCopy II device family:

- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the HardCopy II device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_hcii_ki

HardCopy III Known Issues

The following known issue affects designs that target the HardCopy III device family:

- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the HardCopy III device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_hciii_ki

HardCopy IV Known Issues

The following known issue affects designs that target the HardCopy IV device family:

- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the HardCopy IV device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_hciv_ki

Stratix II Known Issues

The following known issue affects designs that target the Stratix II device family:

- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the Stratix II device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_sii_ki

Stratix II GX Known Issues

The following known issue affects designs that target the Stratix II GX device family:

- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the Stratix II GX device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_siigx_ki

Stratix III Known Issues

The following known issues affect designs that target the Stratix III device family:

- Exceeding the clock boost factor specified in the Stratix III Device Datasheet may cause you design to fail without warning
- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the Stratix III device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_siii_ki

Stratix IV Known Issues

The following known issues affect designs that target the Stratix IV device family:

- An ALTPLL megafunction that targets a Stratix IV device might not retain updated settings
- XAUI PHY: the Quartus II software might change PLL type from ATX to CMU during importation of a design that targets the Stratix V device family
- Designs that contain a DCFIFO megafunction might fail in hardware

For more information about known Quartus II software issues that affect the Stratix IV device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_siv_ki

Stratix V Known Issues

The following known issues affect designs that target the Stratix V device family:

- Designs that contain a DCFIFO megafunction might fail in hardware
- For designs that target the Stratix V device family, you cannot import a Low Latency PHY instance created with an earlier version of the Quartus II software to the Quartus II software version 11.1
- Error RTL 18.3: Function call does not refer to function definition
- INTERNAL ERROR: (vsim-8603) Package 'sv_xcvr_h' has exported 252 items, but 251 items were expected during simulation of a PCI Express megafunction with Mentor Graphics ModelSim SE version 10.0b
- The Quartus II software does not honor DSP Block Balancing assignments made directly to inferred multipliers.
- Dynamic PLL reconfiguration with Stratix V devices has not been tested on hardware
- PLL output counter rotation and PLL merging are not available with the Altera PLL Reconfig v11.1 and Altera PLL v11.1 megafunctions
- To accomplish post-fit simulation of an Altera PLL Reconfig v11.1 megafunction, you must first define a tag

- Output clock edges of Altera PLL megafunctions configured in MHz are not guaranteed to arrive in the same simulation cycle as their corresponding reference clock edges.
- Transmit (TX) Custom PHY megafunctions are not operational on hardware if an adjacent receive (RX) PHY is absent.
- Stratix V ES transceiver REFCLK positive and negative pins are swapped
- Internal Error: Sub-system: ASM, File: /quartus/comp/asm/asm_le.cpp, Line: 3983 !local_delay_chain_used
- The TXPLL of a Deterministic Latency PHY cannot lock if external feedback from tx_clkout is enabled
- Reconfiguration of Custom PHY, Deterministic Latency PHY, and Low Latency PHY megafunctions is not supported

For more information about known Quartus II software issues that affect the Stratix V device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_sv_ki

Incremental compilation is not available for designs that target the Arria V device family.

Description

Incremental compilation is not available for designs that target the Arria V device family.

Workaround

<none>

Designs that contain a DCFIFO megafunction might fail in hardware

Description

The Quartus II software version 11.1 does not correctly analyze timing paths to the memory block within dual-clock FIFO (DCFIFO) megafunctions correctly. Although no timing violations are reported, designs containing a DCFIFO megafunction might fail in hardware or during gate-level simulation.

This problem affects DCFIFO megafunctions that target the following device families: Arria II, Arria V, Arria GX, Cylcone II, Cyclone III, Cyclone IV, Cyclone V, HardCopy II, HardCopy III, HardCopy IV, Stratix II, Stratix II GX, Stratix III, Stratix IV, and Stratix V.

Many Altera megafunctions include a DCFIFO megafunction. To determine whether your design contains a DCFIFO megafunction, refer to the Analysis and Synthesis reports.

Workaround

Refer to the solution Why does my DCFIFO not function correctly in hardware or in simulation? on the Altera website.

Error (175001): Could not place pin rx_in[0] in a design that targets the Arria V device family

Description

Connecting an LVDS receiver (RX) input to multiple LVDS blocks is illegal; however, the Quartus II software does not check for such illegal connectivity in designs that target Arria V devices. If you connect an LVDS RX input to multiple LVDS blocks, compilation fails with errors similar to the following:

```
Error (175001): Could not place pin rx_in[0]

Info (175002): The causes below are listed in descending order of severity

Error (175006): Could not find path between lvds_rx:inst3|altlvds_rx:ALTLVDS_RX_component|lvds_rx_lvds_rx:auto_generated|lvds_rx_d   pa3 and pin rx_in[0]

Error (175021): lvds_rx:inst3|altlvds_rx:ALTLVDS_RX_component|lvds_rx_lvds_rx:auto_generated|lvds_rx_dpa3 was placed into device location       "SERDESDPA_X29_Y0_N68"

Error (175022): pin rx_in[0] could not be placed into any device location to satisfy its connectivity requirements

Error (175006): Could not find path between lvds_rx:inst|altlvds_rx:ALTLVDS_RX_component|lvds_rx_lvds_rx:auto_generated|lvds_rx_dp   a3 and pin rx_in[0]

Error (175021): lvds_rx:inst|altlvds_rx:ALTLVDS_RX_component|lvds_rx_lvds_rx:auto_generated|lvds_rx_dpa3 was placed into device location "SERDESDPA_X20_Y0_N68"

Error (175022): pin rx_in[0] could not be placed into any device location to satisfy its connectivity requirements

Error (184016): There were not enough differential input pin locations available
```

Workaround

Do not connect an LVDS RX input to multiple LVDS blocks.

Quartus II logic options MAX_GLOBAL_CLOCKS_ALLOWED and MAX_CLOCKS_ALLOWED cannot be used with Cyclone V devices

Description

If you use **Maximum Number of Global Clocks Allowed** or **Maximum Number of Clocks of Any Type Allowed** logic options in designs that target the Cyclone V device family, compilation fails with an error similar to the following:

```
Internal Error: Sub-system: FSV, File: /quartus/fit-
ter/fsv/fsv_module.cpp, Line: 2307 Found destination cell
RESERVEDCLKENAGCLK0 that has no atom id while clustering
```

Workaround

Do not use these logic options in your Quartus II settings file (**.qsf**). If it is necessary to reduce clock network usage, for example, to reserve clock resources for future design changes, use the **Global Signal** logic option to prevent specific signals from using global clock network resources.

Exceeding the clock boost factor specified in the Stratix III Device Datasheet may cause you design to fail without warning

Description

If you use an external PLL with an ALTLVDS_RX megafunction, configuring the data rate and input clock frequency such that the clock boost factor (W) exceeds the maximum clock boost factor listed in the *Stratix III Device Datasheet* may cause your design to fail. The Quartus II software does not issue an error if the clock boost factor exceeds the limit shown in the device datasheet.

Workaround

Ensure that the clock boost factor (the ratio between the input data rate and the input clock rate) does not exceed the maximum value specified in the Stratix III Device Datasheet.

An ALTPLL megafunction that targets a Stratix IV device might not retain updated settings

Description

If you change the settings of a generated ALTPLL megafunction and then regenerate it, the regenerated ALTPLL megafunction might retain the settings of the original megafunction.

Workaround

To force the Quartus II software to regenerate the ALTPLL megafunction with the changed settings, remove the <*path to project*>**/db** directory.

XAUI PHY: the Quartus II software might change PLL type from ATX to CMU during importation of a design that targets the Stratix V device family

Description

If you import a XAUI PHY instance created with the Quartus II software version 11.0 SP1 or earlier that has **PLL type** set to **ATX** to the Quartus II software 11.1 or later, the Quartus II software changes **PLL type** to **CMU**.

Workaround

To retain the ATX PLL type, on the **General Options** tab of the XAUI PHY MegaWizard Plug-in Manager page, change **PLL type** to **ATX** before generating your XAUI PHY instance.

For designs that target the Stratix V device family, you cannot import a Low Latency PHY instance created with an earlier version of the Quartus II software to the Quartus II software version 11.1

Description

You cannot migrate a design containing a Low Latency PHY megafunction instance that was created in the Quartus II software version 10.0 SP1 or earlier to the Quartus II software version 11.1.

Workaround

Use the MegaWizard Plug-In Manager in the Quartus II software version 11.1 to recreate your Low Latency PHY instance.

Error RTL 18.3: Function call does not refer to function definition

Description

If you attempt to use the Cadence Encounter Conformal software for formal verification of **altddio_out.v**, **altlvds_tx.v**, **altlvds_rx.v**, **lvds_tx.v**, **lvds_rx.v**, **flvds_tx.v**, **flvds_rx.v**, **altmult_add.v**, **altmult_accum.v**, or **altpll.v**, formal verification fails with the error:

```
Error RTL 18.3: Function call does not refer to function definition
```

Workaround

You cannot verify these files with the Cadence Encounter Conformal software.

INTERNAL ERROR: (vsim-8603) Package 'sv_xcvr_h' has exported 252 items, but 251 items were expected during simulation of a PCI Express megafunction with Mentor Graphics ModelSim SE version 10.0b

Description

During simulation of a Stratix V design that includes a PCI Express® megafunction, Mentor Graphics® ModelSim® SE version 10.0b may issue a fatal error similar to the following:

```
# ** INTERNAL ERROR: (vsim-8603) Package 'sv_xcvr_h' has exported 252
items, but 251 items were expected.

# Region: /top_tb/top_inst/ap-
ps/g_bypass_xcvr_reconfig/genblk1/top_inst
```

Workaround

Use Mentor Graphics ModelSim SE version 10.0c, or use the `-novopt` option with the vsim command in Mentor Graphics ModelSim SE version 10.0b.

The Quartus II software does not honor DSP Block Balancing assignments made directly to inferred multipliers.

Description

For designs that target the Stratix V device family, the Quartus II software does not honor DSP Block Balancing assignments made directly to inferred multipliers.

Workaround

Specify the DSP Block Balancing assignments in your project Quartus II Settings File (**.qsf**).

Dynamic PLL reconfiguration with Stratix V devices has not been tested on hardware

Description

Dynamic PLL reconfiguration with Stratix V devices has not been tested on hardware and is beta for evaluation purposes only. Altera does not recommend using this beta feature for designs intended for production.

Workaround

Do not program production designs that contain PLL dynamic reconfiguration operations for Stratix V devices.

PLL output counter rotation and PLL merging are not available with the Altera PLL Reconfig v11.1 and Altera PLL v11.1 megafunctions

Description

PLL output counter rotation and PLL merging are not available with the Altera PLL Reconfig v11.1 and Altera PLL v11.1 megafunctions. (The Fitter may attempt PLL output counter rotation and PLL merging to improve routability and minimize area.)

Dynamic PLL reconfiguration with post-fit simulation is supported with the following restrictions:

1 A reconfigurable PLL must be placed at FPLL_0, a bottom fractional PLL within one single fracturable PLL location.

2 Before you specify transceiver dynamic reconfiguration addresses, you must determine the post-fit output counter placement because the logical output counter location might differ from the physical output counter location.

Workaround

In your project's Quartus II Settings File (**.qsf**), set the location of the reconfigurable PLL to FPLL_0 with the following statement:

```
set_location_assignment FRACTIONALPLL_X210_Y1_N0 -to
"pll:pll_inst|pll_0002:pll_inst|altera_pll:altera_pll_i|altera_stratix
v_pll:stratixv_pll|altera_stratixv_pll_base:fpll_0|fpll"
```

Run the Fitter before specifying transceiver dynamic reconfiguration addresses for dynamic phase shift and C counter reconfiguration operations.

To accomplish post-fit simulation of an Altera PLL Reconfig v11.1 megafunction, you must first define a tag

Description

To accomplish post-fit simulation of an Altera PLL Reconfig v11.1 megafunction, you must first define a tag.

Workaround

For example, in ModelSim, define the tag as follows:

```
"vlog +define+POSTFIT_SIM_USE_ICD_PLL_RECONFIG_MODEL=1 +de-
fine+TOP_LEVEL_MODULE=<top_inst>
<quartus_directory>/eda/sim_lib/stratixv_atoms.v"
```

Where `<top_inst>` is the instance name of the top level of your design.

Output clock edges of Altera PLL megafunctions configured in MHz are not guaranteed to arrive in the same simulation cycle as their corresponding reference clock edges.

Description

If you configure an output clock of a nonreconfigurable Altera PLL v11.1 megafunction with **Desired Frequency (MHz)**, the output clock produced is based on the events of the reference clock; during simulation of the megafunction, output clock edges arrive at the correct simulation time, but are not guaranteed to arrive in the same simulation cycle as their corresponding reference clock edges.

Workaround

To align the edges of the reference and output clocks, perform one of the following steps:

- Add small delays to the reference clock assignments, or
- Specify the reference clock period in ps instead of specifying its frequency in MHz.

Transmit (TX) Custom PHY megafunctions are not operational on hardware if an adjacent receive (RX) PHY is absent.

Description

Transmit (TX) Custom PHY megafunctions are not operational on hardware if an adjacent receive (RX) PHY is absent.

Workaround

Instantiate an empty RX PHY in the unused RX location.

Stratix V ES transceiver REFCLK positive and negative pins are swapped

Description

In Stratix V ES devices, the transceiver REFCLK positive and negative pins are swapped.

Workaround

Altera recommends keeping the same pin-out for both ES and production devices with respect to this issue. If the REFCLK feeds the core of the device, you can apply 180-degree phase shift with a TimeQuest Timing Analyzer assignment to generate correct timing for ES devices.

Internal Error: Sub-system: ASM, File: /quartus/comp/asm/asm_le.cpp, Line: 3983 !local_delay_chain_used

Description

Moving registers with Engineering Change Orders (ECOs) in the Chip Planner is unstable for the Stratix V device family. Check and Save operations of designs containing registers moved with ECOs might fail with errors similar to the following:

```
Internal Error: Sub-system: ASM, File: /quartus/comp/asm/asm_le.cpp,
Line: 3983 !local_delay_chain_used
```

Workaround

<none>

The TXPLL of a Deterministic Latency PHY cannot lock if external feedback from tx_clkout is enabled

Description

TXPLL external feedback for Deterministic Latency PHY megafunctions has not been verified as working with Stratix V devices. The TXPLL cannot lock if external feedback from tx_clkout is enabled.

Workaround

<none>

Reconfiguration of Custom PHY, Deterministic Latency PHY, and Low Latency PHY megafunctions is not supported

Description

Reconfiguration of Custom PHY, Deterministic Latency PHY, and Low Latency PHY megafunctions is not supported by the Quartus II software version 11.1.

Workaround

<none>

Antivirus Verification

The Altera Complete Design Suite version 11.1 has been verified virus free using the following software:

AVG Version 2012.0.1869
Virus database version: 2092/1

McAfee VirusScan Enterprise + AntiSpyware Enterprise 8.7.i (8.7.0.570)
Scan Engine Version: 5400.1158
DAT Version: 6519.0000

Latest Known Quartus II Software Issues

For more information about known software issues, look for information on the **Quartus II Software Support** page at the following URL:

http://www.altera.com/support/software/sof-quartus.html

You can find known issue information for previous versions of the Quartus II software on the Knowledge Database page at the following URL:

http://www.altera.com/support/kdb/kdb-index.jsp

Software Issues Resolved

The following Customer Service Requests were fixed or otherwise resolved in the Quartus II software version 11.1

Customer Service Request Numbers Resolved in the Quartus II Software Version 11.1							
10540828	10546229	10587039	10627362	10654679	10661316	10661910	10663598
10664363	10664365	10671783	10673977	10674165	10682676	10685727	10685931
10689196	10690667	10694050	10694765	10695997	10698562	10699744	10703153
10708253	10717050	10723848	10725380	10727537	10728466	10729062	10732886
10733513	10734320	10735937	10736673	10736684	10738729	10741192	10743893
10745321	10745642	10747673	10750562	10750954	10751430	10751749	10753233
10753354	10753452	10754148	10754552	10755214	10757373	10758207	10759027
10759155	10760752	10763331	10763383	10764020	10764172	10766656	10767004
10768085	10768240	10768916	10769347	10769667	10770116	10770694	10770769
10770982	10771377	10771554	10771915	10772039	10773446	10773582	10774000
10774597	10775291	10775898	10776002	10776698	10776890	10776898	10776919
10777078	10778212	10778449	10779831	10780656	10781567	10782720	10782765
10783067	10783293	10784253	10784296	10784543	10784768	10784791	10785647
10785755	10786017	10786232	10786350	10786585	10787181	10787285	10787490
10787680	10788375	10788670	10789561	10789577	10790393	10790470	10790750

Customer Service Request Numbers Resolved in the Quartus II Software Version 11.1							
10790800	10790803	10791558	10791948	10792190	10792445	10792600	10793398
10793399	10793546	10793725	10793886	10794113	10794176	10794178	10794552
10794668	10794726	10794801	10794867	10795043	10795138	10795152	10795209
10795229	10795312	10795348	10795450	10795672	10795754	10795954	10795975
10796036	10796282	10796566	10796673	10796877	10796889	10796892	10797018
10797029	10797088	10797089	10797120	10797219	10797276	10797419	10797545
10797641	10797670	10797750	10797819	10798064	10798089	10798355	10798475
10798497	10798500	10798844	10798984	10799198	10799512	10800208	10800445
10800458	10800482	10800488	10800749	10800753	10800925	10800928	10801123
10801197	10801280	10801454	10801486	10802018	10802062	10802464	10802587
10802647	10802759	10802870	10802899	10802946	10803028	10803035	10803051
10803124	10803128	10803138	10803240	10803258	10803448	10803477	10803632
10803804	10803952	10804056	10804427	10804431	10804447	10804487	10804520
10804754	10804758	10804837	10804859	10805024	10805076	10805215	10805308
10805377	10805398	10805580	10805592	10805797	10805822	10805855	10805960
10805997	10806013	10806158	10806161	10806170	10806244	10806304	10806305
10806318	10806330	10806340	10806356	10806384	10806456	10806470	10806471
10806484	10806530	10806564	10806595	10806665	10806738	10806808	10806818
10806819	10806834	10806863	10806936	10806944	10807000	10807016	10807093
10807152	10807163	10807209	10807225	10807248	10807251	10807296	10807325
10807355	10807400	10807435	10807476	10807512	10807572	10807622	10807665
10807698	10807902	10807980	10807987	10808045	10808195	10808384	10808780
10808797	10808817	10808831	10808841	10808844	10808961	10809218	10809533
10809618	10809630	10809798	10809802	10809822	10809848	10809913	10809932
10810065	10810094	10810125	10810167	10810232	10810286	10810348	10810450
10810484	10810529	10810533	10810621	10810696	10810700	10810730	10810743
10810757	10810800	10810849	10810911	10810946	10810950	10810992	10811031
10811043	10811066	10811070	10811088	10811091	10811195	10811412	10811449
10811463	10811477	10811501	10811552	10811645	10811752	10811838	10811888
10811893	10811912	10811952	10811990	10812115	10812117	10812121	10812192
10812193	10812357	10812376	10812378	10812400	10812539	10812540	10812738
10812749	10812781	10812809	10812820	10812824	10812838	10812911	10813026

Customer Service Request Numbers Resolved in the Quartus II Software Version 11.1							
10813033	10813046	10813053	10813077	10813084	10813089	10813090	10813120
10813148	10813255	10813294	10813344	10813350	10813444	10813477	10813544
10813581	10813671	10813703	10813753	10813781	10813805	10813825	10813908
10813985	10814034	10814093	10814126	10814191	10814276	10814295	10814322
10814326	10814433	10814471	10814476	10814486	10814599	10814602	10814622
10814628	10814635	10814636	10814642	10814645	10814694	10814704	10814831
10814866	10815030	10815048	10815101	10815112	10815163	10815306	10815386
10815388	10815421	10815515	10815516	10815569	10815622	10815760	10815792
10815833	10815986	10816004	10816039	10816044	10816127	10816161	10816167
10816171	10816188	10816200	10816241	10816299	10816300	10816325	10816369
10816428	10816434	10816445	10816457	10816472	10816548	10816653	10816696
10816748	10816844	10816889	10816920	10816936	10816952	10816960	10817001
10817064	10817083	10817096	10817105	10817139	10817153	10817154	10817178
10817179	10817337	10817380	10817389	10817395	10817522	10817555	10817558
10817703	10817756	10817772	10817774	10817812	10817827	10817851	10817878
10817938	10817951	10817971	10817986	10818059	10818069	10818144	10818146
10818158	10818162	10818240	10818276	10818392	10818475	10818488	10818640
10818724	10818783	10818789	10818873	10818884	10818950	10818981	10819059
10819113	10819121	10819128	10819167	10819254	10819301	10819313	10819463
10819481	10819528	10819532	10819593	10819657	10819675	10819686	10819689
10819711	10819728	10819800	10819823	10819891	10820013	10820025	10820092
10820232	10820235	10820294	10820383	10820406	10820419	10820461	10820566
10820592	10820606	10820628	10820636	10820657	10820786	10820827	10820845
10820874	10820931	10820965	10820994	10821147	10821194	10821257	10821268
10821442	10821446	10821451	10821582	10821686	10821690	10821757	10821939
10821945	10821954	10821981	10822014	10822018	10822088	10822115	10822196
10822206	10822293	10822320	10822357	10822362	10822556	10822580	10822677
10822704	10822776	10822780	10822865	10822950	10823103	10823131	10823388
10823551	10823740	10823750	10823809	10823832	10823929	10823966	10823989
10823994	10824117	10824248	10824260	10824372	10824412	10824523	10824538
10824548	10824569	10824958	10824967	10824976	10825023	10825091	10825125
10825224	10825257	10825349	10825564	10825603	10825669	10825733	10825865

Customer Service Request Numbers Resolved in the Quartus II Software Version 11.1							
10826114	10826172	10826216	10826251	10826336	10826371	10826598	10826652
10826709	10826760	10826837	10826895	10826935	10827048	10827069	10827076
10827243	10827252	10827313	10827336	10827426	10827436	10827563	10827643
10827687	10827693	10827799	10827814	10828177	10828372	10828478	10828658
10828675	10828791	10828798	10828900	10828982	10829165	10829219	10829266
10829311	10829386	10829390	10829479	10829570	10829610	10829886	10829991
10830018	10830109	10830131	10830478	10830534	10831141	10831220	10831643
10831910	10832065	10832068	10832732	10832898	10833054	10834168	10834276

Software Patches Included in this Release

The Quartus II software version 11.1 includes the following patches released for previous versions of the Quartus II software:

Quartus II Software Version	Patch	Customer Service Request Number
11.1FB	0.03a	—
11.1FB	0.02a	—
11.0SP2	2.sv3a	—
11.0SP2	2.04	10830478
11.0SP2	2.02	10827799
11.0SP2	2.01	10802946
11.0SP1	1.31	—
11.0SP1	1.30	10828478
11.0SP1	1.29	10821690
11.0SP1	1.28	10806318
11.0SP1	1.24	—
11.0SP1	1.23	10817154
11.0SP1	1.21	10819657
11.0SP1	1.20	10824372
11.0SP1	1.18	—
11.0SP1	1.16	10815150
11.0SP1	1.13	10822018
11.0SP1	1.11	10821686
11.0SP1	1.10	10822677

Quartus II Software Version	Patch	Customer Service Request Number
11.0SP1	1.07	10817064
11.0SP1	1.06	10817756
11.0SP1	1.05	10806318
11.0SP1	1.03	10810589
11.0	0.38	10824523
11.0	0.37	10806318
11.0	0.36	10828478
11.0	0.31	10820383
11.0	0.28	10822677
11.0	0.27	10821686
11.0	0.25	10822963
11.0	0.24	10806318
11.0	0.23	10817756
11.0	0.22	10810589
11.0	0.17	10814831
11.0	0.12	10803448
11.0	0.02	10806243
10.1SP1	1.93	10806318
10.1SP1	1.91	10818849
10.1SP1	1.90	10820636
10.1SP1	1.89	10817154
10.1SP1	1.86	10806318
10.1SP1	1.85	10810092
10.1SP1	1.80	10797641
10.1SP1	1.78	10811752
10.1SP1	1.50	10803448
10.1SP1	1.30	—
10.1	0.77	10830886
10.1	0.75	10797641
10.1	0.74	10807225
10.1	0.72	10803448
10.1	0.58	10793725

Quartus II Software Version	Patch	Customer Service Request Number
10.0	0.71	10810589
9.1SP2	2.138	10817154
9.1SP2	2.136	10797641
9.1SP2	2.134	10810911
9.1SP2	2.132	10810774

Document Revision History

The following table shows the revision history for this document.

Document Revision History

Date	Version	Changes
November 2011	1.0	Initial release.