Quartus II Software Version 11.1 Device Support

This document provides late-breaking information about device support in the Altera® Quartus® II software version 11.1. For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<*version number*>/quartus** directory. For information about new features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

This document contains the following sections:

Device Support and Pin-Out Status

This section contains information about the device support status in the Quartus II software version 11.1.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Table 1. Devices with Full Support

Device Family	Devices	
Stratix® V	5SGXEA7ES	5SGTMC7ES

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Advance Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in Table 2 that will be released in the near future. The Compiler generates pin-out information for these devices in this release, but does not generate programming files.

Table 2. Devices with Advance Support

Device Family	Devices	
Arria® V	5AGXBB1	5AGXBB3
	5AGXBB5	5AGXBB7
	5AGXFB1	5AGXFB3
	5AGXFB5	5AGXFB7
	5AGXFB3ES	5AGXMB1
	5AGXMB3	5AGXMB3ES
	5AGXMB5	5AGXMB7
Stratix V	5SGTMC5	5SGTMC7
	5SGXEA5	5SGXEA7
	5SGXEB5	5SGXEB6
	5SGXEB6ES	5SGXMA5
	5SGXMA7	5SGXMB5
	5SGXMB6	

Initial Information Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in Table 3 that will be released in upcoming versions of the Quartus II software. Programming files and pin-out information are not generated for these devices in this release.

Table 3. Devices with Initial Information Support

Device Family	Devices	
Cyclone® V	5CGXBC7	5CGXFC7
Stratix V	5SGSED6	5SGSED8
	5SGSMD3	5SGSMD4
	5SGSMD5	5SGSMD6
	5SGSMD8	5SGXEAB
	5SGXEA3	5SGXEA4
	5SGXEA9	5SGXMAB
	5SGXMA3	5SGXMA4
	5SGXMA9	

Memory Recommendations

A full installation of the Altera software requires up to 10 GB of available disk space on the drive or partition where you are installing the Altera software.

The Quartus II Stand-Alone Programmer requires a minimum of 1 GB of RAM plus additional memory, based on the size and number of **.sof** files and the size and number of devices being configured.

Altera recommends that your system be configured to provide virtual memory equal to the recommended physical RAM that is required to process your design.

Table 4 lists the memory required to process designs targeted for Altera devices.

Table 4. Memory Recommendations

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Arria GX	EP1AGX20	512 MB	512 MB
	EP1AGX35, EP1AGX50, EP1AGX60	1.0 GB	1.5 GB
	EP1AGX90	1.5 GB	2.0 GB
Arria II GX	EP2AGX45	1.0 GB	1.5 GB
	EP2AGX65	1.5 GB	2.0 GB
	EP2AGX95, EP2AGX125, EP2AGX190	3.0 GB	4.0 GB
	EP2AGX260	4.0 GB	6.0 GB
Arria II GZ	EP2AGZ225	3.0 GB	4.0 GB
	EP2AGZ300	4.0 GB	6.0 GB
	EP2AGZ350	N/A	8.0 GB
Arria V	5AGXB1	N/A	8.0 GB
	5AGXB3		
	5AGXB5		12.0 GB
	5AGXB7		
Cyclone	All	512 MB	512 MB
Cyclone II	EP2C5, EP2C8, EP2C15, EP2C20	512 MB	512 MB
	EP2C35, EP2C50	1.0 GB	1.5 GB
	EP2C70	1.5 GB	2.0 GB
Cyclone III	EP3C5, EP3C10, EP3C16, EP3C25, EP3C40	512 MB	512 MB
	EP3C55, EP3C80	768 MB	1.0 GB
	EP3C120	1.5 GB	2.0 GB

Table 4. Memory Recommendations (Continued)

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Cyclone III LS	EP3CLS70, EP3CLS100	1.5 GB	2.0 GB
	EP3CLS150, EP3CLS200	3.0 GB	4.0 GB
Cyclone IV E	EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, EP4CE40	512 MB	512 MB
	EP4CE55, EP4CE75	768 MB	1.0 GB
	EP4CE115	1.0 GB	1.5 GB
Cyclone IV GX	EP4CGX15, EP4CGX22, EP4CGX30	512 MB	512 MB
	EP4CGX50, EP4CGX75	1.0 GB	1.5 GB
	EP4CGX110, EP4CGX150	1.5 GB	2.0 GB
Cyclone V	5CGXC7	3.0 GB	4.0 GB
HardCopy® II	HC210, HC210W	1.5 GB	2.0 GB
	HC220, HC230, HC240	3.0 GB	4.0 GB
HardCopy III	HC325	N/A	8.0 GB
	HC335		12.0 GB
HardCopy IV	HC4E25	N/A	8.0 GB
	HC4GX15		12.0 GB
	HC4E35, HC4GX25		16.0 GB
	HC4GX35		20.0 GB
MAX®	All	512 MB	512 MB
MAX II	All	512 MB	512 MB
MAX V	All	512 MB	512 MB
Stratix	EP1S10, EP1S20	512 MB	512 MB
	EP1S25, EP1S30, EP1S40, EP1S60	1.0 GB	1.5 GB
	EP1S80	1.5 GB	2.0 GB
Stratix GX	EP1SGX10	512 MB	512 MB
	EP1SGX25, EP1SGX40	1.0 GB	1.5 GB
Stratix II	EP2S15	512 MB	512 MB
	EP2S30	1.0 GB	1.5 GB
	EP2S60, EP2S90	1.5 GB	2.0 GB
	EP2S130, EP2S180	3.0 GB	4.0 GB
Stratix II GX	EP2SGX30, EP2SGX60	1.0 GB	1.5 GB
	EP2SGX90	1.5 GB	2.0 GB
	EP2SGX130	3.0 GB	4.0 GB

Table 4. Memory Recommendations (Continued)

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Stratix III	EP3SL50, EP3SE50, EP3SL70	1.0 GB	1.5 GB
	EP3SE80	1.5 GB	2.0 GB
	EP3SL110, EP3SE110, EP3SL150, EP3SL200	3.0 GB	4.0 GB
	EP3SE260, EP3SL340	4.0 GB	6.0 GB
Stratix IV	EP4SGX70	1.5 GB	2.0 GB
	EP4SE230 EP4SGX110, EP4SGX230, EP4S40G2, EP4S100G2	3.0 GB	4.0 GB
	EP4SGX290	4.0 GB	6.0 GB
	EP4SE360 EP4SGX360, EP4S100G3, EP4S100G4	N/A	8.0 GB
	EP4SGX530, EP4SE530, EP4SE820, EP4S40G5, EP4S100G5	N/A	12.0 GB
Stratix V	5SGXA3, 5SGXA4, 5SGSD3, 5SGSD4, 5SGTC5	N/A	12.0 GB
	5SGXA5, 5SGXB5, 5SGSD5	N/A	16.0 GB
	5SGXA7, 5SGXB6, 5SGSD6, 5SGSD8, 5SGTC7	N/A	20.0 GB
	5SGXA9, 5SGXAB	N/A	24.0 GB
	5SEE9, 5SEEB	N/A	28.0 GB

Timing and Power Models

Table 5 lists a summary of timing and power model status in the current version of the Quartus II software.

Table 5. Devices with Timing and Power Models

Device Family	Device	Timing Model Status	Power Model Status
Arria II GX	EP2AGX45	Final – 10.0	Final – 10.0
	EP2AGX65		
	EP2AGX95		
	EP2AGX125		
	EP2AGX190	Final – 10.0 SP1	
	EP2AGX260		
Arria II GZ	All	Final – 10.1	Final – 10.1
Arria V	All	Preliminary	Preliminary
Cyclone III LS	EPC3LS70	Final – 10.0	Final – 10.0 SP1
	EPC3LS100		
	EPC3LS150		
	EPC3LS200		
Cyclone IV E	All 1.0V	Final – 10.0 SP1	Final – 10.0 SP1
	All 1.2V	Final – 10.0	
Cyclone IV GX	EP4CGX15	Final – 10.1	Final – 11.0
	EP4CGX22	Final – 11.0	
	EP4CGX30		Final – (1)
	EP4CGX50	Final – 11.0	Final –11.1
	EP4CGX75		
	EP4CGX110	Final – 10.1	Final – 11.0
	EP4CGX150		
Cyclone V	All	Preliminary	Preliminary
HardCopy III	All	Correlated – 11.1	Preliminary
HardCopy IV E	All	Correlated – 11.1	Preliminary
HardCopy IV GX	All	Correlated – 11.1	Preliminary
MAX V	All	Final – 11.0	Final – 11.0

Table 5. Devices with Timing and Power Models (Continued)

Device Family	Device	Timing Model Status	Power Model Status
Stratix IV	EP4SE230	Final – 9.1 SP1	Final – 10.0
	EP4SGX180		
	EP4SGX230		
	EP4S40G2		
	EP4S100G2		
	EP4SE360	Final – 9.1 SP2	
	EP4SE530		
	EP4SGX290		
	EP4SGX360		
	EP4SGX530		
	EP4S40G5		
	EP4S100G3		
	EP4S100G4		
	EP4S100G5		
	EP4SGX70	Final – 10.0	Final – 10.1
	EP4SGX110		
	EP4SE820	Final – 10.0 SP1	
Stratix V	All	Preliminary	Preliminary
(1) EP4CGX30BF14 and EP4CGX30CF19 are final in 11.0, EP4CGX30CF23 final in 11.1.			

The current version of the Quartus II software also includes final timing and power models for the Arria GX, Cyclone, Cyclone II, Cyclone III, HardCopy II, MAX, MAX II, MAX IIZ, Stratix, Stratix GX, Stratix II, Stratix II GX, and Stratix III device families. Timing models for these device families became final in the Quartus II software versions 9.0 and earlier.

Changes in Device Support

The following section is divided into device support changes according to whether the change is a notification, or whether the change has been fixed or not fixed.

Change Notifications

This section provides notifications for changes to devices.

Cyclone IV GX slew rate change

The transceiver slew rate settings are updated for Cyclone IV GX devices to meet specifications.

Applies to: Cyclone IV GX devices

Arria II GZ pin mark change

For Arria II GZ F1517 packages, the 24 pins listed were previously marked as GXB_NC in the Quartus II software pin file. These pins are now marked as NC and you should leave them unconnected.

The affected devices include EP2AGZ225HF40, EP2AGZ300HF40, and EP2AGZ350HF40. These are the Arria II GZ devices in the F1517 (F40) package.

Applies to: Arria II GZ devices

Stratix IV pin file changes

In pin files that are generated by the Quartus II software version 11.0, you can observe the following changes as compared to the previously generated pin files. The affected devices include Stratix IV EP4SGX290/360 FH29 devices and all Stratix IV GT devices. Certain pins that you could use in configuration mode only or for their JTAG functionality, now show the corresponding functions in the pin file. Previously, they appeared as the GND* pin. You might see similar changes in the Pin Planner. Only the reported names changed; the underlying functionality and the placement remain the same.

Applies to: Stratix IV devices

Final timing model change for Cyclone IV E

The fast corner timing model was updated to reflect a smaller minimum pulse width. This timing model update results in a higher f_{MAX} limit when analyzing under the fast corner operating condition. This fix will remove the false warning "minimum pulse width violation" in timing reports. If your design passes timing checks in existing designs, no action is required. Designs that do not pass all timing checks before this update should employ the necessary timing closure techniques to ensure all timing checks pass.

Applies to: Cyclone IV E devices

Device Support Not Fixed

For the latest known issues related to the Quartus II software, refer to the Knowledge Base:

http://www.altera.com/support/kdb/kdb-search.jsp

Arria V change to pin tables

Description

In the Quartus II software version 11.1, for Arria V devices 5AGXB3 and 5AGXB1 F1517 the pinouts have been changed as follows:

- R9 changed from NC to VccD
- T31 changed from NC to VccD
- U9 changed from NC to VccA
- V31 changed from NC to VccA

Workaround

This change only affects you if you plan to migrate your design from either an 5AGXB1 or 5AGXB3 device to either an 5AGXB7 or 5AGXB5 F1517 device. Without this change, when you migrate your design it will lack the four fractional PLLs. This change has no impact if you do not migrate your design.

Applies to Arria V devices

Negative pin location assignments not supported for MAX V LVDS pair

Description

The Quartus II software does not support pin location assignments for the negative pin of an LVDS pair for MAX V devices.

Workaround

Assign positive pins.

Applies to MAX V devices

ALTGXB not supported for Stratix GX designs

Description

The Quartus II software version 10.0 and later does not support creating or updating the ALTGXB megafunction for Stratix GX devices.

Workaround

Use an earlier version of the Quartus II software to create or update Stratix GX designs using the GXB transceivers.

Applies to Stratix GX devices