



Nios[®] II Release Notes



Contents

1 Introduction.....	3
2 Nios II 17.1 Release Notes.....	4
2.1 Nios II Processor IP 17.1 Release Notes.....	4
2.2 Nios II Embedded Design Suite 17.1 Release Notes.....	4
2.3 Embedded IP 17.1 Release Notes.....	4
3 Nios II 17.0 Release Notes.....	6
3.1 Nios II Processor IP 17.0 Release Notes.....	6
3.2 Nios II Embedded Design Suite 17.0 Release Notes.....	6
3.3 Embedded IP 17.0 Release Notes.....	6
4 Nios II 16.1 Release Notes.....	8
4.1 Nios II Processor IP 16.1 Release Notes.....	8
4.2 Nios II Embedded Design Suite 16.1 Release Notes.....	8
4.3 Embedded IP 16.1 Release Notes.....	9
5 Document Revision History for the 17.1 Release of Nios II.....	10



1 Introduction

These release notes cover the 16.1 through 17.1 releases for the Nios® II Embedded Design Suite (EDS), Nios II Processor IP, and Embedded Intellectual Property (IP) cores.

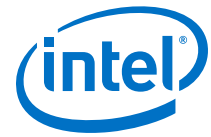
For more information about the Nios II Processor, refer to the "Nios II Processor" web page.

For other important information, refer to:

- The "Knowledge Base" web page on the Intel FPGA website to search for errata based on the product version affected.
- The "Nios II Embedded Design Suite Release Notes" web page to access archived versions of the Nios II Embedded Design Suite (EDS) Release Notes, Nios II Processor Release Notes, and Embedded IP Release Notes.

Related Links

- [Nios II Embedded Design Suite Release Notes \(Archived\)](#)
This web page contains previous versions of the Nios II Embedded Design Suite (EDS) Release Notes, Nios II Processor IP Release Notes, and Embedded Intellectual Property (IP) Release Notes.
- [Nios II Processor and EDS New Features](#)
- [Intel FPGA Knowledge Base](#)



2 Nios II 17.1 Release Notes

This section describes the new features, bug fixes, and enhancements for the 17.1 Nios II release.

2.1 Nios II Processor IP 17.1 Release Notes

New Features

Nios II processor IP support with Intel® Stratix® 10 and Intel Cyclone® 10 LP devices.

2.2 Nios II Embedded Design Suite 17.1 Release Notes

New Features

- Nios II Software Build Tools (SBT): Upgrade of Eclipse to v4.5 for Intel Quartus® Prime Pro Edition and Intel Quartus Prime Standard Edition
- New driver for Intel XWAY PHY11G PEF7071 Ethernet PHY for Intel Quartus Prime Pro Edition and Intel Quartus Prime Standard Edition
- Nios II Software Build Tools (SBT): Windows 10 host support in Intel Quartus Prime Pro Edition and Intel Quartus Prime Standard Edition software
- Nios II Toolchain upgrades for Intel Quartus Prime Pro Edition software:
 - gcc v6.3
 - binutils v2.26.51
 - gdb v7.11.1
 - newlib v2.4

Bug Fixes

- Issue causing locale to be broken on newlib 2.4.0 when using `smallc lib` fixed

Related Links

[Intel FPGA Knowledge Base](#)

2.3 Embedded IP 17.1 Release Notes

New Features

- mSGDMA optimizations for Intel Stratix 10 devices in Intel Quartus Prime Pro Edition software
- CMSIS support for embedded IP in Intel Quartus Prime Pro Edition software
- EPCQA device support for EPCQ Controller and Generic QSPI Controller IP in Intel Quartus Prime Standard Edition software

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Bug Fixes

- Intel Avalon® FIFO IP —Incorrect back pressure behavior during reset state and data loss when FIFO is almost full issue fixed

Enhancements

- Intel FPGA Triple-Speed Ethernet (TSE) iniche driver to support mSGDMA updated
- Redundant software example `simple_socket_server_rgmii` removed

Related Links

- [Intel FPGA Knowledge Base](#)
- [Embedded Peripherals IP User Guide](#)



3 Nios II 17.0 Release Notes

This section describes the new features, bug fixes, and enhancements for the 17.0 Nios II release.

3.1 Nios II Processor IP 17.0 Release Notes

New Features

- Added support for the Nios II processor in Intel Quartus Prime Pro Edition, and Platform Designer

3.2 Nios II Embedded Design Suite 17.0 Release Notes

Enhancements

- Nios II Software Build Tools (SBT)—Windows 10 support added in Intel Quartus Prime Pro Edition

3.3 Embedded IP 17.0 Release Notes

New Features

- Added new Streaming (Avalon-ST) Freeze Bridges for Partial Reconfiguration (PR) support
- New improved data performance Serial flash controller II and Generic Quad SPI controller II IPs
- Added Avalon-ST Freeze Bridges as PR solution IP
- All embedded IPs now support Intel Cyclone 10 device compilation

Bug Fixes

- I²C Slave to Avalon-MM Master—MM master write data corruption due to overrun of internal I²C slave RX shifting logic issue fixed
- Altera Avalon FIFO IP —Incorrect back pressure behavior during reset state and data loss when FIFO is almost full issue fixed
- EPCQ Controller—Incorrect back pressure behavior during reset state issue fixed



Enhancements

- Generic QSPI Controller IP:
 - Modified to enable support for multiple instances in one Platform Designer design
 - N25Q016 flash device now supported
- Serial Flash Controller IP—EPCS4 flash device now supported
- The following IP (from Standard version) are not present in the Pro version:
 - Altera Avalon New SDRAM Controller
 - Altera SDRAM Tristate Controller
 - Altera Avalon EPCS Flash Controller
 - Altera Avalon Compact Flash Controller
 - Altera Avalon Half Rate Bridge
 - Altera Avalon Pixel Converter
 - Altera Avalon Video Sync Generator
 - Altera Avalon LCD 16207
 - Altera Avalon SGDMA
 - Altera Avalon DMA
 - Altera Modular ADC
 - Altera SM Bus Controller

Related Links

- [Intel FPGA Knowledge Base](#)
- [Embedded Peripherals IP User Guide](#)



4 Nios II 16.1 Release Notes

This section describes the new features, bug fixes, and enhancements for the 16.1 Nios II release.

4.1 Nios II Processor IP 16.1 Release Notes

New Features

- The Nios II Processor is supported as a pre-release (beta) version in Intel Quartus Prime Pro Edition because of the changes required to support IP components in Platform Designer.
- Nios II Classic is no longer supported in Intel Quartus Prime Pro Edition.

4.2 Nios II Embedded Design Suite 16.1 Release Notes

New Features

- The GCC (Nios II) toolchain has been upgraded to version 5.3 (other upgrades include gdb binutils v2.25, gdb v7.10, newlib v2.2).

Bug Fixes

- The handling of the `-mgpopt=option` setting has been changed. It is now under the full control of the BSP editor and there is a flag for it in the `public.mk` file.
- `nios2-app-compile` no longer fails when `-mgpopt` is set to "global" and `loglevel` is set to "-1".

For more information about the GCC releases, refer to the GCC, the GNU Compiler Collection website.

Related Links

- [GCC, the GNU Compiler Collection website](#)
For more information about the GCC releases, refer to the *GCC, the GNU Compiler Collection* website.
- [Intel FPGA Knowledge Base](#)



4.3 Embedded IP 16.1 Release Notes

New Features

- A new IP core named Avalon I²C Master has been added to the Platform Designer (Standard) library.
- The 16550 UART IP has been enhanced to support a user-defined TX FIFO level trigger.
- Freeze controller and bridges IPs have been added to the IP library.

Related Links

[Embedded Peripherals IP User Guide](#)



5 Document Revision History for the 17.1 Release of Nios II

Date	Changes
February 2018	Added the new features, enhancements, and bug fixes for the 17.1 release of the Nios II Processor, Nios II EDS, and Embedded IP cores.
May 2017	Documented the new features and bug fixes for the 17.0 release of the Nios II Processor, Nios II EDS, and Embedded IP cores.
November 2016	Documented the new features and bug fixes for the 16.1 release of the Nios II Processor, Nios II EDS, and Embedded IP cores.
June 2016	Initial release of the combined Nios II release notes.

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