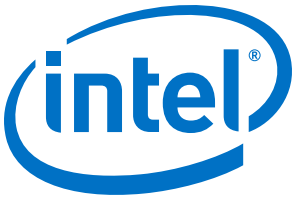

Intel SoC FPGA Embedded Development Suite Release Notes

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1 Intel SoC FPGA Embedded Development Suite (EDS) 17.1 Release Notes

These release notes cover the 17.0 through 17.1 releases of the system on chip (SoC) FPGA Embedded Development Suite (EDS) software.

These release notes are divided into two sections to cover the two editions offered in the 17.1 release.

2 SoC FPGA 17.1 Release Notes

2.1 SoC FPGA Pro Edition

The SoC FPGA Pro Edition targets the Intel Arria 10 SoC and must be used only with FPGA projects created in Intel Quartus Prime Pro Edition.

2.1.1 New Features for the 17.1 Release of the Pro Edition

This section describes the new features for the 17.1 release of the Pro Edition.

Golden Hardware Reference Design (GHRD)

- Upgraded the `sysid` component so that it is Platform Designer compatible
- Added soft IP to support CMSIS
- Cyclone V SoC:
  - Added SoCEDS 17.1 flash support

Bootloader

- Intel Arria 10 SoC U-Boot
  - Added support for semihosting

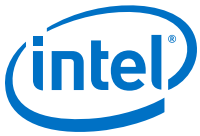
2.1.2 Bug Fixes for the 17.1 Release of the Pro Edition

Arm* Development Studio 5* (DS-5*) Intel SoC FPGA Edition

- Altera-SoCFPGA-HelloWorld-Baremetal-ARMClang software example imports correctly

Bootloader Generator and Bootloader

- Fixed various Coverity critical security warning including U-Boot common code
- UEFI
  - `git_clone.sh` script no longer fails
  - UART output distortion issue fixed



Toolchains

- SoCEDS Toolchains
  - Arm* Development Studio 5* (DS-5*) Intel SoC FPGA Edition
    - Altera-SoCFPGA-Push-Button-Linux-GNU project build no longer fails
  - Updated build configuration so that the SoC EDS Hello World Baremetal project no longer fails

2.1.3 Enhancements for the 17.1 Release of the Pro Edition

This section describes the enhancements for the 17.1 release of the Pro Edition.

Bootloader

- Enhanced U-boot to support 2GB SDRAM

Pro Edition Tool Version Updates

Tools	Version
Arm Development Studio 5 Intel SoC FPGA Edition	5.27.1
Arm Compiler 5	5.06 update 5
Arm Compiler 6	6.7.1
Linux Compiler	4.8.3 (Linaro GCC 4.8-2014.04)
Linux Kernel	4.1.33-ltsi
Mentor Graphics* Baremetal GCC Compiler	6.2.0

2.2 SoC FPGA Standard Edition

The SoC FPGA Standard Edition targets the Cyclone V SoC, Arria V SoC and Intel Arria 10 SoC, and must to be used only with FPGA projects created in Intel Quartus Prime Standard Edition.

2.2.1 New Features for the 17.1 Release of the Standard Edition

This section describes the new features for the 17.1 release of the Standard Edition release.

Golden Hardware Reference Design (GHRD)

- Cyclone V SoC:
  - Added SoCEDS 17.1 flash support

Toolchains

- Upgraded Baremetal GCC Compiler version to 6.2.0

2.2.2 Bug Fixes for the 17.1 Release of the Standard Edition

This section describes the bug fixes for the 17.1 release of the Standard Edition.

Toolchains

- SoCEDS Toolchains
  - Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition
    - Altera-SoCFPGA-Push-Button-Linux-GNU project build no longer fails
  - Upgrading to GCC v6.2.0 U-Boot compile errors fixed
- Nios2HAL EDS
  - Intel Avalon® FIFO IP —Incorrect back pressure behavior during reset state and data loss when FIFO is almost full issue fixed

2.2.3 Enhancements for the 17.1 Release of the Standard Edition

This section describes the enhancements for the 17.1 release of the Standard Edition.

Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition

- Updated Arm DS-5 Intel SoC FPGA Edition version to 5.27.1 to match Pro Edition

Bootloader

- Cyclone V U-Boot
  - Updated to support Mentor Graphics Baremetal GCC Compiler, version 6.2.0

Toolchains

- Nios2EDS Toolchains
  - TSE/iniche driver to support msgdma updated to match the support provided in the Pro edition

Hardware Libraries (HWLIBs)

- Updated QSPI code

Standard Edition Tool Version Updates

Tools	Version
Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition	5.27.1
Arm Compiler 5	5.06 update 5
Arm Compiler 6	6.7.1
Linux Compiler	4.8.3 (Linaro GCC 4.8-2014.04)
Linux Kernel	4.1.33-ltsi
Mentor Graphics Baremetal GCC Compiler	6.2.0

3 SoC FPGA 17.0 Release Notes

3.1 SoC FPGA Pro Edition

Since the Pro Edition was new for 17.0, this section describes only the new features for this release of the Pro Edition.

3.1.1 New Features for the 17.0 Release of the Pro Edition

Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition

- Includes Arm Development Studio 5 Intel SoC FPGA Edition version 5.26.2
- Baremetal cheat sheets added

SoC FPGA Embedded Software

- Linux Device Tree Generator (DTG)—Support added for TSE SGMII PCS.
- SOPC2DTS—Device Tree Compiler (DTC) no longer fails when the Display Port (DP) is initiated.

Bootloader Generator and Bootloader

- Intel Arria 10 U-Boot
  - — I^2C driver is enabled
  - — FPGA boot is enabled
  - — Support for GCC6 is enabled
  - — Multiport front end (MPFE) no longer hangs due to the transient clock
  - — MAC address retrieved from EEPROM is enabled
  - — SDRAM support up to 2 GB is enabled
  - — SDRAM no longer fails initialization when ECC is enabled
- Intel Arria 10 UEFI
  - — Bad block marker implementation is no longer incorrect
  - — MPFE no longer hangs due to the transient clock
  - — NoC MPFE HPS lock issue fixed
  - — Coverity static analysis security no longer generates a warning
  - — Ability to setup the MAC address from an EEPROM value

Linux Device Tree Generator (DTG)

Intel Arria 10 SoC:

- Triple Speed Ethernet (TSE) reference design hardware failure fixed

Golden Hardware Reference Design (GHRD)/Golden System Reference Design (GSRD)

- Intel Arria 10 DisplayPort GSRD hardware design - Display Port with terminal support enabled
- Intel Arria 10 GHRD—Setup timing violation for PCIe Gen2x8, Gen3x4, and Gen3x8 fixed.
- GHRD Partial Reconfiguration (PR)—Default value for the Display Port is no longer causing a generation/compilation issue.
- Resolution updated to 640x480 to fix the blanking issue observed by the DP Linux driver.
- Kernel 4.1.33-LTSI upgraded
- Intel Arria 10 DisplayPort GHRD—Resolution updated from 640x480 to 1280x720.

Toolchains

- Includes A53 Compiler (64-bit support)
- Upgraded Baremetal GCC Compiler version to 6.2.0
- Fixed the Baremetal GCC Compiler newlib error

Hardware Libraries (HWLIBs)

- Intel Arria 10
  - SDRAM example removed
- Arria V MPL
  - Size reduced to allow compiling
- Compiling errors no longer cause UEFI tests to fail
- MPL issues pertaining to SD/MMC boot corrected

3.2 SoC FPGA Standard Edition

This section describes the new features, bug fixes, and enhancements for the 17.0 release of the Standard Edition.

3.2.1 New Features for the 17.0 Release of the Standard Edition

Bootloader Generator and Bootloader

Intel Arria 10 U-Boot

- Enabled I^2C driver
- Enabled support for GCC6
- Enabled FPGA boot

3.2.2 Bug Fixes for the 17.0 Release of the Standard Edition

Bootloader Generator and Bootloader

- **Intel Arria 10 U-Boot**
  - Network-on-chip (NoC) MPFE Hard Processor System (HPS) lock issue fixed
- **Intel Arria 10 UEFI**
  - NoC MPFE HPS lock issue fixed
  - MPFE hang issue due to transient clock fixed
  - Wrong bad block marker implementation fixed
  - Coverity static analysis security warning fixed

Golden Hardware Reference Design (GHRD)

- Intel Arria 10 GHRD—HPS SGMII design build no longer fails `qsys-script` when receiving an invalid parameter from the transceiver PLL.
- `soc_system_board_info.xml` file updated to remove outdated information for the Arria V amd Cyclone V SoC Development Kits

Hardware Libraries (HWLIBs)

- Arria V MPL
  - Size reduced for armcc
- `snprintf` defined
- Design example in GHRD now blinks LED
- `mpl/boot-baremetal-fpga` tests no longer fails
- Compiling errors no longer cause UEFI tests to fail
- HWLib DMA test from OCRAM to SDRAM no longer fails

3.2.3 Enhancements for the 17.0 Release of the Standard Edition

Bootloader Generator and Bootloader

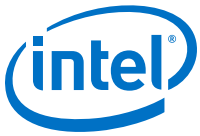
- Intel Arria 10 U-Boot
  - Enabled MAC address retrieved from EEPROM
  - Enabled SDRAM support up to 2 GB
- Intel Arria 10 UEFI—Ability to setup the MAC address from an EEPROM value.

Hardware Libraries (HWLIBs)

- MPL updated
- SDRAM files updated

3.2.4 Known Issues for the 17.0 Release of the Standard and Pro Editions

This section describes the known issues for the 17.0 release of the Standard and Pro Editions.



17.0 Known Issues for Standard Edition

Table 1. SDRAM ECC not Supported in Early IO Boot

Description	The SDRAM ECC is not supported in Early IO release boot because DDR calibration failed after the peripheral RBF was programmed to the FPGA.
Workaround	No workaround. This does not impact the non Early IO release boot.

Table 2. Intel Baremetal Folder Unavailable in SoCEDS-Arm DS-5 Intel SoC FPGA Edition CheatSheet

Description	The DS-5 Intel SoC FPGA Edition tool has been updated to have cheat sheets for Intel Baremetal development. In some cases, the Linux version does not display these cheat sheets.
Workaround	Invoking Arm DS-5 Intel SoC FPGA Edition using `sudo` may allow the cheatsheets to appear.

4 Document Revision History for the 17.1 Release of the Standard and Pro Editions

Table 3. Document Revision History for the 17.1 Release

Version	Changes
2017.12.05	Added new features, bug fixes, enhancements, and known issues during the 17.1 release of the SoC FPGA EDS software - Standard and Pro editions.
2017.05.08	Release Notes divided into a Pro and Standard section.
2016.11.07	Added clarity to the early IO release feature.
2016.05.09	16.0 release updates
2016.01.22	15.1.1 release updates
2015.11.02	15.1 release updates
2015.06.05	15.0.1 release updates
2015.05.01	15.0 release updates