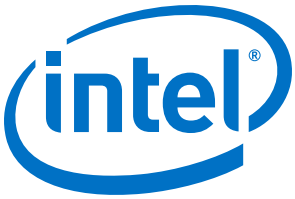

Intel SoC FPGA Embedded Development Suite Release Notes

RN-SOCEDS
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Contents

1 Intel SoC FPGA Embedded Development Suite Release Notes

These release notes cover version 16.1 through version 17.0 for the release of the system on chip (SoC) FPGA Embedded Development Suite (EDS) software.

These release notes are divided into two sections to cover the two editions—Professional (Pro) and Standard (Std)— offered in the 17.0 release.

Related Links

SoC Embedded Design Suite Support Page

1.1 SoC FPGA EDS Standard Edition Revision History

The SoC FPGA Standard Edition targets the Intel Cyclone® V SoC, Intel Arria® V SoC and Intel Arria 10 SoC, and must be used only with FPGA projects created in Quartus® Prime Standard Edition.

1.1.1 New Features

This section describes the new features for the 17.0 release.

Bootloader Generator and Bootloader

Arria 10 U-Boot

- Enabled I^2C driver
- Enabled FPGA boot
- Enabled support for GCC6

1.1.2 Bug Fixes

This section describes the bug fixes for the 17.0 release.

Bootloader Generator and Bootloader

- Arria 10 U-Boot
  - — Network-on-chip (NoC) MPFE Hard Processor System (HPS) lock issue fixed
- Arria 10 UEFI
  - — NoC MPFE HPS lock issue fixed
  - — MPFE no longer hangs due to the transient clock[1]
  - — Wrong bad block marker implementation fixed
  - — Coverity static analysis security warning fixed

Golden Hardware Reference Design (GHRD)

- Arria 10 GHRD—HPS SGMII design build no longer fails `qsys-script` when receiving an invalid parameter from the transceiver PLL
- `soc_system_board_info.xml` file updated to remove outdated information for the Arria V amd Cyclone V SoC Development Kits

Hardware Libraries (HWLIBs)

- Arria V MPL
  - Size reduced for armcc
- `snprintf` defined
- Design example in GHRD now blinks LED
- `mpl/boot-baremetal-fpga` tests no longer fails
- Compiling errors no longer cause UEFI tests to fail
- HWLib DMA test from OCRAM to SDRAM no longer fails

Related Links

SoC FPGA EDS v. 16.1 Release Notes on page 7
This section lists the revision history from the previous release of the SoC FPGA EDS software.

1.1.3 Enhancements

This section describes the enhancements for the 17.0 release.

Bootloader Generator and Bootloader

- Arria 10 U-Boot
  - Enabled MAC address retrieved from EEPROM
  - Enabled SDRAM support up to 2 GB
- Arria 10 UEFI—Ability to setup the MAC address from an EEPROM value

Hardware Libraries (HWLIBs)

- MPL updated
- SDRAM files updated

1.1.4 Known Issues

This section describes the known issues for the 17.0 release.

1 For more information about the issue that was fixed, refer to Table 3 on page 10 in the "Release Notes for 16.1" section.

17.0 Known Issues

Table 1. SDRAM ECC not Supported in Early IO Boot

Description	The SDRAM ECC is not supported in Early IO release boot because DDR calibration failed after the peripheral RBF was programmed to the FPGA.
Workaround	No workaround. This does not impact the non Early IO release boot.

Table 2. Altera Baremetal Folder Unavailable in SOCEDS-DS5 CheatSheet

Description	The DS-5 tool has been updated to have cheat sheets for Altera Baremetal development. In some cases, the Linux version does not display these cheat sheets.
Workaround	Invoking DS-5 using `sudo` may allow the cheatsheets to appear.

Related Links

- Stack Overflow Question and Answer
  How to run eclipse in clean mode? and what happens if we do so?
- RocketBoards Documentation Portal

1.2 SoC FPGA EDS Pro Edition Revision History

The SoC FPGA EDS Pro Edition targets the Arria 10 SoC, and must be used only with FPGA projects created in Quartus Prime Pro Edition. **Note:** The SoC FPGA Pro Edition does not support Cyclone V SoC and Arria V SoC, as they are not supported by Intel Quartus Prime Pro Edition.

The following section will describe "What's New" for this first installment of the Pro Edition.

Related Links

SoC FPGA EDS v. 16.1 Release Notes on page 7
This section lists the revision history from the previous release of the SoC FPGA EDS software.

1.2.1 What's New in the Pro Edition

ARM Development Studio 5 (DS-5) SoC FPGA Edition

- Includes ARM DS-5 SoC FPGA Edition version 5.26.2
- Baremetal cheat sheets added

SoC FPGA Embedded Software

- Linux Device Tree Generator (DTG)—Support added for TSE SGMII PCS

Bootloader Generator and Bootloader

- Arria 10 U-Boot
  - — I^2C driver is enabled
  - — FPGA boot is enabled
  - — Support for GCC6 is enabled
  - — Multiport front end (MPFE) no longer hangs due to the transient clock[2]
  - — MAC address retrieved from EEPROM is enabled
  - — SDRAM support up to 2 GB is enabled
  - — SDRAM no longer fails initialization when ECC is enabled
- Arria 10 UEFI
  - — Bad block marker implementation is no longer incorrect
  - — MPFE no longer hangs due to the transient clock
  - — NoC MPFE HPS lock issue fixed
  - — Coverity static analysis security no longer generates a warning
  - — Ability to setup the MAC address from an EEPROM value

Linux Device Tree Generator (DTG)

- Arria 10 SoC
  - — Triple Speed Ethernet (TSE) reference design hardware failure fixed

Golden Hardware Reference Design (GHRD)/Golden System Reference Design (GSRD)

- Arria 10 DisplayPort GSRD hardware design - Display Port with terminal support enabled
- Arria 10 GHRD—Setup timing violation for PCIe Gen2x8 fixed
- Kernel 4.1.33-LTSI upgraded

Toolchains

- Upgraded Baremetal GCC Compiler version to 6.2.0
- Fixed the Baremetal GCC Compiler newlib error

Hardware Libraries (HWLIBs)

- Arria 10
  - — SDRAM example removed
- Arria V MPL
  - — Size reduced to allow compiling
- MPL issues pertaining to SD/MMC boot corrected

2 For more information about the issue that was fixed, refer to Table 3 on page 10 in the "Release Notes for 16.1" section.

1.3 SoC FPGA EDS v. 16.1 Release Notes

This section lists the revision history from the previous release of the SoC FPGA EDS software.

New Features

ARM Development Studio 5 SoC FPGA Edition

- Includes ARM DS-5 SoC FPGA Edition version 5.25
- Support for Aarch64 Linux application debug
- Cross triggering support with AMP debug

Bootloader Generator and Bootloader

- Arria 10 U-Boot
  - Supported eMMC 4.41 and 5.0
  - Supported NAND flash devices
  - Supported dual stake QSPI flash S70FL01GS, which consist of two S25FL512S dies
  - Supported early IO release, which enables faster boot time by loading the HPS subsystem first before the core RBF is loaded
  - Enabled Ethernet support when boot from NAND
  - Checksum checking on FPGA image which loads from the SD/MMC when the macro **CONFIG_CHECK_FPGA_DATA_CRC** is defined is enabled
- Arria 10 UEFI
  - UEFI is integrated into SOCEDS 16.1 for the first time
  - Added LCD UEFI Application for Arria 10 Development Kit
  - Added EEPROM UEFI Application for Arria 10 Development Kit
  - Enabled checksum check of FPGA image
  - Removed the duplicated HWLib files within UEFI source. The Makefile was modified to be able to copy HWLib from SoCEDS when building UEFI
- Arria 10 Bootloader Generator Support for:
  - NAND boot—Enables designs to boot from NAND Flash
  - UEFI Bootloader—Supports generation of UEFI bootloader image
  - Early IO release

Linux Device Tree Generator (DTG)

- Linux build
  - Support for building Linux 4.1 LTSI kernel

Golden Hardware Reference Design (GHRD) / Golden System Reference Design (GSRD)

- Arria 10 GHRD that demonstrates Partial Reconfiguration
- Arria 10 NAND reference design
- Angstrom v2015.12 upgrade for SoC reference designs
- Kernel 4.1.22-LTSI upgrade for SoC reference designs

Toolchains

- Nios2EDS Toolchains
  - Includes GCC Compiler version 5.3
  - Nios II Embedded Design Suite (EDS) is in Beta support when used with Qsys Pro[3]
- SoCEDS Toolchains
  - Includes ARM Compiler (DS-5 native)
    - ARM Compiler 6 version 6.5
    - ARM Compiler 5 version 5.06u3
  - Includes Bare Metal (Code Sourcery)
    - GCC Compiler version 5.2
  - Includes Linux (DS-5 native)
    - GCC Compiler version 4.8

General

- Windows 10
  - Support for Windows 10 host
- Arria 10 Partial Reconfiguration (PR) Support
  - Tools support generation of Arria 10 PR reference design[4]
- Prebuilt images upgraded to support Linux 4.1LTSI and Angstorm 2015.12

Bug Fixes

Bootloader Generator and Bootloader

3 Full support becomes available in 17.0.

4 Full support in 17.0

- Arria 10 U-Boot
  - Issue with U-Boot hanging when using UART in shared I/O fixed
  - Issue with serial port console in U-Boot with NAND for external FPGA configured by host and HPS fixed
  - PLL ramp code to support use case for a 1:2 ratio of the MPU clock: NOC clock fixed
  - Correct Linux DTB board filename for Arria 10 ensured
- SoC Preloader Generator
  - Cyclone V® HPS double data rate 3 (DDR3) no longer has varying DQS pulse levels during reads
- Arria 10 UEFI
  - Duplicated HWLib files within UEFI source removed[5]
  - Created `HwLib.inf` for a more stable UEFI application
  - DXE console hanging when DMA is enabled fixed
  - UEFI NAND unable to boot from BootROM fixed
  - Ability to build from a generated makefile in Windows fixed
- Cyclone V Preloader
  - Stable low power double data rate 2 (LPDDR2) operation ensured
- Cyclone V and Arria V Preloader
  - Divide by zero issue fixed

Linux Device Tree Generator (DTG)

- DTG for Triple Speed Ethernet (TSE) Serial Gigabit Media Independent Interface (SGMII) driver updated

Hardware Libraries (HWLIBs)

- `HWLIBS_ROOT` define fixed
- **BOOT_FROM_FPGA** added to `config.mk`
- MPL Makefile for **BOOT_FROM_FPGA** updated
- MPL Makefile for the **LOAD_FPGA** default change
- Cyclone V and Arria V MPL:
  - Option for **mkpimage** added for Minimal Preloader (MPL)
- Arria 10 MPL
  - `mpl_a10.c` no longer re-defines **FAT_BOOT**
- UEFI HWLIBs changes are now integrated into the mainline HWLIBs
- New MPL warnings eliminated
- Watchdog timer in QSPI boot disabled
- Clock print for QSPI updated
- Delay between initializing and reading in QSPI increased

5 Makefile was modified to be able to copy HWLib from SoCEDS when building UEFI.

Enhancements

Bootloader Generator and Bootloader

- Arria 10 U-Boot
  - Memory consumption of on-chip RAM is reduced due to buffer reduction and relocation of stack and heap to SDRAM
  - SDMMC sample select value based on the characterization result updated
  - Clock configuration code was changed to avoid potential PLL
  - Performance of loading RBF data from flash was greatly improved by using a large buffer in DDR
  - Security and firewall settings disabled to simplify board bring up
  - `CONFIG_CMD_NAND_TRIMFFS` enabled so that U-Boot can write an image formatted by **mkfs.jffs2** that Linux can use for a root file system without reporting lots of ECC errors
- Arria 10 UEFI
  - Implemented bad block management to:
    - Scan bad blocks
    - Read, write, erase, and skip bad blocks
    - Read raw and spare data
- Implemented the NAND TRIMFFS feature which skips writing all trailing 0xFF pages from an erase block. This is to prevent the RFS 'get' ECC error in the Linux console
- Added PitStop support to program **periph** and combined RBF

Golden Hardware Reference Design (GHRD) / Golden System Reference Design (GSRD)

- Increased the Arria10 HPS VCCL from 0.90 V to 0.95 V in the Qsys design according to latest characterization result

Known Issues

Table 3. Why Does My Arria 10 SoC Design Hang in Bootloader or When Accessing FPGA-to-SDRAM Bridge?

Description	Due to a hardware problem, Arria 10 SoC devices may hang in bootloader, during or after bringing up the SDRAM, or when accessing FPGA-to-SDRAM bridge. The hang can occur: • When accessing SDRAM Interconnect • When accessing SDRAM memory The issue is very rare, and can occur after power on, cold and warm resets.
Workaround	The problem is fixed in the SoC FPGA EDS version 17.0 which is available for download on the "Download Center" web page. A patch for SoC EDS version 16.1 can also be made available upon request.

Table 4. Early IO Release with Secure boot FPGA Key Use Case

Description	When you program the EKP file and then program the SOF[6], U-Boot successfully programs encrypted periph RBF, but it is unable to program encrypted core RBF.
Workaround	Program the FPGA with EKP then SOF, through Quartus Programmer.

Table 5. Reconfiguration of Periph and Combined RBF Does Not work at U-Boot Console

Description	Because the SDRAM memory is being utilized for huge stacks in malloc, it wipes off the SDRAM causing the reconfiguration of periph and combined RBF to fail.
Workaround	There is no workaround because the default use case is to free up more memory in U-Boot.

Table 6. Root File System Needs the `mtd_utils` Capable of Formatting a jffs2 File System in NAND for Arria 10

Description	Running `flash_erase` using the jffs2 argument in NAND for Arria 10 returns an error message.
Workaround	Refer customers to RocketBoards for information on how to apply the `mtd_utils` patch.

Table 7. For A10 MPL, QSPI Fails to Proceed to the Next Stage Load Due to QSPI not in Idle State

Description	When the MPL is configured to boot from QSPI, it fails to proceed further to load next stage image because the logic implemented to check for QSPI idle state is not appropriate. If you use the provided delay or even an increased delay, QSPI not idle is also returned, which aborts the BOOT sequence.
Workaround	Since there is not an option to have a single monolithic RBF in the not_shipped QSPI design, during the build process, you must replace that entry with a real QSPI design.

Table 8. Arria 10 UEFI Bootloader Does Not Support eMMC

Description	Using an eMMC card causes boot issues.
Workaround	There is no workaround; however, the fix is in an upcoming release.

Table 9. Arria 10 Windows MPL Builds Do Not Compile

Description	Arria 10 Windows MPL build do not compile.
Workaround	There is no workaround; however, the fix is in an upcoming release.

Table 10. Cyclone V and Arria V Build for ARMCC is Broken

Description	In some cases, when you have certain features of MPL turned on at the same time, an error message occurs.
Workaround	There is no workaround; however, the fix is in an upcoming release.

6 The SOF contains a signing key in the FPGA OCRAM.

Table 11. MPL-RAW SDMMC Next Stage Image Load in Memory Logic is Incorrect

Description	When the MPL is configured to boot from SDMMC; and both the MPL image and the next stage image are written in RAW mode (RAW partition), the next stage fails to execute and a CRC Error is generated.

Workaround	Edit the loop condition in the MPL source code: `sdmmc_load.c`:
	`for (int i = IMG_HDR_SZ;`
	`  i < (img_hdr_p->img_size);`
	`  i += sizeof(uint32_t));`
	Either start the loop from zero or add the **IMG_HDR_SZ** size to `img_hdr_p->img_size`.

Table 12. Altera-SOCFPGA-HelloWorld-Baremetal-ARMCC for Arria10 runtime error

Description	`Altera-SOCFPGA-HelloWorld-Baremetal-ARMCC` has a runtime error although the Makefile has BOARD set to `arria10`.
Workaround	In the project, change the value in **Properties ➤ C/C++ Build Settings ➤ ARMLinker ➤ Image Layout** to `arria10_scatter.scat`.

Related Links

- Intel FPGA Download Center web page
- Intel FPGA Knowledge Base

1.4 Document Revision History

Table 13. Document Revision History

Date	Version	Changes
May 2017	2017.05.08	17.0 release updates
November 2016	2016.11.07	16.1 release updates
May 2016	2016.05.09	16.0 release updates
January 2016	2016.01.22	15.1.1 release updates
November 2015	2015.11.02	15.1 release updates
June 2015	2015.06.05	15.0.1 release updates
May 2015	2015.05.01	15.0 release updates