Contents

1 Introduction to the SoC FPGA Embedded Development Suite ................................................................. 4
  1.1 Differences Between Standard and Professional Editions ................................................................. 4
  1.2 Overview ........................................................................................................................................ 5
    1.2.1 Linux Device Tree Binary ......................................................................................................... 7
  1.3 Hardware and Software Development Roles ....................................................................................... 7
    1.3.1 Hardware Engineer .................................................................................................................. 8
    1.3.2 Bare-Metal and RTOS Developer ............................................................................................. 8
    1.3.3 Linux Kernel and Driver Developer ........................................................................................ 9
    1.3.4 Linux Application Developer .................................................................................................. 9
  1.4 Hardware – Software Development Flow .......................................................................................... 9
  1.5 Introduction to the SoC FPGA EDS Document Revision History ....................................................... 10

2 Installing the SoC FPGA EDS .................................................................................................................. 11
  2.1 Installation Folders .......................................................................................................................... 11
  2.2 Installing the SoC FPGA EDS on Windows ......................................................................................... 11
  2.3 Installing the ARM DS-5 Intel SoC FPGA Edition Toolkit ................................................................. 12
  2.4 Installing the SoC FPGA EDS Document Revision History .............................................................. 12

3 Licensing ............................................................................................................................................... 14
  3.1 Getting the License .......................................................................................................................... 14
  3.2 Activating the License ...................................................................................................................... 15
  3.3 Licensing for the SoC FPGA EDS Document Revision History ....................................................... 20

4 Embedded Command Shell .................................................................................................................. 22
  4.1 Embedded Command Shell Document Revision History .................................................................. 22

5 Getting Started Guides ......................................................................................................................... 23
  5.1 Getting Started Guides Document Revision History ....................................................................... 23

6 ARM Development Studio 5 for Intel SoC FPGAs .................................................................................. 24
  6.1 Starting Eclipse ARM DS-5 for Intel SoC FPGA Edition .................................................................. 24
  6.2 Bare-Metal Project Management ....................................................................................................... 25
    6.2.1 Bare-Metal Project Management Using Makefiles ................................................................... 25
    6.2.2 GCC-Based Bare-Metal Project Management ......................................................................... 28
    6.2.3 ARM Compiler Bare-Metal Project Management .................................................................. 32
  6.3 Debugging ....................................................................................................................................... 40
    6.3.1 Accessing Debug Configurations ............................................................................................ 40
    6.3.2 Creating a New Debug Configuration ...................................................................................... 40
    6.3.3 Debug Configuration Options .................................................................................................. 42
    6.3.4 DTSL Options .......................................................................................................................... 51
  6.4 ARM DS-5 for Intel SoC FPGA Edition Document Revision History ................................................ 55

7 Boot Tools User Guide .......................................................................................................................... 56
  7.1 Introduction ....................................................................................................................................... 56
  7.2 Second Stage Bootloader Support Package Generator .......................................................................... 57
    7.2.1 BSP Generation Flow ............................................................................................................... 57
    7.2.2 BSP Generator Graphical User Interface ................................................................................. 60
    7.2.3 BSP Generator Command Line Interface ............................................................................... 61
    7.2.4 BSP Files and Folders .............................................................................................................. 64
7.2.5 BSP Settings................................................................. 64
7.3 Second Stage Bootloader Image Tool (mkpimage).................. 73
  7.3.1 Operation................................................................. 73
  7.3.2 Header File Format.................................................. 74
  7.3.3 Tool Usage.............................................................. 75
  7.3.4 Output Image Layout................................................. 76
7.4 U-Boot Image Tool (mkimage)........................................... 78
  7.4.1 Tool Options.......................................................... 78
  7.4.2 Usage Examples..................................................... 79
7.5 Building the Second Stage Bootloader........................................ 79
  7.5.1 Building the Cyclone V and Arria V Preloader................. 79
  7.5.2 Building the Arria 10 Bootloader.............................. 80
7.6 Boot Tools User Guide Document Revision History................ 82

8 Hardware Library........................................................................... 83
  8.1 Feature Description...................................................... 84
    8.1.1 SoC Abstraction Layer (SoCAL)............................... 84
    8.1.2 Hardware Manager (HW Manager)............................ 85
  8.2 Hardware Library Reference Documentation........................ 85
  8.3 System Memory Map................................................... 85
  8.4 Hardware Library Document Revision History.................... 86

9 HPS Flash Programmer User Guide................................................. 87
  9.1 HPS Flash Programmer Command-Line Utility..................... 87
  9.2 How the HPS Flash Programmer Works.............................. 87
  9.3 Using the Flash Programmer from the Command Line............. 88
    9.3.1 HPS Flash Programmer............................................. 88
    9.3.2 HPS Flash Programmer Command Line Examples............... 89
  9.4 Supported Memory Devices............................................ 90
  9.5 HPS Flash Programmer User Guide Document Revision History... 91

10 Bare-Metal Compilers................................................................. 92
  10.1 Mentor Code Sourcery Compiler..................................... 92
  10.2 Bare-Metal Compilers Document Revision History.............. 93

11 SD Card Boot Utility............................................................... 94
  11.1 Usage Scenarios........................................................ 94
  11.2 Tool Options............................................................ 95
  11.3 SD Card Boot Utility Document Revision History................ 96

12 Linux Software Development Tools........................................... 97
  12.1 Linux Compiler........................................................... 97
  12.2 Linux Device Tree Generator........................................ 98
  12.3 Linux Software Development Tools Document Revision History 98

13 Support and Feedback............................................................. 99
  13.1 Support and Feedback Document Revision History............... 99
1 Introduction to the SoC FPGA Embedded Development Suite

The Intel® FPGA system on a chip (SoC) Embedded Development Suite (EDS) is a comprehensive tool suite for embedded software development on Intel FPGA SoC devices.

The SoC FPGA EDS contains development tools, utility programs, run-time software, and application examples that enable firmware and application software development on Intel SoC hardware platforms.

The SoC FPGA EDS is offered in two editions:

- **Standard Edition**—The SoC FPGA EDS Standard Edition targets the Intel Cyclone® V SoC, Intel Arria® V SoC and Intel Arria 10® SoC, and must be used only with FPGA projects created in Quartus® Prime Standard Edition. Although the SoC FPGA and Intel Quartus Prime Standard Edition support Arria 10 SoC, it is recommended to use the Professional (Pro) editions of both tools for new Arria 10 SoC Projects.

- **Professional (Pro) Edition**—The SoC FPGA EDS Pro Edition targets the Arria 10 SoC and must be used only with FPGA projects created in Quartus Prime Pro Edition.

  *Note:* The SoC FPGA Pro Edition does not support Cyclone V SoC and Arria V SoC, as they are not supported by Intel Quartus Prime Pro Edition.

**Related Links**

- SoCEDSGettingStarted
  For more information about getting started, refer to the SoCEDSGettingStarted page on the Intel FPGA Wiki.

- Licensing on page 14

1.1 Differences Between Standard and Professional Editions

The main difference between the two different editions exists in the SoC devices that are supported, as mentioned in the previous section.

The additional differences between the SoC FPGA EDS Standard Edition and the SoC FPGA EDS Professional Edition are described below. Use the table to determine the current tool versions.

Things to know about installation and licensing for the two editions:
The default installation paths are different between editions. For details on the default installation paths, refer to the "Installing the SoC FPGA EDS" chapter.

There are no licensing differences between SoC FPGA EDS editions. The same DS-5 Intel SoC FPGA Edition License will work for both Standard and Pro editions. For details about licensing, refer to the "Licensing" chapter.

**Table 1. Differences Between Standard and Professional Editions**

Refer to this table when you want to determine the tool versions.

<table>
<thead>
<tr>
<th>Tool</th>
<th>Version in 17.0 Standard Edition</th>
<th>Version in 17.0 Pro Edition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mentor bare-metal GCC Compiler</td>
<td>5.2.0 (Sourcery CodeBench Lite 2015.11-45)</td>
<td>6.2.0 (Sourcery CodeBench Lite 2016.11-38)</td>
</tr>
<tr>
<td>Linux Compiler</td>
<td>4.8.3 (Linaro GCC 4.8-2014.04)</td>
<td>4.8.3 (Linaro GCC 4.8-2014.04)</td>
</tr>
<tr>
<td>ARM Compiler 5</td>
<td>5.06 update 3</td>
<td>5.06 update 4</td>
</tr>
<tr>
<td>ARM DS-5</td>
<td>5.25.0</td>
<td>5.26.2</td>
</tr>
</tbody>
</table>

**Related Links**

- Installing the SoC FPGA EDS on page 11
  You must install the SoC FPGA EDS and the ARM DS-5 in order to run the SoC FPGA EDS on an Intel SoC hardware platform.
- Licensing on page 14
- Linux Compiler on page 97

**1.2 Overview**

The SoC FPGA EDS enables you to perform all required software development tasks targeting the Intel FPGA SoCs, including:

- Board bring-up
- Device driver development
- Operating system (OS) porting
- Bare-metal application development and debugging
- OS- and Linux-based application development and debugging
- Debug systems running symmetric multiprocessing (SMP)
- Debug software targeting soft IP residing on the FPGA portion of the device
The major components of the SoC FPGA EDS include:

- ARM® Development Studio 5 (DS-5™) AE (AE) Toolkit
- Compiler tool chains:
  - Bare-metal GNU Compiler Collection (GCC) tool chain from Mentor Graphics®
  - ARMCC Bare-metal compiler
  - Linux GCC compiler tool chain from Linaro®
- Pre-built Linux package including:
  - Linux kernel executable
  - U-boot image
  - Bootloader Device Tree — Device tree blob consumed by U-boot for Arria 10
  - Linux Device Tree — Device tree blob consumed by Linux
  - Secure Digital (SD) card image
  - Script to download Linux source code from the GitHub repository
- SoC Hardware Library (HWLIB)
- Hardware-to-software interface utilities:
  - Second stage bootloader generator
  - Linux device tree generator
- Sample applications
- Golden Hardware Reference Designs (GHRD) including:
  - FPGA hardware project
  - FPGA hardware SRAM Object File (.sof) file
  - Precompiled Second Stage Bootloaders
    - Preloader for Arria V and Cyclone V
    - Bootloader for Arria 10
- Embedded command shell allowing easy invocation of the included tools
- SD Card Boot Utility
- Quartus Prime Programmer and SignalTap II

Note: The Linux package included in the SoC FPGA EDS is not an official release and is intended to be used only as an example. Use the official Linux release described in the Golden System Reference Design (GSRD) User Manual available on the Rocketboards website or a specific release from the Git trees located on the GitHub repository for development.

Note: The SoC FPGA EDS is tested only with the Linux release that comes with it. Newer Linux releases may not be fully compatible with this release of the SoC FPGA EDS.

Note: The Golden Hardware Reference Design (GHRD) included with the SoC FPGA EDS is not an official release and is intended to be used only as an example. For development purposes, use the official GHRD release described in the GSRD User Manual available on the Rocketboards website.

1 The script downloads the sources corresponding to the pre-built Linux package.
1.2.1 Linux Device Tree Binary

There are two different Linux device tree binary (DTB) file versions delivered as part of the SoC FPGA EDS:

- The version from the `prebuilt_images` folder—`socfpga_cyclone5.dtb` and `socfpga_arria10.dtb` are generic DTB files which do not have any dependency on soft IP.²
  
  Note: This DTB file is intended for customers interested in bringing up a new board or just wanting to simplify their boot flow until they get to the Linux prompt. If what is being developed or debugged does not involve the FPGA, it is better to remove the FPGA complexities.

- The version from the hardware design folder—`soc_system.dtb`, `ghrd_5astfd5k3.dtb`, and `ghrd_10as066n2.dtb` are based on the GHRD design, which is part of the GSRD. Since the GHRD does contain soft IPs, these DTB file versions notify Linux to load the soft IP drivers. Therefore, the FPGA needs to be programmed and the bridges released before booting Linux.

1.3 Hardware and Software Development Roles

Depending on your role in hardware or software development, you need a different subset of the SoC FPGA EDS toolkit. The following table lists some typical engineering development roles and indicates the tools that each role typically requires.

For more information about each of these tools, refer to the Intel SoC FPGA Embedded Development Suite page.

### Table 2. Hardware and Software Development Roles

This table lists typical tool usage, but your actual requirements depend on your specific project and organization.

<table>
<thead>
<tr>
<th>Tool</th>
<th>Hardware Engineer</th>
<th>Bare-Metal Developer</th>
<th>RTOS Developer</th>
<th>Linux Kernel and Driver Developer</th>
<th>Linux Application Developer</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM DS-5 Debugging</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>ARM DS-5 Tracing</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
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<tr>
<td>ARM DS-5 Cross Triggering</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hardware Libraries</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Second Stage Bootloader Generator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash Programmer</td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

² Before Linux is able to run, the peripheral RBF must be loaded into the FPGA, so that the DDR becomes available and runs.
1.3.1 Hardware Engineer

As a hardware engineer, you typically design the FPGA hardware in Qsys. You can use the debugger of ARM DS-5 AE to connect to the ARM cores and test the hardware. A convenient feature of the DS-5 debugger is the soft IP register visibility, using Cortex Microcontroller Software Interface Standard (CMSIS) System View Description (.svd) files. With this feature, you can easily read and modify the soft IP registers from the ARM side.

As a hardware engineer, you may generate the Preloader for your hardware configuration. The Preloader is a piece of software that configures the HPS component according to the hardware design.

As a hardware engineer, you may also perform the board bring-up. You can use ARM DS-5 debugger to verify that they can connect to the ARM and the board is working correctly.

These tasks require JTAG debugging, which is enabled only in the ARM DS-5 Intel SoC FPGA Edition, which is part of the paid Intel SoC FPGA EDS license.

Related Links
- Licensing on page 14
- Hardware – Software Development Flow on page 9

1.3.2 Bare-Metal and RTOS Developer

As a bare-metal or a RTOS developer, you need JTAG debugging and low-level visibility into the system. The following tasks require JTAG debugging, which is enabled only in the ARM DS-5 Intel SoC FPGA Edition.

- To compile your code and the SoC Hardware Library to control the hardware in a convenient and consistent way, use the bare-metal compiler.
- To program the flash memory on the target board, use the Flash Programmer.

For more information, see the "Licensing" section.

Related Links
- Licensing on page 14
1.3.3 Linux Kernel and Driver Developer

As a Linux kernel or driver developer, you may use the same tools the RTOS developers use, because you need low-level access and visibility into the system. However, you must use the Linux compiler instead of the bare-metal compiler. You can use the Linux device tree generator (DTG) to generate Linux device trees.

These tasks require JTAG debugging, which is enabled only in the ARM DS-5 Intel SoC FPGA Edition.

For more information, see the "Licensing" section.

Related Links
Licensing on page 14

1.3.4 Linux Application Developer

As a Linux application developer, you write code that targets the Linux OS running on the board. Because the OS provides drivers for all the hardware, you do not need low-level visibility over JTAG. DS-5 offers a very detailed view of the OS, showing information about the threads that are running and the drivers that are loaded.

These tasks do not require JTAG debugging. You can perform these tasks with both the paid and free SoC EDS FPGA licenses. For more information, see the "Licensing" section.

Related Links
Licensing on page 14

1.4 Hardware – Software Development Flow

The Intel hardware-to-software handoff utilities allow hardware and software teams to work independently and follow their respective familiar design flows.

Figure 1. Intel Hardware-to-Software Handoff
The following handoff files are created when the hardware project is compiled:

- **Handoff folder** – contains information about how the HPS component is configured, including things like which peripherals are enabled, the pin MUXing and IOCSR settings, and memory parameters. The handoff folder is used by the second stage bootloader generator to create the preloader.

  For more information about the handoff folder, refer to the "BSP Generation Flow" section.

- **.svd** file – contains descriptions of the HPS registers and of the soft IP registers on the FPGA side implemented in the FPGA portion of the device. The **.svd** file contains register descriptions for the HPS peripheral registers and soft IP components in the FPGA portion of the SoC. This file is used by the ARM DS-5 Debugger to allow these registers to be inspected and modified by the user.

  For more information, refer to the "Linux Device Tree Generator" section.

  *Note:* The soft IP register descriptions are not generated for all soft IP cores.

**Related Links**

- BSP Generation Flow on page 57
- SoC Embedded Development Suite Download Page
- Linux Device Tree Generator on page 98

### 1.5 Introduction to the SoC FPGA EDS Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| May 2017      | 2017.05.08 | • Intel FPGA rebranding
                |           | • Rebranded paths and tools for the Standard and Professional versions |
| November 2016 | 2016.11.07 | Maintenance release                                                      |
| May 2016      | 2016.05.27 | Renamed the Web and Subscription Editions to align with Quartus Prime naming |
| February 2016 | 2016.02.17 | Maintenance release                                                      |
| August 2015   | 2015.08.06 | Added Arria 10 support                                                  |
2 Installing the SoC FPGA EDS

You must install the SoC FPGA EDS and the ARM DS-5 in order to run the SoC FPGA EDS on an Intel SoC hardware platform.

2.1 Installation Folders

The default installation folder for SoC FPGA EDS, referred to as <SoC FPGA EDS installation directory> throughout this document, is:

- **Standard Edition:**
  - c:\intelFPGA\17.0\embedded on Windows
  - ~/intelFPGA/17.0/embedded on Linux

- **Professional Edition:**
  - c:\intelFPGA_pro\17.0\embedded on Windows
  - ~/intelFPGA_pro/17.0/embedded on Linux

The default installation folder for the Quartus Prime Programmer, referred to as <Quartus Prime installation directory> throughout this document, is:

- **Standard Edition:**
  - c:\intelFPGA\17.0\qprogrammer on Windows
  - ~/intelFPGA/17.0/qprogrammer on Linux

- **Professional Edition:**
  - c:\intelFPGA_pro\17.0\qprogrammer on Windows
  - ~/intelFPGA_pro/17.0/qprogrammer on Linux

2.2 Installing the SoC FPGA EDS on Windows

Perform the following steps to install the SoC FPGA EDS Tool Suite in a Windows-based system:

1. Download the latest installation program from the *Intel SoC FPGA Embedded Development Suite Download Center* page of the Intel FPGA website.

2. Run the installer to open the **Installing Intel SoC FPGA Embedded Development Suite (EDS)** dialog box, and click **Next** to start the Setup Wizard.

3. Accept the license agreement, and click **Next**.

4. Accept the default installation directory or browse to another installation directory, and click **Next**.

*Other names and brands may be claimed as the property of others.*
Note: It is recommended to accept the default installation paths for both Quartus Prime and SoC FPGA EDS software, to allow them to properly operate together.

5. Select **All** the components to be installed, and click **Next**. The installer displays a summary of the installation.

6. Click **Next** to start the installation process. The installer displays a separate dialog box with the installation progress of the component installation.

7. When the installation is complete, turn on **Launch DS-5 Installation** to start the ARM DS-5 installation, and click **Finish**.

Note: On some Linux-based machines, you can install the SoC FPGA EDS with a setup GUI similar to the Windows-based setup GUI. Because of the variety of Linux distributions and package requirements, not all Linux machines can use the setup GUI. If the GUI is not available, use an equivalent command-line process. Download the Linux installation program from the Intel SoC FPGA Embedded Development Suite Download Center page on the Intel FPGA website.

**Related Links**
SoC Embedded Development Suite Download Center

### 2.3 Installing the ARM DS-5 Intel SoC FPGA Edition Toolkit

For the last step of the SoC FPGA EDS installation process, start the ARM DS-5 for Intel SoC FPGA Edition Toolkit installer.

Note: Make sure you have the proper setting to access the internet.

1. When the **Welcome** message is displayed, click **Next**.
2. Accept the license agreement and click **Next**.
3. Accept the default installation path, to ensure proper interoperability between SoC FPGA EDS and ARM DS-5 for Intel SoC FPGA Edition, and click **Next**.
4. Click **Install** to start the installation process. The progress bar is displayed.
5. When a driver installation window appears, click **Next**.
6. Accept the driver installation and click **Install**.
7. After successful installation, click **Finish**. ARM DS-5 for Intel SoC FPGA Edition installation is complete.
8. Click **Finish**.

### 2.4 Installing the SoC FPGA EDS Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>May 2017</td>
<td>2017.05.08</td>
<td>• Intel FPGA rebranding</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Rebranded paths and tools for the Standard and Professional versions</td>
</tr>
<tr>
<td>November 2016</td>
<td>2016.11.07</td>
<td>Maintenance release</td>
</tr>
</tbody>
</table>

**continued...**
## 2 Installing the SoC FPGA EDS

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>May 2016</td>
<td>2016.05.27</td>
<td>Maintenance release</td>
</tr>
<tr>
<td>February 2016</td>
<td>2016.02.17</td>
<td>Updated the installation path to 15.1</td>
</tr>
<tr>
<td>August 2015</td>
<td>2015.08.06</td>
<td>Added Arria 10 support</td>
</tr>
</tbody>
</table>
3 Licensing

The only SoC FPGA EDS component that requires a license is the ARM DS-5 Intel SoC FPGA Edition. The rest of the SoC FPGA EDS components, such as tools and software, do not require a license. This is the same for both Standard and Professional editions of SoC FPGA EDS.

The ARM DS-5 has three different license options:

- ARM DS-5 Intel SoC FPGA Edition License
- ARM DS-5 Community Edition License
- 30-day Evaluation of ARM DS-5 Intel SoC FPGA Edition License

The following table shows the different debugging capabilities of the ARM DS-5 Intel SoC FPGA Edition Licenses:

<table>
<thead>
<tr>
<th>Licensing Option</th>
<th>Debugging Scenarios Enabled</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM DS-5 Community Edition License</td>
<td>• Linux application debugging over ethernet</td>
</tr>
</tbody>
</table>
| ARM DS-5 Intel SoC FPGA Edition License, including the 30 day evaluation version | • JTAG-based Bare-Metal Debugging  
• JTAG-based Linux Kernel and Driver Debugging  
• Linux Application Debugging over Ethernet |

Based on the specific ARM DS-5 Intel SoC FPGA Edition License that is used, the SoC FPGA EDS has two different licensing options:

- SoC FPGA EDS Paid license - using ARM DS-5 Intel SoC FPGA Edition license
- SoC FPGA EDS Free license - using ARM DS-5 Community Edition license

**Note:** For a detailed comparison chart, refer to the "Compare Editions" section on the Intel SoC FPGA Embedded Development Suite web page.

**Related Links**
SoC Embedded Development Suite web page

3.1 Getting the License

Depending on the licensing option, it is necessary to follow the steps detailed for each option to obtain the license.

**ARM DS-5 Intel SoC FPGA Edition License** - If you have purchased a SoC development kit or a stand-alone license for DS-5 AE, then you have already received an ARM license serial number. This is a 15-digit alphanumeric string with two dashes in between. Use this serial number to activate your license in DS-5, as shown in the "Activating the License" section.
This license contains one-year of Support and Maintenance from ARM starting at the date of purchase or renewal.

**DS-5 Community Edition License** - If you are using the SoC FPGA EDS Lite Edition, you are able to use the DS-5 perpetually to debug Linux applications over an Ethernet connection. Get your ARM license activation code from the "DS-5 Community Edition" section on the DS-5 Development Studio page on the ARM website and then activate your license in DS-5, as shown in the "Activating the License" section.

**30-Day Evaluation of DS-5 Intel SoC FPGA Edition License** - If you want to evaluate the DS-5 Intel SoC FPGA Edition, you can get a 30-Day Evaluation activation code from the "DS-5 Intel SoC FPGA Edition 30-Day Evaluation" section on the DS-5 Development Studio page on the ARM website and then activate your license in ARM DS-5 Intel SoC FPGA Edition, as shown in the "Activating the License" section.

**Related Links**
- SoC FPGA EDS Download Page
- Activating the License on page 15
- DS-5 Community Edition License
  For more information about obtaining your ARM license activation code for the DS-5 Community Edition license
- DS-5 Intel FPGA Edition 30-Day Evaluation
  For more information about obtaining your activation code for the DS-5 Intel FPGA Edition 30-Day Evaluation license

**3.2 Activating the License**

This section presents the steps required for activating the license in the ARM DS-5 for Intel SoC FPGA Edition by using the serial license number or activation code that were mentioned in the "Getting the License" chapter.

**Note:** An active user account is required to activate the ARM DS-5 Intel SoC FPGA Edition AE license. If you do not have an active user account, it can be created on the ARM Self-Service page available on the ARM website.

1. The first time the ARM DS-5 Intel SoC FPGA Edition is run, it notifies you that it requires a license. Click the Open License Manager button.
2. If at any time it is required to change the license, select Help ➤ ARM License Manager to open the License Manager.

3. The License Manager - View and edit licenses dialog box opens and shows that a license is not available. Click the Add License button.
4. In the **Add License - Obtain a new licenses** dialog box, select the type of license to enter. In this example, select the radio button, **“Enter a serial number or activation code to obtain a license”** to enter the choices listed, below. When done, click **Enter**.

   a. ARM DS-5 Intel SoC FPGA Edition—Enter the ARM License Number.

5. Click **Next**.

6. In the **Add License - Choose Host ID** dialog box, select the Host ID (Network Adapter MAC address) to tie the license to. If there are more than one option, select the one you desire to lock the license to, and click **Next**.
7. In the **Add License - Developer account details** dialog box, enter an ARM developer (Silver) account. If you do not have an account, it can be created easily by clicking the provided link. After entering the account information, click **Finish**.

**Note:** The License Manager needs to be able to connect to the Internet in order to activate the license. If you do not have an Internet connection, you will need to write down your Ethernet MAC address and generate the license directly from the ARM Self-Service web page on the ARM website, then select the "**Already have a license**" option in the License Manager.
Note: Only the ARM DS-5 Intel SoC FPGA Edition, with an associated license number can be activated this way. The ARM DS-5 Community Edition and 30-day Evaluation of ARM DS-5 Intel SoC FPGA Edition are based on activation codes, and these codes cannot be used on the ARM Self-Service web page on the ARM website. They need to be entered directly in the License Manager; which means an Internet connection is a requirement for licensing.

The ARM License Manager uses the Eclipse settings to connect to the Internet. The default Eclipse settings use the system-wide configuration for accessing the Internet. In case the License Manager cannot connect to the Internet, you can try to change the Proxy settings by going to Window ➤ Preferences ➤ General ➤ Network Connections. Ensure that "HTTPS" proxy entry is configured and enabled.

8. After a few moments, the ARM DS-5 will activate the license and display it in the License Manager. Click Close.

Figure 8. ARM License Manager

Related Links
- ARM website
- Getting the License on page 14

3.3 Licensing for the SoC FPGA EDS Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
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<tr>
<td>May 2017</td>
<td>2017.05.08</td>
<td>• Intel FPGA rebranding</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Rebranded paths and tools for the Standard and Professional versions</td>
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continued...
### Licensing

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<td>Renamed the Web and Subscription Editions to align with Quartus Prime naming</td>
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<td>2016.02.17</td>
<td>Maintenance release</td>
</tr>
<tr>
<td>August 2015</td>
<td>2015.08.06</td>
<td>Added Arria 10 support</td>
</tr>
</tbody>
</table>
4 Embedded Command Shell

The purpose of the embedded command shell is to provide an option for you to invoke the SoC FPGA EDS tools. It enables you to invoke the SoC FPGA EDS tools without qualifying them with the full path. Commands like `eclipse`, `bsp-editor`, or `arm-altera-eabi-gcc` can be executed directly.

On Windows, the embedded command shell is started by running:

```bash
<SoC FPGA EDS installation directory>\Embedded_Command_Shell.bat.
```

On Linux, the embedded command shell is started from the Start menu or by running:

```bash
<SoC FPGA EDS installation directory>/embedded_command_shell.sh.
```

4.1 Embedded Command Shell Document Revision History

<table>
<thead>
<tr>
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<th>Version</th>
<th>Changes</th>
</tr>
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</tbody>
</table>
5 Getting Started Guides

The Getting Started Guides chapter provides instructions on how to access complete Getting Started instructions including the following:

- Board Setup
- Running Linux
- Running the Tools
- Second Stage Bootloader
- Baremetal Debugging
- Hardware Libraries (HWLibs)
- Peripheral Register Visibility
- Baremetal Project Management
- Linux Application Debugging
- Linux Kernel and Driver Debugging
- Tracing

Related Links

SoCEDSGettingStarted
For more information about getting started, refer to the SoCEDSGettingStarted page on the Intel FPGA Wiki.

5.1 Getting Started Guides Document Revision History

<table>
<thead>
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<td>2016.02.17</td>
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<td>August 2015</td>
<td>2015.08.06</td>
<td>Removed content from this section and moved it to the Intel FPGA Wiki</td>
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6 ARM Development Studio 5 for Intel SoC FPGAs

The ARM Development Studio 5 (ARM DS-5) for Intel SoC FPGA is a device-specific exclusive offering from Intel; and is a powerful Eclipse-based comprehensive Integrated Development Environment (IDE).

For the current version, refer to Table 1 on page 5, located in the "Differences Between Standard and Professional Editions" section.

Some of the most important provided features are:

- File editing, supporting syntax highlighting and source code indexing
- Build support, based on makefiles
- Bare-metal debugging
- Linux application debugging
- Linux kernel and driver debugging
- Multicore debugging
- Access to HPS peripheral registers
- Access to FPGA soft IP peripheral registers
- Tracing of program execution through Program Trace Macrocells (PTM)
- Tracing of system events through System Trace Macrocells (STM)
- Cross-triggering between HPS and FPGA
- Connecting to the target using Intel FPGA Download Cable II

The ARM DS-5 for Intel SoC FPGA Edition is a complex tool with many features and options. This chapter only describes the most common features and options and provides getting started scenarios to help you get started, quickly.

You can access the ARM DS-5 for Intel SoC FPGA Edition reference material from Eclipse, by navigating to Help ➤ Help Contents ➤ ARM DS-5 Documentation or on the ARM website.

Related Links

- Online ARM DS-5 Documentation
  The ARM DS-5 for Intel SoC FPGA reference material can be accessed online on the documentation page of the ARM website.
- Differences Between Standard and Professional Editions on page 4

6.1 Starting Eclipse ARM DS-5 for Intel SoC FPGA Edition

ARM DS-5 for Intel SoC FPGA Edition must be started from the Embedded Command Shell.
Eclipse needs to be started from the Embedded Command Shell so that all the utilities are added to the search path, and they can be used directly from the makefiles without the full path.

To start the Eclipse IDE that the ARM DS-5 for Intel SoC FPGA Edition uses, you must type `eclipse &` at the command line.

### 6.2 Bare-Metal Project Management

ARM DS-5 for Intel SoC FPGA Edition enables convenient project management for bare-metal projects using two different methods:

- Using Makefiles
- Using the ARM DS-5 for Intel SoC FPGA Edition graphical interface

Some users prefer Makefiles because they allow the option for the project compilation to be performed from scripts. Other users prefer to use a GUI to manage the project, and this is available for both GCC and ARM Compiler bare-metal projects.

<table>
<thead>
<tr>
<th>Method</th>
<th>Advantages</th>
<th>Compiler Toolchain Support</th>
</tr>
</thead>
<tbody>
<tr>
<td>Makefile</td>
<td>Scripted compilation</td>
<td>GCC</td>
</tr>
<tr>
<td>ARM DS-5 for Intel SoC FPGA Edition graphical interface</td>
<td>Multiple toolchain support</td>
<td>GCC, ARM Compiler</td>
</tr>
</tbody>
</table>

#### 6.2.1 Bare-Metal Project Management Using Makefiles

The ARM DS-5 for Intel SoC FPGA Edition enables convenient project management using makefiles. The sample projects that are provided with SoC FPGA EDS use makefiles to manage the build process.

*Note:* This option refers to just the DS-5 specific aspects. If you are not familiar with defining and using makefiles, please use the ARM DS-5 for Intel SoC FPGA Edition GUI option detailed in the next section.

To allow ARM DS-5 for Intel SoC FPGA Edition to manage a makefile-based project, create a project, as follows:

1. Create a folder on the disk.
2. Create the project by selecting `File > New > Makefile Project with Existing Code.`
3. Type the folder name in the **Existing Code Location** edit box and then click **Finish**.
4. Create a Makefile in that folder, and define the rules required for compiling the code. Make sure it has the **all** and the **clean** targets. ARM DS-5 for Intel SoC FPGA Edition now offers the possibility of invoking the build process from the IDE and allows you to build your project, as shown in the following figure:
If the compilation tools issue errors, ARM DS-5 for Intel SoC FPGA Edition parses and formats them for you and displays them in the Problems view.


6.2.2 GCC-Based Bare-Metal Project Management

This section shows how the Bare-metal toolchain plugin can be used to manage GCC-based projects in a GUI environment.

6.2.2.1 Creating Project

1. Start Eclipse.
2. Go to File ➤ New C Project.
3. Determine if you want to create an Executable empty project or a Bare-metal library empty project.
   a. Bare-metal executable
      Select Project Type to be Executable ➤ Empty Project then Toolchain to be Intel FPGA Baremetal GCC then click Finish.
Figure 12. Bare-Metal Executable Project Type

b. Static Library
Select **Bare-metal Library ➤ Empty Project** and click Finish.
Figure 13. Bare-Metal Library Project Type
### 6.2.2.2 Build Settings

Once the project is created, the project properties can be accessed by going to **Project ➤ Properties**.

**Figure 14. Project Properties**

Then, in the **Project Properties** window, the **Compilation** settings can be accessed by selecting **C/C++ Build ➤ Settings**.
The **Build Settings** include detailed settings for all tools:

- Compiler
- Assembler
- Linker

The "Getting Started Guides" section in this document contains a link to complete instructions on how to create a project from scratch, compile it and run it on an Intel SoC development board.

**Related Links**

- Getting Started Guides on page 23

### 6.2.3 ARM Compiler Bare-Metal Project Management

The ARM Compiler 5 is shipped with the SoC FPGA EDS.

For the current version, refer to Table 1 on page 5, located in the "Differences Between Standard and Professional Editions" section. The ARM DS-5 can be used to manage ARM compiler projects in a GUI environment.

**Related Links**

- Differences Between Standard and Professional Editions on page 4
6.2.3.1 Creating a Project

1. Start Eclipse.
2. Go to **File ➤ New C Project**.
3. Select one of the following options:
   a. Select "Project Type" as **Executable ➤ Empty Project** and then for "Toolchains", select **ARM Compiler 5**. Click **Finish**.

**Figure 16.  Create an Empty ARM Compiler Bare-Metal Executable Project**

b. Select **Static Library ➤ Empty Project** and then for "Toolchains", select **ARM Compiler 5**. Click **Finish**.

Intel® SoC FPGA Embedded Development Suite User Guide
**6.2.3.2 Linker Script**

ARM DS-5 for Intel SoC FPGA Edition offers a visual tool to help create linker scripts.

1. Go to **File ➤ New ➤ Other...**
2. Select **Scatter File Editor ➤ Scatter File** and press **Next**.
Figure 19. Creating a Scatter File

3. Select the location of the new file, type in the file name and press **Finish**.
4. The linker script file can be edited directly as shown in the example below.
5. The file can also be edited by using the tools on the Outline view for the file.

Figure 22. Editing "Scatter.scat" File Using Tools on the Outline View

6.2.3.3 Build Settings

1. Once the project is created, the project properties can be accessed by going to Project ➤ Properties.
2. Then, in the **Project Properties** window, the "Compilation" settings can be accessed by selecting **C/C++ Build ➤ Settings**.

The build settings include detailed settings for all tools:
6 ARM Development Studio 5 for Intel SoC FPGAs

- Compiler
- Assembler
- Linker

The "Getting Started with ARM Compiler Bare Metal Project Management" contains a link to complete instructions on how to create a project from scratch, compile it and run it on an Intel SoC development board.

Related Links
Getting Started Guides on page 23

6.3 Debugging

The ARM DS-5 for Intel SoC FPGA Edition offers you a variety of debugging features.

6.3.1 Accessing Debug Configurations

The settings for a debugging session are stored in a Debug Configuration. The Debug Configurations window is accessible from the Run ➤ Debug Configurations menu.

Figure 25. Accessing Debug Configurations

6.3.2 Creating a New Debug Configuration

A Debug Configuration is created in the Debug Configurations window by selecting DS-5 Debugger as the type of configuration in the left panel and then right-clicking with the mouse and selecting the New menu option.
Figure 26. **Create New Debug Configuration**

In the ARM DS-5 for Intel SoC FPGA Edition, you can assign a default name to the configuration, which you can edit.

Figure 27. **Rename Debug Configuration**
6.3.3 Debug Configuration Options

This section lists the **Debug Configuration** options, which allows you to specify the desired debugging options for a project:

- Connection Options
- File Options
- Debugger Options
- RTOS Awareness
- Arguments
- Environment
- Event Viewer

**Related Links**

- **SoCedSGettingStarted**
  For examples on how to use the ARM DS-5 for Intel SoC FPGA debugging features, refer to the SoCedSGettingStarted page on the Intel FPGA Wiki.

- **Online ARM DS-5 Documentation**
  For more information, refer to the DS-5 reference documentation located on the ARM website.

### 6.3.3.1 Connection Options

The **Connection** tab allows the user to select the desired target. The following targets are available for the Intel platforms:

**Arria 10 SoC:**

- Bare Metal Debug
  - Debug Cortex-A9_0
  - Debug Cortex-A9_1
  - Debug Cortex-A9x2 SMP

- Linux Application Debug
  - Connect to already running gdbserver
  - Download and debug application
  - Start gdbserver and debug target resident application

- Linux Kernel and/or Device Driver Debug
  - Debug Cortex-A9_0
  - Debug Cortex-A9_1
  - Debug Cortex-A9x2 SMP

**Arria V SoC:**
- Bare Metal Debug
  - Debug Cortex-A9_0
  - Debug Cortex-A9_1
  - Debug Cortex-A9x2_SMP
- Linux Application Debug
  - Connect to already running `gdbserver`
  - Download and debug application
  - Start `dbgserver` and debug target resident application
- Linux Kernel and/or Device Driver Debug
  - Debug Cortex-A9_0
  - Debug Cortex-A9_1
  - Debug Cortex-A9x2_SMP

Cyclone V SoC (Single Core):
- Bare Metal Debug
  - Debug Cortex-A9_0
- Linux Application Debug
  - Connect to already running `gdbserver`
  - Download and debug application
  - Start `dbgserver` and debug target resident application
- Linux Kernel and/or Device Driver Debug
  - Debug Cortex-A9_0

Cyclone V SoC (Dual Core):
- Bare Metal Debug
  - Debug Cortex-A9_0
  - Debug Cortex-A9_1
  - Debug Cortex-A9x2_SMP
- Linux Application Debug
  - Connect to already running `gdbserver`
  - Download and debug application
  - Start `dbgserver` and debug target resident application
- Linux Kernel and/or Device Driver Debug
  - Debug Cortex-A9_0
  - Debug Cortex-A9_1
  - Debug Cortex-A9x2_SMP

Dual Arria V SoC (Two Dual Core SoCs):
• Bare Metal Debug
  — Debug HPS0 Cortex-A9_0
  — Debug HPS0 Cortex-A9_1
  — Debug HPS0 Cortex-A9x2_SMP
  — Debug HPS1 Cortex-A9_0
  — Debug HPS1 Cortex-A9_1
  — Debug HPS1 Cortex-A9x2_SMP

• Linux Application Debug
  — Connect to already running gdbserver
  — Download and debug application
  — Start dbgserver and debug target resident application

• Linux Kernel and/or Device Driver Debug
  — Debug HPS0 Cortex-A9_0
  — Debug HPS0 Cortex-A9_1
  — Debug HPS0 Cortex-A9x2_SMP
  — Debug HPS1 Cortex-A9_0
  — Debug HPS1 Cortex-A9_1
  — Debug HPS1 Cortex-A9x2_SMP

Dual Cyclone V SoC (Two Dual Core SoCs):
• Bare Metal Debug
  — Debug HPS0 Cortex-A9_0
  — Debug HPS0 Cortex-A9_1
  — Debug HPS0 Cortex-A9x2_SMP
  — Debug HPS1 Cortex-A9_0
  — Debug HPS1 Cortex-A9_1
  — Debug HPS1 Cortex-A9x2_SMP

• Linux Application Debug
  — Connect to already running gdbserver
  — Download and debug application
  — Start dbgserver and debug target resident application

• Linux Kernel and/or Device Driver Debug
  — Debug HPS0 Cortex-A9_0
  — Debug HPS0 Cortex-A9_1
  — Debug HPS0 Cortex-A9x2_SMP
  — Debug HPS1 Cortex-A9_0
  — Debug HPS1 Cortex-A9_1
  — Debug HPS1 Cortex-A9x2_SMP

Android Application Debug:
Native Application/Library Debug

- APK Native Library Debug via `gdbserver`
  - Attach to a running Android application
  - Download and debug an Android application

Linux Application Debug:

- Application Debug
  - Connections via `gdbserver`
    - Connect to already running `gdbserver`
    - Download and debug application
    - Start `dbgserver` and debug target resident application

Depending on the selected Target, the Connections panel will look different. For Bare Metal Debug and Linux Kernel and/or Device Driver Debug target types:

- A Target Connection option appears and it allows the user to select the type of connection to the target. Intel USB-Blaster and DSTREAM are two of the most common options.
- A DTSL option appears, allowing the user to configure the Debug and Traces Services Layer (detailed later).
- A Connections Browse button appears, allowing the user to browse and select either of the specific instances for the connection—Intel USB-Blaster or the DSTREAM instance.

**Figure 28. Connection Options for Bare-metal and Linux Kernel and/or Device Driver Debug**
For the **Linux Application Debug** targets, the connection parameters will be different depending on which type of connection was selected. The following two pictures illustrate the options.

**Figure 29.** Linux Application Debugging – Connect to a Running GDB Server

![Linux Application Debugging – Connect to a Running GDB Server](image)

DS-5 Debugger will connect to an already running gdbserver on the target system.

<table>
<thead>
<tr>
<th>Connections</th>
<th>gdbserver (TCP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address</td>
<td></td>
</tr>
<tr>
<td>Port</td>
<td>5000</td>
</tr>
</tbody>
</table>

- Use Extended Mode
- Terminate gdbserver on disconnect
Figure 30. Linux Application Debugging – Download And Debug Application

Note: For the Linux Application Debug, the Connection needs to be configured in the Remote System Explorer view, as shown in the "Getting Started with Linux Application Debugging" section.

Related Links
- DTSL Options on page 51
  For more information about the option on the Connections tab, refer to the DTSL Options section.
- Debugger Options on page 48
- Getting Started Guides on page 23
6.3.3.2 Files Options

The **Files** tab allows the following settings to be configured:

- **Application on host to download** – the file name of the application to be downloaded to the target. It can be entered directly in the edit box or it can be browsed for in the **Workspace** or on the **File System**.

- **Files** – contains a set of files. A file can be added to the set using the “+” button, and files can be removed from the set using the “-” button. Each file can be one of the following two types:
  - **Load symbols from file** – the debugger will use that file to load symbols from it,
  - **Add peripheral description files from directory** – the debugger to load peripheral register descriptions from the .SVD files stored in that directory. The SVD file is a result of the compilation of the hardware project.

![Files Settings](image.png)

**Figure 31. Files Settings**

6.3.3.3 Debugger Options

The **Debugger** tab offers the following configurable options

- **Run Control** Options
  - Option to connect only, debug from entry point or debug from user-defined symbol,
  - Option to run user-specified target initialization script,
  - Option to run user-specified debug initialization script,
  - Option to execute user-defined debugger commands

- **Host working directory** – used by semihosting

- **Paths** – allows the user to enter multiple paths for the debugger to search for sources. Paths can be added with “+” button and removed with “-” button.
6.3.3.4 RTOS Awareness

The RTOS Awareness tab allows the user to enable RTOS awareness for the debugger.
**6.3.3.5 Arguments**

The **Arguments** tab allows the user to enter program arguments as text.

**6.3.3.6 Environment**

The **Environment** tab allows the user to enter environment variables for the program to be executed.
6.3.4 DTSL Options

The Debug and Trace Services Layer (DTSL) provides tracing features. To configure trace options, in your project’s Debug Configuration window, in the "Connection" tab, click the Edit button to open the DTSL Configuration window.
6.3.4.1 Cross Trigger Settings

The Cross Trigger tab allows the configuration of the cross triggering option of the SoC FPGA.

The following options are available:

- **Enable FPGA > HPS Cross Trigger** – for enabling triggers coming from FPGA to HPS
- **Enable HPS > FPGA Cross Trigger** – for enabling triggers coming from HPS to FPGA

**Figure 37. DTSL Configuration Editor - Cross Trigger**

6.3.4.2 Trace Capture Settings

The Trace Capture tab allows the selection of the destination of the trace information. As mentioned in the introduction, the destination can be one of the following:

- **None** – meaning the tracing is disabled
- **ETR** – using any memory buffer accessible by HPS
- **ETF** – using the 32KB on-chip trace buffer
- **DSTREAM** – using the 4GB buffer located in the DSTREAM

The DSTREAM option is available only if the Target connection is selected as DSTREAM in the Debug Configuration.

**Figure 38. DTSL Configuration Editor - Trace Capture > Trace Capture Method**

The Trace Buffer tab provides the option of selecting the timestamp frequency.
6.3.4.3 Cortex-A9 Settings

The **Cortex-A9** tab allows the selection of the desired core tracing options.

**Figure 40. DTSL Configuration Editor - Cortex-A9**
The following Core Tracing Options are available:

- **Enable Cortex-A9 0 core trace** – check to enable tracing for core #0
- **Enable Cortex-A9 1 core trace** – check to enable tracing for core #1
- **PTM Triggers halt execution** – check to cause the execution to halt when tracing
- **Enable PTM Timestamps** – check to enable time stamping
- **Enable PMT Context IDs** – check to enable the context IDs to be traced
- **Context ID Size** – select 8-, 16- or 32-bit context IDs. Used only if Context IDs are enabled
- **Cycle Accurate** – check to create cycle accurate tracing
- **Trace capture range** – check to enable tracing only a certain address interval
- **Start Address, End Address** – define the tracing address interval (Used only if the Trace Capture Range is enabled)

### 6.3.4.4 STM Settings

The STM tab allows you to configure the System Trace Macrocell (STM).

**Figure 41.** DTSL Configuration Editor - STM

Only one option is available:

- **Enable STM Trace** – check to enable STM tracing.

### 6.3.4.5 ETR Settings

The ETR settings allow the configuration of the Embedded Trace Router (ETR) settings.

The Embedded Trace Router is used to direct the tracing information to a memory buffer accessible by HPS.

**Figure 42.** DTSL Configuration Editor - ETR
The following options are available:

- **Configure the system memory trace buffer** – check this if the ETR is selected for trace destination on the Trace Capture tab.
- **Start Address, Size** – define the trace buffer location in system memory and its size.
- **Enable scatter-gather mode** – use when the OS cannot guarantee a contiguous piece of physical memory. The scatter-gather table is setup by the operating system using a device driver and is read automatically by the ETR.

### 6.3.4.6 ETF Settings

The ETF tab allows the configuration of the Embedded Trace FIFO (ETF) settings.

The Embedded Trace FIFO is a 32KB buffer residing on HPS that can be used to store tracing data to be retrieved by the debugger, but also as an elastic buffer for the scenarios where the tracing data is stored in memory through ETR or on the external DSTREAM device using TPIU.

![Figure 43. DTSL Configuration Editor - ETF](image)

The following options are available:

- **Configure the on-chip trace buffer** – check this if ETF is selected for trace destination on the Trace Capture tab.
- **Size** – define the ETF size. The default size is set to 0x8000 (32KB).

### 6.4 ARM DS-5 for Intel SoC FPGA Edition Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
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|            |         | • Rebranded paths and tools for the Standard and Professional versions |
| November 2016 | 2016.11.07 | Maintenance release |
| May 2016   | 2016.05.27 | Maintenance release |
| February 2016 | 2016.02.17 | Updated default size in ETF Settings |
| August 2015 | 2015.08.06 | Added Arria 10 support |
7 Boot Tools User Guide

7.1 Introduction

The boot flow for all Intel SoC devices includes the second stage bootloader (SSBL). The SSBL is usually referred to as "preloader" in the context of Cyclone V and Arria V devices, and "bootloader" in the context of Arria 10 devices.

The SSBL is loaded by the boot ROM into the on-chip RAM (OCRAM) and has the task of bringing up the SDRAM, and loading and executing the next stage in the boot process.

![Figure 44. Cyclone V and Arria V Typical Boot Flow](image1)

For Cyclone V and Arria V devices, the OCRAM size is 64 KB, which limits the SSBL size and typically requires an additional bootloader stage, which then is used to load an operating system.

For Arria 10 devices, there is no need for an additional bootloader stage, because the OCRAM size is 256 KB and the required functionality is included in the SSBL.

This chapter presents the tools that are used to enable the SSBL management:

- **SSBL Support Package Generator** — enables the user to create and manage the SSBL
- **SSBL Image Tool (mkpimage)** — enables the user to add the boot ROM-required header on top of the SSBL
- **U-Boot Image Tool (mkimage)** — enables the user to add the SSBL-required header on top of the files loaded by SSBL
7.2 Second Stage Bootloader Support Package Generator

The Second Stage Bootloader (SSBL) Support Package Generator provides an easy, safe, and reliable way to customize the SSBL for the Intel SoC devices.

The SSBL Support Package is referred to as “BSP” and the SSBL Support Package Generator is referred to as “BSP Generator” for the remainder of this document.

The BSP Generator allows you to perform the following tasks:

• Create a new BSP
• Report BSP settings
• Modify BSP settings
• Generate BSP files

The generated BSP includes a makefile, which can be used to build the corresponding bootable Preloader or Bootloader image.

The BSP Generator functionality can be accessed from a Graphical User Interface or by using a set of command line tools, which allow complete scripting of the flow.

7.2.1 BSP Generation Flow

This section presents the BSP generation flow for both the Cyclone V and Arria V Preloader and Arria 10 Bootloader. While the flows are similar, there are some important differences.

7.2.1.1 Cyclone V and Arria V Flow

For Cyclone V and Arria V, the BSP Generator creates a customized BSP with preloader generic source files and board-specific SoC FPGA files. The generator consolidates the hardware settings and user inputs to create the BSP. The BSP files include a makefile to create the preloader image. The preloader image can then be downloaded to a Flash device or FPGA RAM to be used for booting HPS.

Figure 46. Arria V/ Cyclone V BSP Generator Flow
The hardware handoff information contains various settings that the user entered when creating the hardware design in Qsys and Quartus Prime Standard Edition. These include the following:

- Pin-muxing for the HPS dedicated pins
- I/O settings for the HPS dedicated pins:
  - Voltage
  - Slew rate
  - Pull up/ down
- State of HPS peripherals:
  - Enabled
  - Disabled
- Configuration of the bridges between HPS and FPGA
- Clock tree settings:
  - PLL settings
  - Clock divider settings
  - Clock gating settings
- DDR settings:
  - Technology
  - Width
  - Speed

The handoff settings are output from the Quartus Prime Standard Edition compilation and are located in the `<quartus project directory>/hps_isw_handoff/<hps entity name>` directory (where `<hps entity name>` is the HPS component name in Qsys).

You must update the hardware handoff files and regenerate the BSP each time a hardware change impacts the HPS, such as after pin multiplexing or pin assignment changes.

### 7.2.1.2 Arria 10 Flow

For Arria 10, the BSP Generator creates a customized BSP consisting of a makefile and a Bootloader Device Tree. There is no source code generated, as all customization is encapsulated in the Bootloader Device Tree and makefile settings. The makefile can be used to create the combined bootloader image, which contains both the bootloader executable and the bootloader device tree. The combined image can then be downloaded to a Flash device or FPGA RAM to be used for booting HPS.
The hardware handoff information contains various settings that the user entered when creating the hardware design in Qsys and Quartus Prime Standard Edition. These include the following:

- Pin-muxing for the HPS dedicated pins
- I/O settings for the HPS dedicated pins:
  - Voltage
  - Slew rate
  - Pull up/ down
- Pin-muxing for the shared pins
- State of HPS peripherals:
  - Enabled
  - Disabled
- Configuration of the bridges between HPS and FPGA
- Clock tree settings:
  - PLL settings
  - Clock divider settings
  - Clock gatting settings

The handoff settings are output from the Quartus Prime Standard Edition compilation and are located in the `<quartus project directory>/hps_isw_handoff` directory.

The user must run the BSP Generator and re-generate the Bootloader device tree each time a hardware change results in a change of the above parameters.

However, the user does not have to always recompile the Bootloader whenever a hardware setting is changed. The Bootloader needs to be recompiled only when changing the boot source.
7.2.2 BSP Generator Graphical User Interface

You must perform the following steps to use the BSP Generator GUI, \texttt{bsp-editor}:

1. Start an embedded command shell.

2. Run the \texttt{bsp-editor} command in the embedded command shell to launch the BSP Generator GUI.

3. To open and modify an existing BSP project, click \textbf{File > Open} and browse to an existing .bsp file.

4. To create a new BSP project, click \textbf{File > New HPS BSP} to open the \texttt{New BSP} dialog box. The \texttt{New BSP} dialog box includes the following settings and parameters:
   - \textbf{Preloader settings directory} – the path to the hardware handoff files. The generator inspects the handoff files to verify the validity of this path.
   - \textbf{Operating system} – Select the type of SSBL from the following two options:
     - U-Boot SPL Preloader (Cyclone V/Arria V HPS)
     - U-Boot Bootloader or UEFI Bootloader (Arria 10 HPS)
   - \textbf{Version} – the SSBL version to use. This release only supports the default 1.0 version.
   - \textbf{Use default locations} – checked by default, to derive the location of the BSP from the location of the hardware handoff folder. Uncheck if a custom path is desired instead.
   - \textbf{BSP target directory} – the destination folder for new BSP files created by the generator. This document refers to this as <bsp directory>. The default directory name is spl_bsp for the Arria V/ Cyclone V Preloader and uboot_bsp or uefi_bsp for the Arria 10 Bootloader. The directory name can be modified when \texttt{Use default locations} is unchecked.
   - \textbf{BSP settings file name} – the location and filename of the .bsp file containing the BSP settings.
   - \textbf{Additional .tcl scripting} – the location and filename of a .tcl script for overriding the default BSP settings.

5. You can customize the BSP. After creating or opening a .bsp file, access the \texttt{Settings} in the \texttt{BSP Editor} dialogue box. The Settings are divided into Common and Advanced settings. When you select a group of settings, the controls for the selected settings appear on the right side of the dialogue box.

When you select a single setting, the setting name, description and value are displayed. You can edit these settings in the \texttt{BSP Editor} dialogue box.

6. Click \textbf{Generate} to generate the BSP.

7. Click \textbf{Exit} to exit the BSP Generator GUI.

7.2.2.1 Using .tcl Scripts

Instead of using the default settings, you can create a tcl script file (.tcl) to define custom settings during BSP creation.

\texttt{set_setting} is the only available .tcl command.
For more information about the list of available settings, refer to the "BSP Settings" section.

The following shows example commands that are used to set parameters in the BSP settings file:

```plaintext
set_setting spl.boot.BOOT_FROM_QSPI true
set_setting spl.boot.QSPI_NEXT_BOOT_IMAGE 0x50000
```

Related Links
BSP Settings on page 64

7.2.3 BSP Generator Command Line Interface

The BSP command-line tools can be invoked from the embedded command shell, and provide all the features available in the BSP Generator GUI:

- The `bsp-create-settings` tool creates a new BSP settings file.
- The `bsp-update-settings` tool updates an existing BSP settings file.
- The `bsp-query-settings` tool reports the setting values in an existing BSP settings file.
- The `bsp-generate-files` tool generates a BSP from the BSP settings file.

**Note:** Help for each tool is available from the embedded command shell. To display help, type the following command: `<name of tool> --help`.

7.2.3.1 bsp-create-settings

The `bsp-create-settings` tool creates a new BSP settings file with default settings. You have the option to modify the BSP settings or generate the BSP files as shown in the following example.

**Example 1. Creating a New BSP Settings File**

The following example creates a new Preloader BSP settings file, based on the hardware handoff information and using the default BSP settings:

```plaintext
bsp-create-settings --type spl -- BSP-dir ./
--settings settings.bsp \
--preloader-settings-dir ../..//hps_isw_handoff/<hps_entity_name>
```

**Table 4. User Parameters: bsp-create-settings**

<table>
<thead>
<tr>
<th>Option</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>--type &lt;bsp type&gt;</td>
<td>Yes</td>
<td>This option specifies the type of BSP. Allowed values are:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• &quot;spl&quot; for Cyclone V/Arria V Preloader</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• &quot;uboot&quot; and &quot;uefi&quot; for Arria 10 Bootloader</td>
</tr>
<tr>
<td>--settings &lt;filename&gt;</td>
<td>Yes</td>
<td>This option specifies the path to a BSP settings file. The file is created with default settings. Intel recommends that you name the BSP settings file &quot;settings.bsp&quot;.</td>
</tr>
</tbody>
</table>
### 7.2.3.2 bsp-update-settings

The **bsp-update-settings** tool updates the settings stored in the BSP settings file, as shown in the following example.

#### Example 2. Updating a BSP Settings File

The following command changes the value of a parameter inside the file "settings.bsp":

```bash
bsp-update-settings --settings settings.bsp --set spl.debug.SEMIHOSTING 1
```

#### Table 5. User Parameters: bsp-update-settings

<table>
<thead>
<tr>
<th>Option</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>--settings &lt;settings-file&gt;</td>
<td>Yes</td>
<td>This option specifies the path to an existing BSP settings file to update.</td>
</tr>
<tr>
<td>--bsp-dir &lt;bsp-dir&gt;</td>
<td>No</td>
<td>This option specifies the path where the BSP files are generated. When this option is specified, <strong>bsp -create-settings</strong> generates the BSP files after the settings file has been created.</td>
</tr>
<tr>
<td>--set &lt;name&gt; &lt;value&gt;</td>
<td>No</td>
<td>This option sets the BSP setting &lt;name&gt; to the value &lt;value&gt;. Multiple instances of this option can be used with the same command. Refer to <strong>BSP Settings</strong> for a complete list of available setting names and descriptions.</td>
</tr>
</tbody>
</table>

### 7.2.3.3 bsp-query-settings

The **bsp-query-settings** tool queries the settings stored in BSP settings file, as shown in the following example.

#### Example 3. Querying a BSP Settings File

The following command will retrieve all the settings from "settings.bsp" and displays the setting names and values:

```bash
bsp-query-settings --settings settings.bsp --get-all --show-names
```
### Table 6. User Parameters: bsp-query-settings

<table>
<thead>
<tr>
<th>Option</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>--settings &lt;settings-file&gt;</td>
<td>Yes</td>
<td>This option specifies the path to an existing BSP settings file.</td>
</tr>
<tr>
<td>--get &lt;name&gt;</td>
<td>No</td>
<td>This option instructs <code>bsp-query-settings</code> to return the value of the BSP setting &lt;name&gt;.</td>
</tr>
<tr>
<td>--get-all</td>
<td>No</td>
<td>This option shows all the BSP settings values. When using --get-all, you must also use --show-names.</td>
</tr>
<tr>
<td>--show-names</td>
<td>No</td>
<td>This option only takes effect when used together with --get &lt;name&gt; or --get-all. When used with one of these options, names and values of the BSP settings are shown side-by-side.</td>
</tr>
</tbody>
</table>

### 7.2.3.4 bsp-generate-files

The `bsp-generate-files` tool generates the files and settings stored in BSP settings file, as shown in the following examples.

#### Example 4. Generating Files After BSP Creation

The following commands create a settings file based on the handoff folder, and then generate the BSP files based on those settings:

```bash
bsp-create-settings --type spl --bsp-dir . \
 --settings settings.bsp \ 
 --preloader-settings-dir \ 
 ../../hps_isw_handoff/<hps_entity_name> \
 bsp-generate-files --settings settings.bsp --bsp-dir
```

#### Example 5. Generating Files After BSP Updates

The following commands update the settings of an existing BSP settings file, and then generate the BSP files based on those settings:

```bash
bsp-update-settings --settings settings.bsp --set \ 
 spl.debug.SEMIHOSTING 1 \
 bsp-generate-files --settings settings.bsp --bsp-dir
```

Use the `bsp-generate-files` tool when BSP files need to be regenerated in one of the following conditions:

- **bsp-create-settings** created the BSP settings, but the --bsp-dir parameter was not specified, so BSP files were not generated.
- **bsp-update-settings** updated the BSP settings, but the --bsp-dir parameter was not specified, so the files were not updated.
- You want to ensure the BSP files are up-to-date.

### Table 7. User Parameters: bsp-generate-files

<table>
<thead>
<tr>
<th>Option</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>--settings &lt;settings-file&gt;</td>
<td>Yes</td>
<td>This option specifies the path to an existing BSP settings file.</td>
</tr>
<tr>
<td>--bsp-dir &lt;bsp-dir&gt;</td>
<td>Yes</td>
<td>This option specifies the path where the BSP files are generated.</td>
</tr>
</tbody>
</table>
7.2.4 BSP Files and Folders

The files and folders created with the BSP Generator are stored in the location you specified in **BSP target directory** in the **New BSP** dialog box.

For Cyclone V/Arria Preloader BSPs, the generated files include the following:

- **settings.bsp** – file containing all BSP settings
- **Makefile** – makefile used to compile the Preloader and create the preloader image; for more information, refer to Preloader Compilation
- **preloader.ds** – ARM DS-5 script, that can be used to download and debug the Preloader on a target device
- **generated** – folder containing files generated from the hardware handoff files

For Arria 10 Bootloader BSPs, for both U-Boot and UEFI, the generated files include the following:

- **settings.bsp** – file containing all BSP settings
- **Makefile** – makefile used to compile the Bootloader, convert the Bootloader device tree file to binary, and create the combined Bootloader and Bootloader Device Tree image; for more information, refer to Preloader Compilation
- **config.mk** – makefile configuration file, containing the boot source selection and whether the Bootloader compilation is selected
- **devicetree.dts** – Bootloader device tree, containing the Bootloader customization details, derived from the handoff files and the user settings

7.2.5 BSP Settings

This section lists all the available BSP settings, which can be accessed from either the Graphical User Interface application (**bsp-editor**) or from the command line tools (**bsp-create-settings**, **bsp-update-settings**, **bsp-query-settings**).

The available BSP settings are different between Cyclone V and Arria V SSBL (Preloader) and Arria 10 SSBL (Bootloader).

7.2.5.1 Cyclone V and Arria V BSP Settings

<table>
<thead>
<tr>
<th>BSP Setting</th>
<th>Type</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>spl.PRELOADER_TGZ</td>
<td>String</td>
<td>&lt;SoC FPGA EDS installation directory&gt;/host_tools/altera/preloader/uboot-socpfga.tar.gz</td>
<td>This setting specifies the path to archive file containing the preloader source files.</td>
</tr>
<tr>
<td>spl.CROSS_COMPILE</td>
<td>String</td>
<td>&quot;arm-altera-eabi-&quot;</td>
<td>This setting specifies the cross compilation tool chain for use.</td>
</tr>
<tr>
<td>spl.boot.BOOT_FROM_QSPI</td>
<td>Boolean</td>
<td>False</td>
<td>Select the source for the subsequent boot image. Note that only one source can be active at a time. When using <strong>bsp-create-settings</strong> or <strong>bsp-update-</strong></td>
</tr>
<tr>
<td>spl.boot.BOOT_FROM_SDMNC</td>
<td>Boolean</td>
<td>True</td>
<td>continued...</td>
</tr>
<tr>
<td>BSP Setting</td>
<td>Type</td>
<td>Default Value</td>
<td>Description</td>
</tr>
<tr>
<td>------------------------------</td>
<td>--------------</td>
<td>---------------</td>
<td>--------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>spl.boot.BOOT_FROM_RAM</td>
<td>Boolean</td>
<td>False</td>
<td>Settings, you must turn off the boot option that is currently turned on before you can turn on a different boot option.</td>
</tr>
<tr>
<td>spl.boot.BOOT_FROM_NAND</td>
<td>Boolean</td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>spl.boot.QSPI_NEXT_BOOT_IMAGE</td>
<td>Hexadecimal</td>
<td>0x60000</td>
<td>This setting specifies the location of the subsequent boot image in QSPI.</td>
</tr>
<tr>
<td>spl.boot.SDMMC_NEXT_BOOT_IMAGE</td>
<td>Hexadecimal</td>
<td>0x40000</td>
<td>This setting specifies the location of the subsequent boot image in SD/MMC.</td>
</tr>
<tr>
<td>spl.boot.NAND_NEXT_BOOT_IMAGE</td>
<td>Hexadecimal</td>
<td>0xC0000</td>
<td>This setting specifies the location of the subsequent boot image in NAND.</td>
</tr>
<tr>
<td>spl.boot.FAT_SUPPORT</td>
<td>Boolean</td>
<td>False</td>
<td>Enable FAT partition support when booting from SD/MMC.</td>
</tr>
<tr>
<td>spl.boot.FAT_BOOT_PARTITION</td>
<td>DecimalNumber</td>
<td>1</td>
<td>When FAT partition support is enabled, this specifies the FAT partition where the boot image is located.</td>
</tr>
<tr>
<td>spl.boot.FAT_LOAD_PAYLOAD_NAME</td>
<td>String</td>
<td>&quot;u-boot.img&quot;</td>
<td>When FAT partition supported is enabled, this specifies the boot image filename to be used.</td>
</tr>
<tr>
<td>spl.boot.WATCHDOG_ENABLE</td>
<td>Boolean</td>
<td>True</td>
<td>This setting enables the watchdog during the preloader execution phase. The watchdog remains enabled after the preloader exits.</td>
</tr>
<tr>
<td>spl.boot.CHECKSUM_NEXT_IMAGE</td>
<td>Boolean</td>
<td>True</td>
<td>This setting enables the preloader to validate the checksum in the subsequent boot image header information.</td>
</tr>
<tr>
<td>spl.boot.EXE_ON_FPGA</td>
<td>Boolean</td>
<td>False</td>
<td>This setting executes the preloader on the FPGA. Select spl.boot.EXE_ON_FPGA when the preloader is configured to boot from the FPGA.</td>
</tr>
<tr>
<td>spl.boot.STATE_REG_ENABLE</td>
<td>Boolean</td>
<td>True</td>
<td>This setting enables writing the magic value to the INITSWSTATE register in the system manager when the preloader exists; this indicates to the boot ROM that the preloader has run successfully.</td>
</tr>
<tr>
<td>spl.boot.BOOTROM_HANDSHAKE_CFGIO</td>
<td>Boolean</td>
<td>True</td>
<td>This setting enables handshake with boot ROM when configuring the IOCSR and pin multiplexing. If spl.boot.BOOTROM_HANDSHAKE_CFGIO is enabled and warm reset occurs when the preloader is configuring IOCSR and pin multiplexing, the boot ROM will reconfigure IOCSR and pin multiplexing again. This option is enabled by default.</td>
</tr>
<tr>
<td>spl.boot.WARMRST_SKIP_CFGIO</td>
<td>Boolean</td>
<td>True</td>
<td>This setting enables the preloader to skip IOCSR and pin multiplexing configuration during warm reset. spl.boot.WARMRST_SKIP_CFGIO is only applicable if the boot ROM has skipped IOCSR and pin multiplexing configuration.</td>
</tr>
<tr>
<td>spl.boot.SDRAM_INITIALIZATION</td>
<td>Boolean</td>
<td>False</td>
<td>Initialize the SDRAM to initialize the ECC bits.</td>
</tr>
<tr>
<td>spl.boot.SDRAM_ECC_INIT_BOOT_REGION_START</td>
<td>Hexadecimal</td>
<td>0x1000000</td>
<td>The start address of the memory region within the SDRAM to be initialized.</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>BSP Setting</th>
<th>Type</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>spl.boot.SDRAM_ECC_INIT_BOOT_REGION_END</td>
<td>Hexadecimal</td>
<td>0x2000000</td>
<td>The end address of the memory region within SDRAM to be initialized.</td>
</tr>
<tr>
<td>spl.boot.SDRAM_ECC_INIT_REMAIN_REGION</td>
<td>Boolean</td>
<td>True</td>
<td>Initialize the remaining SDRAM, during the flash accesses to load the image.</td>
</tr>
<tr>
<td>spl.debug.DEBUG_MEMORY_WRITE</td>
<td>Boolean</td>
<td>False</td>
<td>This setting enables the preloader to write debug information to memory for debugging, useful when UART is not available. The address is specified by spl.debug.DEBUG_MEMORY_ADDR.</td>
</tr>
<tr>
<td>spl.debug.SEMIHOSTING</td>
<td>Boolean</td>
<td>False</td>
<td>This setting enables semihosting support in the preloader, for use with a debugger tool. spl.debug.SEMIHOSTING is useful when UART is unavailable.</td>
</tr>
<tr>
<td>spl.debug.SKIP_SDRAM</td>
<td>Boolean</td>
<td>False</td>
<td>The preloader skips SDRAM initialization and calibration when this setting is enabled.</td>
</tr>
<tr>
<td>spl.performance.SERIAL_SUPPORT</td>
<td>Boolean</td>
<td>True</td>
<td>This setting enables UART print out support, enabling preloader code to call printf() at runtime with debugging information. stdout output from printf() is directed to the UART. You can view this debugging information by connecting a terminal program to the UART specified peripheral.</td>
</tr>
<tr>
<td>spl.reset_assert.DMA</td>
<td>Boolean</td>
<td>False</td>
<td>When enabled, this setting will force the corresponding peripheral to remain in reset. You must ensure the debugger does not read registers from these components.</td>
</tr>
<tr>
<td>spl.reset_assert.GPIO0</td>
<td>Boolean</td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>spl.reset_assert.GPIO1</td>
<td>Boolean</td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>spl.reset_assert.GPIO2</td>
<td>Boolean</td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>spl.reset_assert.L4WD1</td>
<td>Boolean</td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>spl.reset_assert.OSCTIMER1</td>
<td>Boolean</td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>spl.reset_assert.SDR</td>
<td>Boolean</td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>spl.reset_assert.SPTIMER0</td>
<td>Boolean</td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>spl.reset_assert.SPTIMER1</td>
<td>Boolean</td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>spl.warm_reset_handshake.FPGA</td>
<td>Boolean</td>
<td>True</td>
<td>This option allows the SDRAM contents to be preserved across warm resets.</td>
</tr>
<tr>
<td>spl.warm_reset_handshake.ETR</td>
<td>Boolean</td>
<td>True</td>
<td>This setting enables the reset manager to perform handshake with the FPGA before asserting a warm reset.</td>
</tr>
<tr>
<td>spl.warm_reset_handshake.SDRAM</td>
<td>Boolean</td>
<td>False</td>
<td>This setting enables the reset manager to request that the Embedded Trace Router (ETR) stalls the Advanced eXtensible Interface (AXI) master and waits for the ETR to finish any outstanding AXI transactions before asserting a warm reset of the L3 interconnect or a debug reset of the ETR.</td>
</tr>
<tr>
<td>BSP Setting</td>
<td>Type</td>
<td>Default Value</td>
<td>Description</td>
</tr>
<tr>
<td>------------------------------</td>
<td>-----------</td>
<td>---------------</td>
<td>-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>spl.boot.FPGA_MAX_SIZE</td>
<td>Hexadecimal</td>
<td>0x10000</td>
<td>This setting specifies the maximum code (.text and .rodata) size that can fit within the FPGA. If the code build is bigger than the specified size, a build error is triggered.</td>
</tr>
<tr>
<td>spl.boot.FPGA_DATA_BASE</td>
<td>Hexadecimal</td>
<td>0xFFFF0000</td>
<td>This setting specifies the base location for the data region (.data, .bss, heap and stack) when execute on FPGA is enabled.</td>
</tr>
<tr>
<td>spl.boot.FPGA_DATA_MAX_SIZE</td>
<td>Hexadecimal</td>
<td>0x10000</td>
<td>This setting specifies the maximum data (.data, .bss, heap and stack) size that can fit within FPGA. If the code build is bigger than the specified size, a build error is triggered.</td>
</tr>
<tr>
<td>spl.debug.DEBUG_MEMORY_ADDR</td>
<td>Hexadecimal</td>
<td>0xFFFFFD00</td>
<td>This setting specifies the base address for storing preloader debug information enabled with the spl.debug.DEBUG_MEMORY_WRITE setting.</td>
</tr>
<tr>
<td>spl.debug.DEBUG_MEMORY_SIZE</td>
<td>Hexadecimal</td>
<td>0x200</td>
<td>This setting specifies the maximum size used for storing preloader debug information.</td>
</tr>
<tr>
<td>spl.debug.DEBUG_MEMORY_ADDR</td>
<td>Hexadecimal</td>
<td>0xFFFFFD00</td>
<td>This setting specifies the base address for storing preloader debug information enabled with the spl.debug.DEBUG_MEMORY_WRITE setting.</td>
</tr>
<tr>
<td>spl.debug.HARDWARE_DIAGNOSTIC</td>
<td>Boolean</td>
<td>False</td>
<td>Enable hardware diagnostic support. To enable this, at least 1GB of memory is needed, otherwise hardware diagnostic will fail to run properly.</td>
</tr>
<tr>
<td>spl.boot.RAMBOOT_PLLRESET</td>
<td>Boolean</td>
<td>True</td>
<td>Execute RAM Boot PLL reset code on warm reset when CSEL = 00. This option is required to enable correct warm reset functionality when using CSEL = 00. When enabling this option, the upper 4 KB of OCRAM are reserved and must not be modified by the user software. Note: Enabling this feature with CSEL != 00 does not have any effect, as the impacted code checks for this.</td>
</tr>
</tbody>
</table>
7.2.5.2 Arria 10 BSP Settings

The Arria 10 BSP Settings are divided in four different groups:

- Main Group
- MPU Firewall
- L3 Firewall Group
- F2S Firewall Group

The following table presents the settings prefix to be added in front of the setting name for each of the groups. They are presented in a table to make the rest of this section more readable.

Table 9. Arria 10 BSP Firewall Setting Prefixes

<table>
<thead>
<tr>
<th>Settings Group</th>
<th>Setting Group Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Group</td>
<td>N/A</td>
</tr>
<tr>
<td>MPU Firewall</td>
<td>For U-Boot: altera_arria10_soc_noc_arria10_uboot_driver.I_NOC.mpu_m0.noc_fw_ddr_mpu_fpga2sdram_ddr_scr. For UEFI: altera_arria10_soc_noc_arria10_uefi_driver.I_NOC.mpu_m0.noc_fw_ddr_mpu_fpga2sdram_ddr_scr.</td>
</tr>
<tr>
<td>L3 Firewall Group</td>
<td>For U-Boot: altera_arria10_soc_noc_arria10_uboot_driver.I_NOC.mpu_m0.noc_fw_ddr_l3_ddr_scr. For UEFI: altera_arria10_soc_noc_arria10_uefi_driver.I_NOC.mpu_m0.noc_fw_ddr_l3_ddr_scr.</td>
</tr>
<tr>
<td>F2S Firewall Group</td>
<td>For U-Boot: altera_arria10_soc_noc_arria10_uboot_driver.I_NOC.mpu_m0.noc_fw_ddr_mpu_fpga2sdram_ddr_scr. For UEFI: altera_arria10_soc_noc_arria10_uefi_driver.I_NOC.mpu_m0.noc_fw_ddr_mpu_fpga2sdram_ddr_scr.</td>
</tr>
</tbody>
</table>

7.2.5.2.1 Arria 10 Main BSP Settings Group

Table 10. Arria 10 Main BSP Settings Group for U-Boot

<table>
<thead>
<tr>
<th>BSP Setting</th>
<th>Type</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>uboot.boot_device</td>
<td>String</td>
<td>SD/MMC</td>
<td>Select the source for the boot image. Possible values are SD/MMC, QSPI, and NAND.</td>
</tr>
<tr>
<td>uboot.model</td>
<td>String</td>
<td>SOCPFPGA Arria10 Dev Kit</td>
<td>Name of the board to be displayed when bootloader starts.</td>
</tr>
<tr>
<td>uboot.external_fpga_config</td>
<td>Boolean</td>
<td>False</td>
<td>Configure Uboot to wait early on in the boot sequence to allow the FPGA to be brought to user mode by either a JTAG download or an externally connected flash.</td>
</tr>
<tr>
<td>uboot.rbf_filename</td>
<td>String</td>
<td>socfpga.rbf</td>
<td>Full FPGA .rbf filename. This setting is ignored when the uboot.external_fpga_config setting is enabled.</td>
</tr>
</tbody>
</table>

continued...
### Table 11. Arria 10 Main BSP Settings Group for UEFI

<table>
<thead>
<tr>
<th>BSP Setting</th>
<th>Type</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>uboot.rbf_offset</td>
<td>Hexadecimal</td>
<td>0x7200000</td>
<td>RBF offset address in QSPI Flash.</td>
</tr>
<tr>
<td>uboot.disable_uboot_build</td>
<td>Boolean</td>
<td>False</td>
<td>Can be used to disable building Uboot, and just generate the Bootloader Device Tree file.</td>
</tr>
<tr>
<td>uboot.secureboot.enable_bootloader_encryption</td>
<td>Boolean</td>
<td>0</td>
<td>Encrypt Bootloader using key file specified.</td>
</tr>
<tr>
<td>uboot.secureboot.enable_bootloader_signing</td>
<td>Boolean</td>
<td>0</td>
<td>Sign Bootloader using the key pair file specified.</td>
</tr>
<tr>
<td>uboot.secureboot.encryption_key_file</td>
<td>String</td>
<td>encrypt.key</td>
<td>Key file used for Bootloader encryption.</td>
</tr>
<tr>
<td>uboot.secureboot.encryption_key_name</td>
<td>String</td>
<td>key1</td>
<td>Key Name to use within Key File for Bootloader Encryption.</td>
</tr>
<tr>
<td>uboot.secureboot.signing_key_fpga_offset</td>
<td>Hexadecimal</td>
<td>0x0</td>
<td>Offset from H2F Bridge Base Address (0xC0000000) to location of root-public-key.</td>
</tr>
<tr>
<td>uboot.secureboot.signing_key_pair_file</td>
<td>String</td>
<td>root_key.pem</td>
<td>Key Pair File to use when signing is enabled. You can generate this file with the command: 'make generate-signing-key-pair-file'.</td>
</tr>
<tr>
<td>uboot.secureboot.signing_key_type</td>
<td>String</td>
<td>user</td>
<td>Sign Bootloader using key pair file specified.</td>
</tr>
</tbody>
</table>

For more information about authentication and encryption, refer to the *Arria 10 SoC Secure Boot User Guide*.

**Related Links**

- Arria 10 SoC Secure Boot User Guide
  For more information about authentication and encryption
### 7.2.5.2.2 Arria 10 Bootloader MPU Firewall BSP Settings Group

**Table 12. Arria 10 Bootloader MPU Firewall BSP Settings Group**

<table>
<thead>
<tr>
<th>BSP Setting</th>
<th>Type</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>enable.mpuregion0enable</td>
<td>Boolean</td>
<td>True</td>
<td>Enable MPU Firewall Regions</td>
</tr>
<tr>
<td>enable.mpuregion1enable</td>
<td>False</td>
<td></td>
<td></td>
</tr>
<tr>
<td>enable.mpuregion2enable</td>
<td>False</td>
<td></td>
<td></td>
</tr>
<tr>
<td>enable.mpuregion3enable</td>
<td>False</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mpuregion0addr.base</td>
<td>Hexadecimal</td>
<td>0x0</td>
<td>MPU Firewall region bases</td>
</tr>
<tr>
<td>mpuregion1addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mpuregion2addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mpuregion3addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mpuregion0addr.limit</td>
<td>Hexadecimal</td>
<td>0xffff</td>
<td>MPU Firewall region limits</td>
</tr>
<tr>
<td>mpuregion1addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mpuregion2addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mpuregion3addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 7.2.5.2.3 Arria 10 Bootloader L3 Firewall BSP Settings Group

**Table 13. Arria 10 Bootloader L3 Firewall BSP Settings Group**

<table>
<thead>
<tr>
<th>BSP Setting</th>
<th>Type</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>enable.hpsregion0enable</td>
<td>Boolean</td>
<td>True</td>
<td>Enable L3 Firewall regions</td>
</tr>
<tr>
<td>enable.hpsregion1enable</td>
<td>False</td>
<td></td>
<td></td>
</tr>
<tr>
<td>enable.hpsregion2enable</td>
<td>False</td>
<td></td>
<td></td>
</tr>
<tr>
<td>enable.hpsregion3enable</td>
<td>False</td>
<td></td>
<td></td>
</tr>
<tr>
<td>enable.hpsregion4enable</td>
<td>False</td>
<td></td>
<td></td>
</tr>
<tr>
<td>enable.hpsregion5enable</td>
<td>False</td>
<td></td>
<td></td>
</tr>
<tr>
<td>enable.hpsregion6enable</td>
<td>False</td>
<td></td>
<td></td>
</tr>
<tr>
<td>enable.hpsregion7enable</td>
<td>False</td>
<td></td>
<td></td>
</tr>
<tr>
<td>hpsregion0addr.base</td>
<td>Hexadecimal</td>
<td>0x0</td>
<td>L3 Firewall region bases</td>
</tr>
<tr>
<td>hpsregion1addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>hpsregion2addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>hpsregion3addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>hpsregion4addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3 Use the Arria 10 BSP Firewall Setting Prefixes. Table 9 on page 68

4 Use the Arria 10 BSP Firewall Setting Prefixes. Table 9 on page 68
### Arria 10 Bootloader F2S Firewall BSP Settings Group

#### Table 14. Arria 10 Bootloader F2S Firewall BSP Settings Group

<table>
<thead>
<tr>
<th>BSP Setting5</th>
<th>Type</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>enable.fpga2sdram0region0</td>
<td>Boolean</td>
<td>True</td>
<td>Enable F2S Firewall regions</td>
</tr>
<tr>
<td>enable.fpga2sdram0region1</td>
<td></td>
<td>True</td>
<td></td>
</tr>
<tr>
<td>enable.fpga2sdram0region2</td>
<td></td>
<td>True</td>
<td></td>
</tr>
<tr>
<td>enable.fpga2sdram0region3</td>
<td></td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>enable.fpga2sdram1region0</td>
<td></td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>enable.fpga2sdram1region1</td>
<td></td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>enable.fpga2sdram1region2</td>
<td></td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>enable.fpga2sdram1region3</td>
<td></td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>enable.fpga2sdram2region0</td>
<td></td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>enable.fpga2sdram2region1</td>
<td></td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>enable.fpga2sdram2region2</td>
<td></td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>enable.fpga2sdram2region3</td>
<td></td>
<td>False</td>
<td></td>
</tr>
<tr>
<td>fpga2sdram0region0addr.base</td>
<td>Hexadecimal</td>
<td>0x0</td>
<td>F2S Firewall region bases</td>
</tr>
<tr>
<td>fpga2sdram0region1addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram0region2addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram0region3addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram1region0addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram1region1addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram1region2addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

4 Use the Arria 10 BSP Firewall Setting Prefixes. Table 9 on page 68

5 Use the Arria 10 BSP Firewall Setting Prefixes. Table 9 on page 68
<table>
<thead>
<tr>
<th>BSP Setting</th>
<th>Type</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>fpga2sdram1region1addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram1region2addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram1region3addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram2region0addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram2region1addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram2region2addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram2region3addr.base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram0region0addr.limit</td>
<td>Hexadecimal</td>
<td>0xffff</td>
<td>F2S Firewall region limits</td>
</tr>
<tr>
<td>fpga2sdram0region1addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram0region2addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram0region3addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram1region0addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram1region1addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram1region2addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram1region3addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram2region0addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram2region1addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram2region2addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fpga2sdram2region3addr.limit</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

5 Use the Arria 10 BSP Firewall Setting Prefixes. Table 9 on page 68
7.3 Second Stage Bootloader Image Tool (mkpimage)

The Second Stage Bootloader (SSBL) Image Tool (mkpimage) creates an Intel BootROM-compatible image of the Arria V and Cyclone V Preloader or Arria 10 Bootloader. The tool can also decode the header of previously generated images.

The mkpimage tool makes the following assumptions:

- The input file format is raw binary. You must use the `objcopy` utility provided with the GNU Compiler Collection (GCC) tool chain from the Mentor Graphics website to convert other file formats, such as Executable and Linking Format File (.elf), Hexadecimal (Intel-Format) File (.hex), or S-Record File (.srec), to a binary format.
- The output file format is binary.
- The tool always creates the output image at the beginning of the binary file. If the image must be programmed at a specific base address, you must supply the address information to the flash programming tool.
- The output file contains only Preloader or Bootloader images. Other images such as Linux, SRAM Object File (.sof) and user data are programmed separately using a flash programming tool or related utilities in the U-boot on the target system.

**Figure 48. Basic Operation of the mkpimage Tool**

![Diagram showing the basic operation of the mkpimage tool.](image)

### 7.3.1 Operation

The mkpimage tool runs on a host machine. The tool generates the header and CRC checksum and inserts them into the output image with the SSBL program image and its exception vector.

For certain flash memory tools, the position of the SSBL images must be aligned to a specific block size; the mkpimage tool generates any padding data that may be required.

The mkpimage tool optionally decodes and validates header information when given a pre-generated SSBL image.

As illustrated, the binary SSBL image is an input to the mkpimage tool. The compiler leaves an empty space between the SSBL exception vector and the program. The mkpimage tool overwrites this empty region with header information and calculates a checksum for the whole image.

When necessary, the mkpimage tool appends the padding data to the output image.

The mkpimage tool can operate with either one or four input files. Operation on four input files consists in processing each file individually, then concatenating the four resulted images.
### 7.3.2 Header File Format

The mkpimage header file format has two versions:

- Version 0, used for Cyclone V and Arria V SSBL (Preloader)
- Version 1, used for Arria 10 SSBL (Bootloader)

For Version 0, used for Cyclone V and Arria V Preloader, the header includes the following:

- Validation word (0x31305341)
- Version field (set to 0x0)
- Flags field (set to 0x0)
- Program length measured by the number of 32 bit words in the Preloader program
- 16-bit checksum of the header contents (0x40 – 0x49)

**Figure 49. Header Format Version 0**

For Version 1, used for Arria 10 Bootloader, the header includes the following:

- Validation word (0x31305341).
- Version field (set to 0x1).
- Flags field (set to 0x0).
- Header length, in bytes, set to 0x14 (20 bytes).
- Total program length (including the exception vectors and the CRC field) in bytes. For an image to be valid, length must be a minimum of 0x5C (92 bytes) and a maximum of 0x32000 (200KiB).
- Program entry offset relative to the start of header (0x40) and should be 32-bit word-aligned. Default is 0x14, any value smaller than that is invalid.
- 16-bit checksum of the header contents (0x40 – 0x51):

**Figure 50. Header Format Version 1**

The header checksum for both versions of the mkpimage header is the CRC checksum of the byte value from offset 0x0 to (n*4)-4 bytes where n is the program length.
The CRC is a standard CRC32 with the polynomial:
\[ x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x + 1 \].
There is no reflection of the bits and the initial value of the remainder is 0xFFFFFFFF and the final value is exclusive OR-ed with 0xFFFFFFFF.

7.3.3 Tool Usage

The mkimage tool has three usage models:
- Single image creation
- Quad image creation
- Single or quad image decoding

If an error is found during the make image process, the tool stops and reports the error. Possible error conditions include:
- For Cyclone V and Arria V Preloaders: input image is smaller than 81 bytes or larger than 60 KB.
- For Arria 10 Bootloaders: input image is smaller than 92 bytes or larger than 200 KB.

`mkpimage` invokes the tool; invoking the tool with the --help option provides a tool description and tool usage and option information.

```
$ mkpimage --help
mkpimage version 17.0
Description: This tool creates an Intel BootROM-compatible image of Second Stage Boot Loader (SSBL). The input and output files are in binary format. It can also decode and check the validity of previously generated image.
Usage:
Create quad image:
  mkpimage [options] -hv <num> -o <outfile> <infile> <infile> <infile> <infile>
Create single image:
  mkpimage [options] -hv <num> -o <outfile> <infile>
Decode single/quad image:
  mkpimage -d [-a <num>] <infile>
Options:
  -a (--alignment) <num>       : Address alignment in kilobytes for output image (64, 128, 256, etc.), default to 64 for header version 0 and 256 for header version 1, override if the NAND flash has a different block size. If outputting a single image, value of '0' is permitted to specify no flash block padding (needed for SSBL image encryption).
  -d (--decode)                : Flag to decode the header information from input file and display it
  -f (--force)                 : Flag to force decoding even if the input file is an unpadded image
  -h (--help)                  : Display this help message and exit
  -hv (--header-version) <num> : Header version to be created (Arria/Cyclone V = 0, Arria 10 = 1)
  -o (--output) <outfile>     : Output file, relative and absolute path supported
  -off (--offset) <num>       : Program entry offset relative to start of header (0x40), default to 0x14. Used for header version 1 only
  -v (--version)               : Display version and exit
```
7.3.4 Output Image Layout

7.3.4.1 Base Address

The bootable SSBL image must be placed at 0x0 for NAND and QSPI flash. For SD/MMC the image can also be placed at 0x0, but typically the image is placed at offset 0x0 in a custom partition of type 0xA2. The custom partition does not have a filesystem on it. The boot ROM is able to locate the partition using the MBR (Master Boot Record) located at 0x0 on the SD/MMC card.

The mkpimage tool always places the output image at the start of the output binary file, regardless of the target flash memory type. The flash programming tool is responsible for placing the image at the desired location on the flash memory device.

7.3.4.2 Size

For Cyclone V and Arria V, a single Preloader has a maximum 60 KB image size. You can store up to four preloader images in flash. If the boot ROM does not find a valid preloader image at the first location, it attempts to read an image from the next location and so on. To take advantage of this feature, program four preloader images in flash.

For Arria 10, a single Bootloader has a maximum 200 KB image size. You can store up to four Bootloader images in flash. If the boot ROM does not find a valid Bootloader image at the first location, it attempts to read the next one and so on. To take advantage of this feature, program four Bootloader images in flash.

7.3.4.3 Address Alignment

For Cyclone V and Arria V, every Preloader image has to be aligned to a 64KB boundary, except for NAND devices. For NAND devices, each Preloader image has to be aligned to the greater of 64 KB or NAND block size.

For Arria 10, every Bootloader image has to be aligned to a 256 KB boundary, except for NAND devices. For NAND devices, each Bootloader image has to be aligned to the greater of 256 KB or NAND block size.

The following tables present typical image layouts, that are used for QSPI, SD/MMC and NAND devices with NAND erase block size equal or less to 64 KB (for Cyclone V/Arria V) or 256 KB (for Arria 10).

Table 15. Typical Arria V/Cyclone V Preloader Image Layout

<table>
<thead>
<tr>
<th>Offset</th>
<th>Image</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x30000</td>
<td>Preloader Image 3</td>
</tr>
<tr>
<td>0x20000</td>
<td>Preloader Image 2</td>
</tr>
<tr>
<td>0x10000</td>
<td>Preloader Image 1</td>
</tr>
<tr>
<td>0x00000</td>
<td>Preloader Image 0</td>
</tr>
</tbody>
</table>
### Table 16. Typical Arria 10 Bootloader Image Layout

<table>
<thead>
<tr>
<th>Offset</th>
<th>Image</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xC0000</td>
<td>Bootloader Image 3</td>
</tr>
<tr>
<td>0x80000</td>
<td>Bootloader Image 2</td>
</tr>
<tr>
<td>0x40000</td>
<td>Bootloader Image 1</td>
</tr>
<tr>
<td>0x00000</td>
<td>Bootloader Image 0</td>
</tr>
</tbody>
</table>

The mkpimage tool is unaware of the target flash memory type. If you do not specify the block size, the default is 64 KB.

#### 7.3.4.3.1 NAND Flash

Each Preloader or Bootloader image occupies an integer number of blocks. A block is the smallest entity that can be erased, so updates to a particular boot image do not impact the other images.

For example for Cyclone V and Arria V, a single Preloader image has a maximum size of 64 KB. But it the NAND block is 128 KB, then the Preloader images will need to be located at 128 KB intervals.

#### 7.3.4.3.2 Serial NOR Flash

Each QSPI boot image occupies an integer number of sectors unless subsector erase is supported; this ensures that updating one image does not affect other images.

#### 7.3.4.3.3 SD/MMC

The master boot record, located at the first 512 bytes of the device memory, contains partition address and size information. The Preloader and Bootloader images are stored in partitions of type 0xA2. Other items may be stored in other partition types according to the target file system format.

You can use the fdisk tool to set up and manage the master boot record. When the fdisk tool partitions an SD/MMC device, the tool creates the master boot record at the first sector, with partition address and size information for each partition on the SD/MMC.

#### 7.3.4.4 Padding

The mkimage tool inserts a CRC checksum in the unused region of the image. Padding fills the remaining unused regions. The contents of the padded and unused regions of the image are undefined.

**Related Links**

  For more information, please refer to the Booting and Configuration chapter.
  For more information, please refer to the Booting and Configuration chapter.
  For more information, please refer to the Booting and Configuration chapter.
7.4 U-Boot Image Tool (mkimage)

Both the Preloader (for Arria V/ Cyclone V) and the Bootloader (for Arria 10) require the presence of the U-Boot image header at the beginning of the next stage boot image. Depending on usage scenario, other items that are loaded by either Preloader or Bootloader may also require the presence of the U-Boot image header.

The mkimage utility is delivered with SoC FPGA EDS and can be used to append the U-Boot image header to the next stage boot image or any other required files.

Figure 51. mkimage Header

The header consists of the following items:

- Image magic number - determines if the image is a valid boot image
- Image data size - the length of the image to be copied
- Data load address - the entry point of the boot image (not used for items that are not bootable images)
- Operating system - determines the type of image
- Image name - the name of the boot image
- Image CRC - the checksum value of the boot image

Figure 52. mkimage Header Layout

7.4.1 Tool Options

mkimage invokes the mkimage tool and the --help option provides the tool description and option information.

```
$ mkimage --help
Usage: mkimage [options] image
       mkimage [-D dtc_options] [-f fit-image.its|-F] fit-image
-D => set options for device tree compiler

Options:
-l ==> list image header information
-mkimage [-x] -A arch -O os -T type -C comp -a addr -e ep -n name -d
       data_file[…] image
-A ==> set architecture to 'arch'
-O ==> set operating system to 'os'
-T ==> set image type to 'type'
-C ==> set compression type 'comp'
-a ==> set load address to 'addr' (hex)
-e ==> set entry point to 'ep' (hex)
-n ==> set image name to 'name'
-d ==> use image data from 'datafile'
-x ==> set XIP (execute in place)
```
7.4.2 Usage Examples

Example 6. Creating a U-boot Image

```bash
mkimage -A arm -T firmware -C none -O u-boot -a 0x08000040 -e 0 -n "U-Boot 2014.10 for SOCFGPA board" -d u-boot.bin u-boot.img
```

Example 7. Creating a Bare-metal Application Image

```bash
mkimage -A arm -O u-boot -T standalone -C none -a 0x02100000 -e 0 -n "baremetal image" -d hello_world.bin hello_world.img
```

7.5 Building the Second Stage Bootloader

This section presents the details of how the bootable SSBL image is created, with the aid of the generated Makefile, for both Cyclone V and Arria V Preloader, and Arria 10 Bootloader.

7.5.1 Building the Cyclone V and Arria V Preloader

The following figure presents the Cyclone V and Arria V Preloader build flow, as performed by the generated Makefile when invoking `make`. In order to keep the illustration simple, the generated Makefile itself is not shown.

**Figure 53. Cyclone V/Arria V Preloader Build Flow**

Legend:
- Part of SoC FPGA EDS
The makefile performs the following tasks:

- Copies the generic preloader source code into `<bsp directory>/uboot-socfpga`
- Copies the generated BSP files and hardware handoff files to the source directory in `<bsp_directory>/uboot-socfpga/board/altera/socfpga_<device>`
- Configures the compiler tools to target an SoC FPGA
- Compiles the source files in `<bsp directory>/uboot-socfpga` with the user-specified cross compiler (specified in the BSP settings) and stores the generated preloader binary files in `<bsp_directory>/uboot-socfpga/spl`
- Converts the preloader binary file to a preloader image, `<bsp_directory>/preloader-mkpimage.bin`, with the `mkpimage` tool

The makefile contains the following targets:

- `make all` – compiles the preloader
- `make clean` – deletes preloader-mkpimage.bin from the `<bsp directory>`
- `make clean-all` – deletes `<bsp directory>`, including the source files in the directory

### 7.5.2 Building the Arria 10 Bootloader

The following figure presents the Arria 10 Bootloader build flow, as performed by the generated Makefile when invoking `make`. In order to keep the illustration simple, the generated Makefile itself is not shown.

**Figure 54. Arria 10 Bootloader Build Flow**

![Arria 10 Bootloader Build Flow Diagram]

**Legend**

- Part of SoC FPGA EDS

**Note:** For this release of the tools, the U-Boot compilation is only supported on Linux host machines. On Windows machines, the U-Boot compilation is not supported, and the bootloader must be generated with compilation disabled (with `--set uboot.disable_uboot_build set to true` or from `bsp-editor` interface). In this case, a pre-built version of U-Boot is used. The only limitation is that the U-Boot sources cannot be modified. Since the U-Boot configuration is contained in the bootloader device tree, this should not be a problem in most situations. However, if U-Boot source customization is required, a Linux host machine needs to be used.
Note: The Bootloader needs to be recompiled only when the boot source is changed (SD/MMC and QSPI are currently supported). The Bootloader does not need to be recompiled when other settings are changed, as those settings are encapsulated in the Bootloader Device Tree.

7.5.2.1 U-Boot Build Flow

The U-Boot makefile performs the following tasks:

- Copies the bootloader source code into `<bsp directory>/uboot-socfpga`
- Configures the bootloader to target the Arria 10 SoC
- Compiles the source files in `<bsp directory>/uboot-socfpga` and creates the Bootloader binary `<bsp directory>/uboot-socfpga/uboot.bin`
- Compiles the bootloader device tree source file by using `dtc` (Device Tree Compiler) into `<bsp directory>/devicetree.dtb`
- Concatenates the bootloader device tree binary and the bootloader binary files into a combined binary file `<bsp directory>/u-boot_w_dtb.bin`
- Converts the combined binary file to a bootable combined image, `<bsp directory>/uboot_w_dtb-mkpimage.bin`, with the `mkpimage` tool

The U-Boot makefile contains the following targets:

- make all – builds everything
- make src – copies the bootloader source code folder
- make uboot – builds the bootloader binary
- make dtb – compiles the bootloader device tree source to device tree binary
- make clean – deletes all built files
- make clean-all – deletes all built files, and the bootloader source code folder

7.5.2.2 UEFI Build Flow

The makefile performs the following tasks:

- Copies the UEFI source code into `<bsp directory>/uefi-socfpga`
- Configures the UEFI to target the Arria 10 SoC.
- Compiles the bootloader device tree source file by using the Device Tree Compiler (dtc) into `<bsp directory>/devicetree.dtb`
- Compiles the UEFI bootloader, concatenates the device tree and creates a bootable image in `<bsp directory>/uefi-socfpga/Build/PEI.ROM`. This is the equivalent of `uboot_w_dtb-mkpimage.bin`.

For more information about UEFI bootloader, refer to the "UEFI Bootloader" page on the Intel FPGA Wiki.

Related Links

Altera Wiki

For more information about UEFI bootloader, refer to the "UEFI Bootloader" page.
### 7.6 Boot Tools User Guide Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| May 2017      | 2017.05.08 | • Intel FPGA rebranding  
• Rebranded paths and tools for the Standard and Professional versions |
| November 2016 | 2016.11.7 | Added an "UEFI Build Flow" section                                                            |
| May 2016      | 2016.05.27 | Added a link to the Arria 10 SoC Secure Boot User Guide                                        |
| February 2016 | 2016.02.17 | • Updated the help definition for `mkpimage` in the "Tools Usage" and "Tool Options" sections  
• Updated the Arria 10 Main BSP Settings Group table                                           |
| August 2015   | 2015.08.06 | Added Arria 10 support                                                                         |
The Intel SoC FPGA Hardware Library (HWLIB) was created to address the needs of low-level software programmers who require full access to the configuration and control facilities of SoC FPGA hardware. An additional purpose of the HWLIB is to mitigate the complexities of managing the operation of a sophisticated, multi-core application processor and its integration with hardened IP peripheral blocks and programmable logic in a SoC architecture.

Within the context of the SoC HW/SW ecosystem, the HWLIB is capable of supporting software development in conjunction with full featured operating systems or standalone bare-metal programming environments. The relationship of the HWLIB within a complete SoC HW/SW environment is illustrated in the above figure.

The HWLIB provides a symbolic register abstraction layer known as the SoC Abstraction Layer (SoCAL) that enables direct access and control of HPS device registers within the address space. This layer is necessary for enabling several key stakeholders (boot loader developers, driver developers, board support package developers, debug agent developers, and board bring-up engineers) requiring a precise degree of access and control of the hardware resources.

The HWLIB also deploys a set of Hardware Manager (HW Manager) APIs that provides more complex functionality and drivers for higher level use case scenarios.

The HWLIB has been developed as a source code distribution. The intent of this model is to provide a useful set of out-of-the-box functionality and to serve as a source code reference implementation that a user can tailor accordingly to meet their target system requirements.
The capabilities of the HWLIB are expected to evolve and expand over time particularly as common use case patterns become apparent from practical application in actual systems.

In general, the HWLIB assumes to be part of the system software that is executing on the Hard Processor System (HPS) in privileged supervisor mode and in the secure state.

The anticipated HWLIB clients include:
- Bare-Metal application developers
- Custom preloader and boot loader software developers
- Board support package developers
- Diagnostic tool developers
- Software driver developers
- Debug agent developers
- Board bring-up engineers
- Other developers requiring full access to SoC FPGA hardware capabilities

8.1 Feature Description

This section provides a description of the operational features and functional capabilities present in the HWLIB. An overview and brief description of the HWLIB architecture is also presented.

The HWLIB is a software library architecturally comprised of two major functional components:
- SoC Abstraction Layer (SoCAL)
- Hardware Manager (HW Manager)

8.1.1 SoC Abstraction Layer (SoCAL)

The SoC Abstraction Layer (SoCAL) presents the software API closest to the actual HPS hardware. Its purpose is to provide a logical interface abstraction and decoupling layer to the physical devices and registers that comprise the hardware interface of the HPS.

The SoCAL provides the benefits of:
- A logical interface abstraction to the HPS physical devices and registers including the bit-fields comprising them.
- A loosely coupled software interface to the underlying hardware that promotes software isolation from hardware changes in the system address map and device register bit field layouts.
8.1.2 Hardware Manager (HW Manager)

The Hardware Manager (HW Manager) component provides a group of functional APIs that address more complex configuration and operational control aspects of selected HPS resources.

The HW Manager functions have the following characteristics:

- Functions employ a combination of low level device operations provided by the SoCAL executed in a specific sequence to effect a desired operation.
- Functions may employ cross functional (such as from different IP blocks) device operations to implement a desired effect.
- Functions may have to satisfy specific timing constraints for the application of operations and validation of expected device responses.
- Functions provide a level of user protection and error diagnostics through parameter constraint and validation checks.

The HW Manager functions are implemented using elemental operations provided by the SoCAL API to implement more complex functional capabilities and services. The HW Manager functions may also be implemented by the compound application of other functions in the HW Manager API to build more complex operations (for example, software controlled configuration of the FPGA).

8.2 Hardware Library Reference Documentation

Reference documentation for the SoCAL API and HW Manager API are distributed as part of the Intel SoC FPGA EDS Toolkit; and are accessible online, in HTML format, from any web browser.

The locations of the online SoC FPGA Hardware Library (HWLIB) Reference Documentation are:

- SoC Abstraction Layer (SoCAL) API Reference Documentation:

8.3 System Memory Map

The addresses of the HPS hard IP modules are accessible through the provided SoCAL macros. SoCAL also provides macros for accessing the individual registers and register fields of the HPS hard IP modules.

For the FPGA IP modules, the macros for accessing IP registers and register fields are usually part of the IP deliverables. However, the actual IP modules-based addresses are often changed at system integration time, in the Qsys tool.

The tool "sopc-create-header-files" can be used to create a C include file with the bases addresses of all the IP modules residing in the FPGA fabric.
The tool is part of Quartus Prime Standard Edition, and not of SoC FPGA EDS. The tool can be invoked from the SoC FPGA EDS Embedded Command Shell once Quartus Prime Standard Edition is installed.

The basic usage of the tool is to invoke it with the .sopcinfo file as a single parameter. For example, in order to generate the include files for the Arria 10 GHRD, the following command can be executed in that folder: `sopc-create-header-files ghrd_10as066n2.sopcinfo`.

The tool creates a separate include file for each of the masters in the system, showing the system addresses from that master's point of view. Use the file `<hps_component_name>_a9_0.h` for HPS software development, as it shows the system addresses from the HPS point of view.

The following example demonstrates how to use the tool to generate only the file that shows the HPS A9 Core 0 point of view:

```
sopc-create-header-files ghrd_10as066n2.sopcinfo --module\n arria10_hps_0_arm_a9_0 --single arria10_hps_0_arm_a9_0.h
```

This creates just one file, called "arria10_hps_0_arm_a9_0.h".

You can also run "sopc-create-header-files --help" for more details about the tool, or refer to Quartus Prime Standard Edition documentation.

### 8.4 Hardware Library Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| May 2017     | 2017.05.08 | • Intel FPGA rebranding  
• Rebranded paths and tools for the Standard and Professional versions |
| November 2016 | 2016.11.07 | Maintenance release                                                      |
| May 2016     | 2016.05.27 | Maintenance release                                                      |
| February 2016 | 2016.02.17 | • Updated the HW Library figure  
• Added a new section called "System Memory Map" |
| August 2015  | 2015.08.06 | Added Arria 10 support                                                  |
The Quartus Prime software and Quartus Prime Programmer include the HPS flash programmer. Hardware designs, such as HPS, incorporate flash memory on the board to store FPGA configuration data or HPS program data. The HPS flash programmer programs the data into a flash memory device connected to an Intel FPGA SoC. The programmer sends file contents over an Intel download cable, such as the USB-Blaster™ II, to the HPS and instructs the HPS to write the data to the flash memory.

The HPS flash programmer programs the following content types to flash memory:

- **HPS software executable files** — Many systems use flash memory to store non-volatile program code or firmware. HPS systems can boot from flash memory.
  
  *Note:* The HPS Flash Programmer is mainly intended to be used for programming the Preloader image to QSPI or NAND flash. Because of the low speed of operation, it is not recommended to be used for programming large files.

- **FPGA configuration data** — At system power-up, the FPGA configuration controller on the board or HPS read FPGA configuration data from the flash memory to program the FPGA. The configuration controller or HPS may be able to choose between multiple FPGA configuration files stored in flash memory.

- **Other arbitrary data files** — The HPS flash programmer programs a binary file to any location in a flash memory for any purpose. For example, a HPS program can use this data as a coefficient table or a sine lookup table.

The HPS flash programmer programs the following memory types:

- Quad serial peripheral interface (QSPI) Flash
- Open NAND Flash Interface (ONFI) compliant NAND Flash

### 9.1 HPS Flash Programmer Command-Line Utility

You can run the HPS flash programmer directly from the command line.

- For the Quartus Prime software, the HPS flash programmer is located in the `<Quartus Prime installation directory>/quartus/bin` directory.
- For the SoC FPGA EDS software, the HPS flash programmer is located in the `<SoC FPGA EDS installation directory>/qprogrammer/bin` directory.

### 9.2 How the HPS Flash Programmer Works

The HPS flash programmer is divided into a host and a target. The host portion runs on your computer and sends flash programming files and programming instructions over a download cable to the target. The target portion is the HPS in the SoC. The target accepts the programming data flash content and required information about the target flash memory device sent by the host. The target writes the data to the flash memory device.
The HPS flash programmer determines the type of flash to program by sampling the boot select (BSEL) pins during cold reset; you do not need to specify the type of flash to program.

9.3 Using the Flash Programmer from the Command Line

9.3.1 HPS Flash Programmer

The HPS flash programmer utility can erase, blank-check, program, verify, and examine the flash. The utility accepts a Binary File with a required ".bin" extension.

The HPS flash programmer command-line syntax is:

```
quartus_hps <options> <file.bin>
```

*Note:* The HPS flash programmer uses byte addressing.

Table 17. HPS Flash Programmer Parameters

<table>
<thead>
<tr>
<th>Option</th>
<th>Short Option</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
</table>
| --cable  | -c           | Yes      | This option specifies what download cable to use. To obtain the list of programming cables, run the command "jtagconfig". It will list the available cables, like in the following example:

```
jtagconfig
1) USB-Blaster [USB-0]
2) USB-Blaster [USB-1]
3) USB-Blaster [USB-2]
```

The "-c" parameter can be the number of the programming cable, or its name. The following are valid examples for the above case:

```
-c 1
-c "USB-Blaster [USB-2]"
```

| --device | -d           | Yes (if there are multiple HPS devices in the chain) | This option specifies the index of the HPS device. The tool will automatically detect the chain and determine the position of the HPS device; however, if there are multiple HPS devices in the chain, the targeted device index must be specified. |

*continued...*
<table>
<thead>
<tr>
<th>Option</th>
<th>Short Option</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>--operation</td>
<td>-o</td>
<td>Yes</td>
<td>This option specifies the operation to be performed. The following operations are supported:  • I: Read IDCODE of SOC device and discover Access Port  • S: Read Silicon ID of the flash  • E: Erase flash  • B: Blank-check flash  • P: Program flash  • V: Verify flash  • EB: Erase and blank-check flash  • BP: Program &lt;BlankCheck&gt; flash  • PV: Program and verify flash  • BPV: Program (blank-check) and verify flash  • X: Examine flash</td>
</tr>
<tr>
<td>--addr</td>
<td>-a</td>
<td>Yes (if the start address is not 0)</td>
<td>This option specifies the start address of the operation to be performed.</td>
</tr>
<tr>
<td>--size</td>
<td>-s</td>
<td>No</td>
<td>This option specifies the number of bytes of data to be performed by the operation. size is optional.</td>
</tr>
<tr>
<td>--repeat</td>
<td>-t</td>
<td>No</td>
<td>These options must be used together. The HPS BOOT flow supports up to four images where each image is identical and these options duplicate the operation data; therefore you do not need eSW to create a large file containing duplicate images. repeat specifies the number of duplicate images for the operation to perform. interval specifies the repeated address. The default value is 64 kilobytes (KB). repeat and interval are optional.</td>
</tr>
<tr>
<td>--interval</td>
<td>-i</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 9.3.2 HPS Flash Programmer Command Line Examples

Type `quartus_hps --help` to obtain information about usage. You can also type `quartus_hps --help=<option>` to obtain more details about each option. For example "quartus_hps --help=o".

**Example 8. Program File to Address 0 of Flash**

`quartus_hps -c 1 -o P input.bin` programs the input file (`input.bin`) into the flash, starting at flash address 0 using a cable M.

**Example 9. Program First 500 Bytes of File to Flash (Decimal)**

`quartus_hps -c 1 -o PV -a 1024 -s 500 input.bin` programs the first 500 bytes of the input file (`input.bin`) into the flash, starting at flash address 1024, followed by a verification using a cable M.

*Note:* Without the prefix 0x for the flash address, the tool assumes it is decimal.

**Example 10. Program First 500 Bytes of File to Flash (Hexadecimal)**

`quartus_hps -c 1 -o PV -a 0x400 -s 500 input.bin` programs the first 500 bytes of the input file (`input.bin`) into the flash, starting at flash address 1024, followed by a verification using a cable M.
Note: With the prefix 0x, the tool assumes it is hexadecimal.

Example 11. Program File to Flash Repeating Twice at Every 1 MB
quartus_hps –c 1 –o BPV –t 2 –i 0x100000 input.bin programs the input file (input.bin) into the flash, using a cable M. The operation repeats itself twice at every 1 megabyte (MB) of the flash address. Before the program operation, the tool ensures the flash is blank. After the program operation, the tool verifies the data programmed.

Example 12. Erase Flash on the Flash Addresses
quartus_hps –c 1 –o EB input.bin erases the flash on the flash addresses where the input file (input.bin) resides, followed by a blank-check using a cable M.

Example 13. Erase Full Chip
quartus_hps –c 1 –o E erases the full chip, using a cable M. When no input file (input.bin) is specified, it will erase all the flash contents.

Example 14. Erase Specified Memory Contents of Flash
quartus_hps –c 1 –o E –a 0x100000 –s 0x400000 erases specified memory contents of the flash. For example, 4 MB worth of memory content residing in the flash address, starting at 1 MB, are erased using a cable M.

Example 15. Examine Data from Flash
quartus_hps –c 1 –o X –a 0x98679 –s 56789 output.bin examines 56789 bytes of data from the flash with a 0x98679 flash start address, using a cable M.

9.4 Supported Memory Devices

Table 18. QSPI Flash

<table>
<thead>
<tr>
<th>Flash Device</th>
<th>Manufacturer</th>
<th>Device ID</th>
<th>DIE #</th>
<th>Density (Mb)</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>M25P40</td>
<td>Micron</td>
<td>0x132020</td>
<td>1</td>
<td>4</td>
<td>3.3</td>
</tr>
<tr>
<td>N25Q064</td>
<td>Micron</td>
<td>0x17BA20</td>
<td>1</td>
<td>64</td>
<td>3.3</td>
</tr>
<tr>
<td>N25Q128</td>
<td>Micron</td>
<td>0x18BA20</td>
<td>1</td>
<td>128</td>
<td>3.3</td>
</tr>
<tr>
<td>N25Q128</td>
<td>Micron</td>
<td>0x18BB20</td>
<td>1</td>
<td>128</td>
<td>1.8</td>
</tr>
<tr>
<td>N25Q256</td>
<td>Micron</td>
<td>0x19BA20</td>
<td>1</td>
<td>256</td>
<td>3.3</td>
</tr>
<tr>
<td>N25Q256</td>
<td>Micron</td>
<td>0x19BB20</td>
<td>1</td>
<td>256</td>
<td>1.8</td>
</tr>
<tr>
<td>MT25QL512</td>
<td>Micron</td>
<td>0x20BA20</td>
<td>1</td>
<td>512</td>
<td>3.3</td>
</tr>
<tr>
<td>N25Q512</td>
<td>Micron</td>
<td>0x20BA20</td>
<td>2</td>
<td>512</td>
<td>3.3</td>
</tr>
<tr>
<td>MT25QU512</td>
<td>Micron</td>
<td>0x20BB20</td>
<td>1</td>
<td>512</td>
<td>1.8</td>
</tr>
<tr>
<td>N25Q512A</td>
<td>Micron</td>
<td>0x20BB20</td>
<td>2</td>
<td>512</td>
<td>1.8</td>
</tr>
<tr>
<td>N25Q00AA</td>
<td>Micron</td>
<td>0x21BA20</td>
<td>4</td>
<td>1024</td>
<td>3.3</td>
</tr>
<tr>
<td>MT25QU01G</td>
<td>Micron</td>
<td>0x21BB20</td>
<td>2</td>
<td>1024</td>
<td>1.8</td>
</tr>
<tr>
<td>N25Q00AA</td>
<td>Micron</td>
<td>0x21BB20</td>
<td>4</td>
<td>1024</td>
<td>1.8</td>
</tr>
<tr>
<td>MT25QL02G</td>
<td>Micron</td>
<td>0x22BA20</td>
<td>4</td>
<td>2048</td>
<td>3.3</td>
</tr>
</tbody>
</table>

continued...
<table>
<thead>
<tr>
<th>Flash Device</th>
<th>Manufacturer</th>
<th>Device ID</th>
<th>DIE #</th>
<th>Density (Mb)</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>MT25QU02G</td>
<td>Micron</td>
<td>0x22BB20</td>
<td>4</td>
<td>2048</td>
<td>1.8</td>
</tr>
<tr>
<td>S25FL128S</td>
<td>Cypress</td>
<td>0x182001</td>
<td>1</td>
<td>128 (64KB Sectors)</td>
<td>3.3</td>
</tr>
<tr>
<td>S25FL128S</td>
<td>Cypress</td>
<td>0x182001</td>
<td>1</td>
<td>128 (256KB Sectors)</td>
<td>3.3</td>
</tr>
<tr>
<td>S25FL256S</td>
<td>Cypress</td>
<td>0x190201</td>
<td>1</td>
<td>256 (64KB Sectors)</td>
<td>3.3</td>
</tr>
<tr>
<td>S25FL256S</td>
<td>Cypress</td>
<td>0x190201</td>
<td>1</td>
<td>256 (256KB Sectors)</td>
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<tr>
<td>S25FL512S</td>
<td>Cypress</td>
<td>0x200201</td>
<td>1</td>
<td>512</td>
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<tr>
<td>MX25L2563S</td>
<td>Macronix</td>
<td>0x1920C2</td>
<td>1</td>
<td>256</td>
<td>3</td>
</tr>
<tr>
<td>MX66L1G4S</td>
<td>Macronix</td>
<td>0x1B20C2</td>
<td>1</td>
<td>1024</td>
<td>3</td>
</tr>
<tr>
<td>MX66U5123S</td>
<td>Macronix</td>
<td>0x3A25C2</td>
<td>1</td>
<td>512</td>
<td>1.8</td>
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</table>

Table 19. ONFI Compliant NAND Flash

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>MFC ID</th>
<th>Device ID</th>
<th>Density (Gb)</th>
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<tr>
<td>Micron</td>
<td>0x2C</td>
<td>0x68</td>
<td>32</td>
</tr>
<tr>
<td>Micron</td>
<td>0x2C</td>
<td>0x48</td>
<td>16</td>
</tr>
<tr>
<td>Micron</td>
<td>0x2C</td>
<td>0xA1</td>
<td>8</td>
</tr>
<tr>
<td>Micron</td>
<td>0x2C</td>
<td>0xF1</td>
<td>8</td>
</tr>
</tbody>
</table>

**Note:** The above table contains just examples of supported devices. The HPS Flash Programmer supports all ONFI compliant NAND flash devices that are supported by the HPS QSPI Flash Controller.

**Note:** The HPS Flash Programmer supports the Cyclone V, Arria V and Arria 10 SoC devices. For more information, refer to the "Supported Flash Devices for Cyclone V and Arria V SoC" and the "Supported Flash Devices for Arria 10 SoC" web pages.

**Related Links**
- Supported Flash Devices for Cyclone V and Arria V SoC
- Supported Flash Devices for Arria 10 SoC

### 9.5 HPS Flash Programmer User Guide Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
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<td>May 2017</td>
<td>2017.05.08</td>
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<tr>
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<td></td>
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</tr>
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<tr>
<td>May 2016</td>
<td>2016.05.27</td>
<td>Maintenance release</td>
</tr>
<tr>
<td>February 2016</td>
<td>2016.02.17</td>
<td>Added QSPI Flash part number to the QSPI Flash table in the &quot;Supported Memory Devices&quot; chapter</td>
</tr>
<tr>
<td>August 2015</td>
<td>2015.08.06</td>
<td>Added Arria 10 support</td>
</tr>
</tbody>
</table>
10 Bare-Metal Compilers

The SoC FPGA EDS provides two bare-metal compilers:

- ARM Bare-metal Compiler (ARMCC)

The ARM Bare-metal Compiler (ARMCC) documentation is integrated in DS-5, like with all the DS-5 components.

Related Links

- Mentor Graphics
- SoC EDS Getting Started Guides

10.1 Mentor Code Sourcery Compiler

The bare-metal compiler that is shipped with the SoC FPGA EDS is the Mentor Graphics Sourcery™ CodeBench Lite. For the current version, refer to Table 1 on page 5, located in the "Differences Between Standard and Professional Editions" section.

For more information on the Sourcery CodeBench Lite Edition and to download the latest version of the tools, refer to the Mentor Graphics website.

The compiler is a GCC-based arm-altera-eabi port that targets the ARM processor, assumes bare-metal operation, and uses the standard ARM embedded-application binary interface (EABI) conventions.

The bare-metal compiler is installed as part of the SoC FPGA EDS installation in the following folder:

```<SoC FPGA EDS installation directory>/host_tools/mentor/gnu/arm/baremetal.```

The Embedded Command Shell sets the correct environment PATH variables for the bare-metal compilation tools to be invoked. You can open the shell from the `<SoC FPGA EDS installation directory>`. After starting the shell, commands like arm-altera-eabi-gcc can be invoked directly. When the ARM DS-5 for Intel SoC FPGA Edition environment is started from the embedded command shell, it inherits the environment settings, and it can call these compilation tools directly.

You can also use the full path to the compilation tools:

```<SoC FPGA EDS installation directory>/host_tools/mentor/gnu/arm/baremetal/bin.```
The bare-metal compiler is installed with full documentation, located at:

```
<SoC FPGA EDS installation directory>/host_tools/mentor/gnu/arm/baremetal/share/doc/sourceryg++-arm-altera-eabi.
```

The documentation is offered in four different formats to accommodate various user preferences:
- HTML files
- Info files
- Man pages
- PDF files

Among the provided documents are:
- Compiler manual
- Assembler manual
- Linker manual
- Binutils manual
- GDB manual
- Getting Started Guides
- Libraries Manual

**Related Links**

Differences Between Standard and Professional Editions on page 4

### 10.2 Bare-Metal Compilers Document Revision History

<table>
<thead>
<tr>
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<th>Changes</th>
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| May 2017     | 2017.05.08 | • Intel FPGA rebranding  
              |                     | • Rebranded paths and tools for the Standard and Professional versions |
| November 2016| 2016.11.07 | Added a "Mentor Code Sourcery Compiler” section                           |
| May 2016     | 2016.05.27 | Maintenance release                                                       |
| February 2016| 2016.02.17 | Updated the compiler version for Mentor Graphics Sourcery CodeBench Lite Edition |
| August 2015  | 2015.08.06 | Added Arria 10 support                                                    |

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6 The Getting Started Guides are located on the "SoCEDSGettingStarted" page on the Intel FPGA Wiki.
11 SD Card Boot Utility

The SoC FPGA EDS SD card boot utility is a tool for updating the boot software on an SD card.

The Preloader is typically stored in a custom partition (with type = 0xA2) on the SD card. Optionally the next boot stage (usually the Bootloader) can also be stored on the same custom partition.

Since it is a custom partition, without a file-system, the Preloader and/or Bootloader cannot be updated by copying the new file to the card; and a software tool is needed.

The SD card boot utility allows the user to update the Preloader and/or Bootloader on a physical SD card or a disk image file. The utility is not intended to create a new bootable SD card or disk image file from scratch. In order to do that, it is recommended to use `fdisk` on a Linux host OS.

Related Links
Linux Software Development Tools on page 97

11.1 Usage Scenarios

This utility is intended to update boot software on that resides on an existing:

- Existing SD card
- Existing disk image file

The tool supports updating the following:

- Cyclone V and Arria V Preloader
- Cyclone V and Arria V Bootloader
- Arria 10 Bootloader

**Note:** For Cyclone V and Arria V, the Preloader file needs to have the mkpimage header, as required by the boot ROM, and the Bootloader file needs to have the mkimage header, as required by the Preloader.

**Note:** For Arria 10, the Bootloader needs to have the mkpimage header, as required by BootROM.

**Note:** Both mkpimage and mkimage tools are delivered as part of SoC FPGA EDS.

The tool only updates the custom partition that stores the Intel SoC boot code. The rest of the SD card or disk image file is not touched. This includes the Master Boot Record (MBR) and any other partitions (FAT, EXT3 etc) and free space.
**Warning:** The users of this tool need administrative or root access to their computer to use this tool to write to physical SD cards. These rights are not required when only working with disk image files. Please contact the IT department if you do not have the proper rights on your PC.

### 11.2 Tool Options

The utility is a command line program. The table describes all the command line options; and the figure shows the `--help` output from the tool.

<table>
<thead>
<tr>
<th>Command line Argument</th>
<th>Required?</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>-p filename</code></td>
<td>Optional</td>
<td>Specifies Preloader file to write</td>
</tr>
<tr>
<td><code>-b filename</code></td>
<td>Optional</td>
<td>Specifies Cyclone V or Arria V Bootloader file to write</td>
</tr>
<tr>
<td><code>-B filename</code></td>
<td>Optional</td>
<td>Specifies Arria 10 Bootloader file to write</td>
</tr>
<tr>
<td><code>-a write</code></td>
<td>Required</td>
<td>Specifies action to take. Only &quot;write&quot; action is supported. Example: &quot;-a write&quot;</td>
</tr>
<tr>
<td><code>disk_file</code></td>
<td>Required(unless -d option is used)</td>
<td>Specifies disk image file or physical disk to write to. A disk image file is a file that contains all the data for a storage volume including the partition table. This can be written to a physical disk later with another tool. For physical disks in Linux, just specify the device file. For example:/dev/mmcblk0 For physical disks in Windows, specify the physical drive path such as \physicaldrive2 or use the drive letter option(-d) to specify a drive letter. The drive letter option is the easiest method in Windows</td>
</tr>
<tr>
<td><code>-d</code></td>
<td>Optional</td>
<td>specify disk drive letter to write to. Example: &quot;-d E&quot;. When using this option, the disk_file option cannot be specified.</td>
</tr>
<tr>
<td><code>-h</code></td>
<td>Optional</td>
<td>Displays help message and exits</td>
</tr>
<tr>
<td><code>--version</code></td>
<td>Optional</td>
<td>Displays script version number and exits</td>
</tr>
</tbody>
</table>

**Sample Output from Utility**

```bash
$ alt-boot-disk-util --help
Alterra Boot Disk Utility
Copyright (C) 1991-2014 Altera Corporation

Usage:
#write preloader to disk
  alt-boot-disk-util -p preloader -a write disk_file

#write bootloader to disk
  alt-boot-disk-util -b bootloader -a write disk_file

#write BOOTloader and PREloader to disk
  alt-boot-disk-util -p preloader -b bootloader -a write disk_file
```
#write Arria10 Bootloader to disk
    alt-boot-disk-util -B a10bootloader -a write disk_file

#write BOOTloader and PREloader to disk drive 'E'
    alt-boot-disk-util -p preloader -b bootloader -a write -d E

Options:
- --version show program's version number and exit
- -h, --help show this help message and exit
- -b FILE, --bootloader=FILE bootloader image file'
- -p FILE, --preloader=FILE preloader image file'
- -a ACTION, --action=ACTION only supports 'write' action'
- -B FILE, --a10-bootloader=FILE arria10 bootloader image file
- -d DRIVE, --drive=DRIVE specify disk drive letter to write to

11.3 SD Card Boot Utility Document Revision History

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| February 2016| 2016.02.17| Maintenance release                                                      |
| August 2015  | 2015.08.06| Added Arria 10 support                                                  |
12 Linux Software Development Tools

The Linux software development tools are listed below. The Linux compiler and the Linux device tree generator are described in the following sections of this chapter.

- Linux compiler
- SD card boot utility
- Linux device tree generator (DTG)

Related Links
SD Card Boot Utility on page 94
- The SoC FPGA EDS SD card boot utility is a tool for updating the boot software on an SD card.

12.1 Linux Compiler

The Linaro Linux compiler is shipped with the SoC FPGA EDS. For the current version, refer to Table 1 on page 5, located in the "Differences Between Standard and Professional Editions" section.

For more information about the Linux compiler and to download the latest version of the tools, refer to the download page at the Linaro website.

The compiler is a GCC-based arm-linux-gnueabihf port. It targets the ARM processor, it assumes the target platform is running Linux, and it uses the GNU embedded-application binary interface (EABI) hard-float (HF) conventions.

The Linux compiler is installed as part of the ARM DS-5 for Intel SoC FPGA Edition, which is installed as part of the SoC FPGA EDS. The compilation tools are located at:

```
<SoC FPGA EDS installation directory>/ds-5/bin.
```

The Linux compiler is installed with full documentation, located at:

```
```

The documents are provided as HTML files. Some of the provided documents are:

- Compiler manual
- Assembler manual
- Linker manual
- Binutils manual
- GDB manual
- Getting Started Guide
12.2 Linux Device Tree Generator

A device tree is a data structure that describes the underlying hardware to an operating system - primarily Linux. By passing this data structure to the OS kernel, a single OS binary may be able to support many variations of hardware. This flexibility is particularly important when the hardware includes an FPGA.

The Linux Device Tree Generator (DTG) tool is part of Intel SoC FPGA EDS and is used to create linux device trees for SoC systems that contain FPGA designs created using Qsys. The generated device tree describes the HPS peripherals, selected FPGA Soft IP, and peripherals that are board dependent.

Note: The Arria 10 Bootloader also has an associated Device Tree called Bootloader Device Tree that is created and managed by the BSP Editor tool.

Warning: The Linux Device Tree Generator is tested with and supports only the Linux kernel version targeted by the associated GSRD. It is not recommended to use the Linux Device Tree Generator if your design targets a different Linux kernel version. Instead, it is recommended to manage the Device Tree manually by using the Device Tree files provided by the kernel as a baseline, and by adding the FPGA IP and board information manually.

Related Links
- Intel FPGA Wiki
  For more information about the Linux DTG, refer to the Intel FPGA Wiki website.
- Linux Device Tree Generator User Guide
  For more details, navigate to the Device Tree Generator User Guide located on the Device Tree Generator Documentation page on the Rocketboards website.

12.3 Linux Software Development Tools Document Revision History

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</tr>
</tbody>
</table>
13 Support and Feedback

Intel values your feedback. Please contact your Intel TSFAE or submit a service request at myAltera to report software bugs, potential enhancements, or obtain any additional information.

Related Links

- SoCEDSGettingStarted
  For more information about getting started, refer to the SoCEDSGettingStarted page on the Intel FPGA Wiki.
- myAltera Account Sign In

13.1 Support and Feedback Document Revision History

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