White Paper

# Stratix III FPGA Signal Integrity

*As devices move towards faster switching speed and higher pin counts, signal and power integrity become crucial, making or breaking a system. Chip designs that work perfectly for 90-nm process technology may no longer be good enough for a 65-nm chip. Poor signal integrity causes poor reliability, degrades system performance, and, worst of all, system failures. Numerous enhancements have been implemented on Stratix® III FPGAs to improve signal and power integrity performance over the previous generation Stratix II family. These include die- and package-level signal return paths optimized with an 8:1:1 user I/O to ground/power ratio to reduce loop inductance, an improved decoupling scheme, dynamic on-chip termination (OCT), programmable LVDS buffer, and new control features for slew rate and staggered output delay that enable the designer to control the noise level of the device.*

*This white paper discusses how the new features and enhancements of Altera® Stratix III FPGAs address these issues and benefit customers' systems by improving signal and power integrity and simplifying printed circuit board (PCB) design.*

## Introduction

Today's systems demand faster performance with higher bandwidth, pushing devices towards faster switching speeds and higher pin counts-in FPGAs in particular, the pin count can increase by hundreds. With systems running at gigahertz speeds, timing margins are decreasing, while edge rates for devices are increasing, so the impact that parasitic capacitance and inductance have on device signal and power integrity is of great concern to the designer. Phenomena such as crosstalk, ringing, simultaneous switching noise (SSN), reflections, jitter, and signal attenuation due to transmission line effects hamper the integrity of the signals, making PCB design trickier and more complex. The PCB and chip power distribution network (PDN) must be designed carefully, as a badly designed PDN will affect the power integrity of the system.

## Effects of Signal Integrity

System designers must be careful when managing signal integrity, as well as when running system performance simulations. Enormous amounts of time and effort are spent debugging systems, as poor signal integrity causes poor reliability, degrades system performance, and, worst of all, system failures. However, shorter product life cycles and faster times to market are crucial, so spending huge amounts of time debugging a system due to signal integrity problems is no longer viable. Spending this extra time results in lost opportunities, expensive board re-spins, and extra man-hours. If signal integrity problems cause product failure in the field, then the incurred cost is the threat to the company's reputation.

Following on a continuous improvement path from the already robust and reliable Stratix II FPGAs, excellent signal and power integrity are some of the many rigorous design goals set for Stratix III devices. Detailed analysis has further enhanced the die and packaging to ensure that Stratix III FPGAs have best-in-class signal integrity, as well as a silicon-package PCB co-design strategy that enables easy system design. These chip enhancements and new features help customers' system-level designs to simplify PCB design and greatly reduce total system cost.

## Stratix III Signal Integrity Advantages

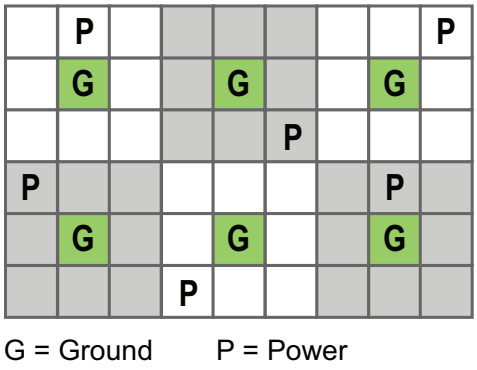
Signal integrity advantages of the new Stratix III FPGA include an 8:1:1 user I/O to ground/power ratio, optimized die- and package-level signal return path, adjustable slew rate control, staggered output delay control, dynamic OCT, on-package decoupling and on-die capacitance, and LVDS buffer enhancement.

### *8:1:1 User I/O to Ground/Power Ratio*

The new Stratix III FPGA comes with a user I/O to ground/power ratio of 8:1:1. This new package pinout pattern (shown in Figure 1) with a ground or power located adjacent to each of the I/Os provides a low impedance return path for the I/Os. Lowering the loop inductance reduces $V_{CC}$ sag and ground bounce. The new design reduces noise while

providing the optimum number of user I/Os. The 8:1:1 ratio is ideal, as beyond it are diminishing returns with a cost of a decreasing number of user I/Os.

*Figure 1. Stratix III Package Pinout*




### *Optimized Die- and Package-Level Signal Return Path*

Designed with several die- and package-level enhancements over Stratix II devices, Stratix III FPGAs further reduce signal return path inductance and lower crosstalk between I/Os. These enhancements include:

- Extensive distributed ground bumps at the die level with 8:2:1 user I/O to ground/power ratio
- All traces referenced to solid, continuous planes with more layers
- More ground reference vias within package
- Better distribution of power/ground balls
- More vias from package balls to planes
- Overall better return paths and better PDN design

### *Adjustable Slew Rate Control*

The edge rate of the signals can impact a system's performance. For example, a very fast edge rate can cause overshot and other signal integrity problems, while a very slow edge rate may reduce the timing margin. Finding the right balance between the two is the key to a good system design.

Stratix III FPGAs offer adjustable slew rate control to allow designers to adjust the edge rate of the signal for better signal integrity, while simultaneously achieving optimum performance for their system. Four different slew rate settings control the buffer rise and fall times, matching the desired I/O standard and controlling noise and overshoot. This flexibility provides the designer greater control over the design to achieve optimum system performance and excellent signal integrity.

### *Staggered Output Delay Control*

SSN is caused by a large number of I/Os switching at the same time. One way to reduce this number is by delaying some of the simultaneous switching output (SSO) edges, thus spacing out the output switching time, spreading out the SSN effect over time, and reducing its magnitude.

Stratix III FPGAs offer a new staggered output delay setting to control and delay some SSO, as well as allowing designers to control and lower SSN to obtain maximum performance. In addition, this feature also allows designers to adjust signal duty cycles and skew compensation due to board trace mismatch, thereby simplifying system and PCB design and reducing cost.

### *Dynamic OCT*

Impedance mismatch between the source output ($Z_S$), transmission line ($Z_O$), and load ($Z_L$) causes signal reflection and distortion such as overshoot, undershoot, and ringing and stair-step waveforms, producing erroneous signals.

Different termination schemes are used to overcome impedance mismatch, depending on the applications. Traditionally, external components, such as resistors, are used for the terminations, but a better alternative is to use the OCT resistors available on the device. This reduces the number of components on the PCB, thus saving precious board area and component cost. It also eliminates additional track stubs, which can cause signal integrity problems such as reflections of the signal.

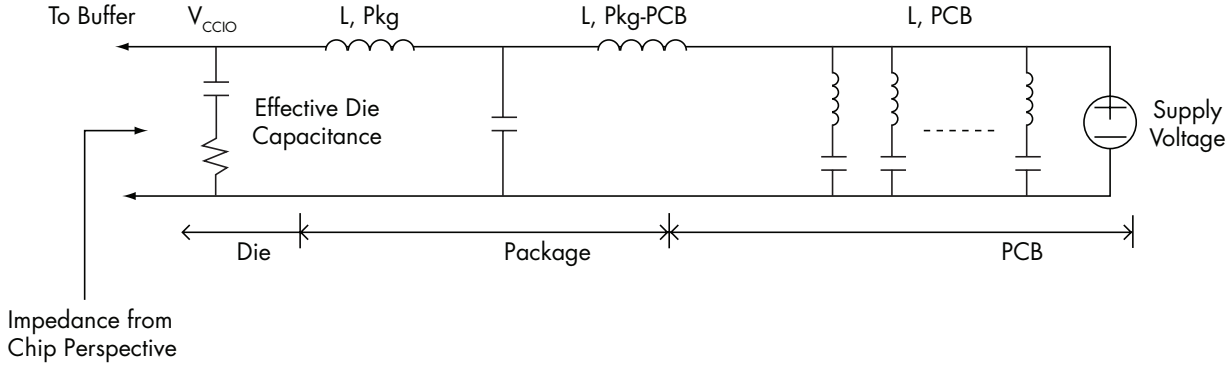
Stratix III FPGAs offer advanced dynamic OCT technology on all I/Os to eliminate the need for external termination resistors. This provides better system reliability and signal integrity performance with lower system cost and simpler PCB design. The new dynamic OCT feature for single-ended serial and parallel terminations enables termination schemes to be changed dynamically. This feature is extremely useful for implementing bidirectional interfaces, such as those in the DDR memories where OCT schemes can be changed dynamically depending where they are in the read or write cycle.

Aimed at reducing power consumption, dynamic OCT eliminates constant DC power on the bus by turning on the OCT resistors only when necessary. Stratix III FPGAs also provide differential OCT for high-speed interface. All Stratix III FPGA I/Os come with built-in enhanced digital autocalibration circuitry to provide precise impedance control and compensate impedance change due to temperature and voltage fluctuation, in order to produce accurate, repeatable, and predictable termination.

### *On-Package Decoupling and On-Die Capacitance*

In a typical FPGA system (see Figure 2), a PDN consists of three main parts: chip, package, and PCB, which includes the voltage regulator modules (VRM). Decoupling capacitors on the PCB, such as bulk capacitors and ceramic capacitors, maintain low PDN impedance in the frequency range of 100-300 kHz. On-board VRMs support lower frequencies and are effective up to 100 kHz. For higher frequency decoupling, Stratix III FPGAs now come with both on-package decoupling and on-die capacitance. These capacitors provide instantaneous charges from a nearby location to buffers, and replenish source-drain current rush upon gate transition.

*Figure 2. PDN Sections in a Typical FPGA System*




The on-package decoupling utilizes the land-grid array (LGA) capacitors with extremely low equivalent series inductance (ESL). These low inductance capacitors help to maintain low PDN impedance in a wider frequency range and to suppress power noise for cleaner power supplies. The on-die capacitance with high I/O driver capacitance value also helps to maintain cleaner power supplies, especially in the high-frequency band. The decoupling capacitors reduce the number of external PCB decoupling capacitors, thus saving precious board space, reducing cost, and greatly simplifying PCB design.

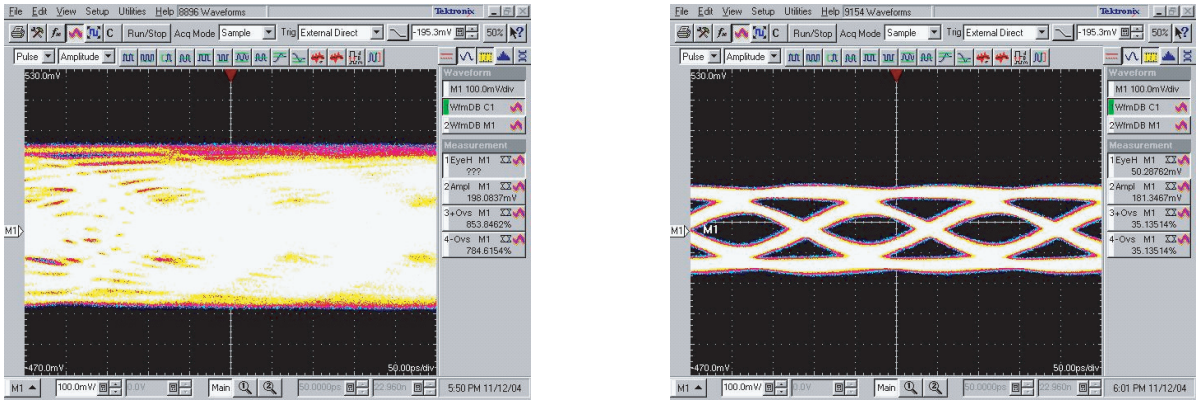
### *LVDS Buffer Enhancement*

At low frequency, a transmission line can be assumed to be ideal and lossless. But at high frequency, the transmission line is no longer ideal. As high-speed signals travel through board traces, transmission line effects (such as skin effect and dielectric absorption) cause signal attenuation. All Stratix III FPGA LVDS I/O buffers provide programmable

pre-emphasis and $V_{OD}$ features to address high-speed signal requirements for long and short trace lengths and to reduce signal attenuation so that the signals can be interpreted correctly at the receiver end.

The programmable pre-emphasis feature compensates for high-frequency attenuation by boosting high-frequency signal components and reducing pattern-dependant jitter. Four settings allow adjustment and compensation for various trace lengths, transmission line characteristics, and power to offer customers the flexibility to optimize the level of pre-emphasis for different scenarios (demonstrated in Figure 3).

*Figure 3. Examples of Signal Without Pre-Emphasis (left) and With Pre-Emphasis (right) Across 40 Inches of Backplane*



The programmable $V_{OD}$ settings enable designers to adjust output eye height to accommodate long-distance and high-performance links, which require an increased $V_{OD}$ drive for a larger eye opening and improved voltage margins at the receiving end, and short-distance and power-sensitive applications, which require a smaller $V_{OD}$ swing for optimized power consumption.

## Silicon-Package PCB Co-Design Strategy

As systems become more complex and encounter the various signal integrity problems mentioned earlier, PCB designs become more complicated and more costly. The Stratix III silicon-package PCB co-design strategy provides customer with a high performance and robust solution with excellent signal and power integrity, greatly simplifying PCB design and decoupling schemes to reduce system solution cost. The on-die and on-package capacitors provide effective decoupling to power supply noise and reduce the need for PCB decoupling capacitors. The new package design is aimed at reducing I/O crosstalk in the package-PCB breakout area and facilitating PCB decoupling implementation. Adjacent power and ground-ball pairing facilitates board designers to implement effective PCB decoupling using small-size low ESL decoupling capacitors.

## Altera's Commitment to Customers

Achieving excellent signal and power integrity and simplifying PCB design are two of Altera's many rigorous design goals for Stratix III FPGAs. Signal and power integrity have been a focus of Stratix III FPGAs from the very early stages of the design cycle, and every design detail has been taken into consideration. Detailed analysis and extensive device- and system-level characterizations and simulations have been carried out to enhance the die and packaging.

Altera offers a wide range of support to make designing with Stratix III FPGAs even easier. Solutions ranging from collateral-such as design guidelines, handbooks and characterization reports-to advanced design tools-such as the Quartus® II development software-help customers explore the benefits and advantages of Stratix III FPGAs and design with confidence.

## Conclusion

Altera's innovative silicon-package PCB co-design strategy was developed to help improve customers' system designs by increasing signal and power integrity. Die- and package-level signal return paths are optimized to reduce loop inductance, and new control features for slew rate and staggered output delay enable the designer to control the noise level of the device. The dynamic OCT technology and the advance on-die capacitance and on-package decoupling schemes for Stratix III FPGAs further improve signal and power integrity performance while simplifying PCB design and reducing cost. Additionally, the enhanced Stratix III LVDS buffers with programmable pre-emphasis and programmable $V_{OD}$ features compensate for signal attenuation on transmission lines.

Numerous enhancements to the silicon-package PCB co-design strategy ensure that Stratix III FPGAs offer excellent signal and power integrity. By using Stratix III FPGAs, customers reduce the risk of system failures, simplify the design process, and enhance design performance and flexibility to help their product achieve design goals easily with faster time-to-market. Altera is committed to providing customers with the best signal integrity solutions.

## Further Information

- Learn more about Stratix III FPGA signal integrity from the Signal Integrity Center: **www.altera.com/si.**
- Basic Principles of Signal Integrity: **www.altera.com/literature/wp/wp_sgnlntgry.pdf**
- AN 224: High-Speed Board Design Guidelines Using Stratix Devices: **www.altera.com/literature/an/an224.pdf**
- Hong Shi, et al, "Analysis of FPGA Simultaneous Switching Noise in Three Domains: Time, Frequency, and Spectrum," DesignCon 2006: **www.altera.com/literature/cp/cp-simswit.pdf**
- Larry Smith, et al, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," IEEE Transactions on Advanced Packaging, Vol. 22, No. 3, August 1999: **http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?tp=&arnumber=784476&isnumber=17029**
- Online Lecture 803: "Best Board Design Practices for Power Distribution Network," by Dr. Eric Bogatin of Bogatin Enterprises, LLC: **www.bethesignal.com**

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com