

Selecting the Ideal FPGA Vendor for Military Programs

Introduction

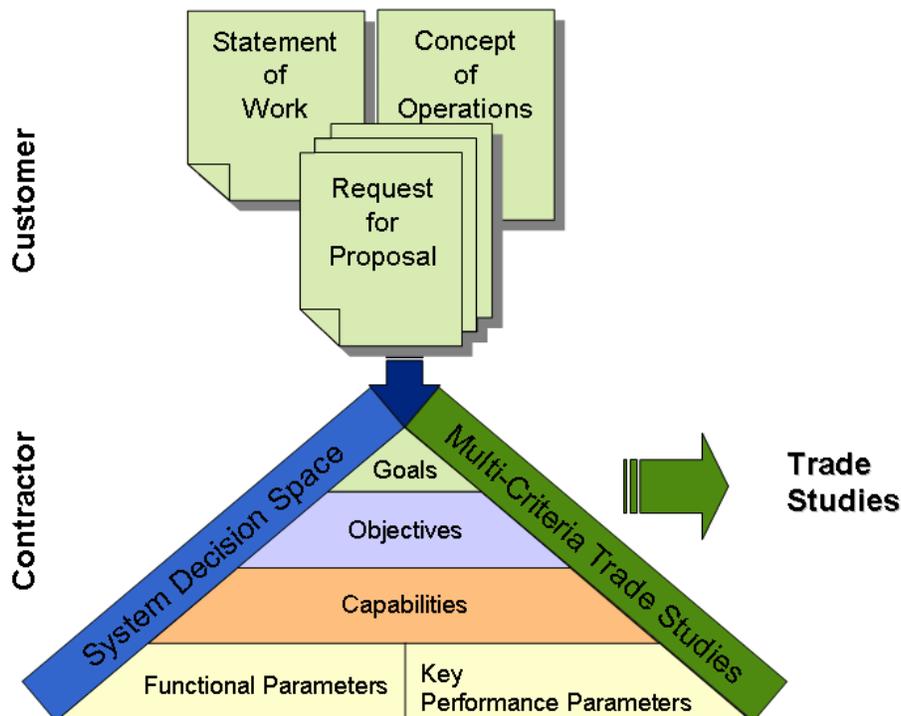
As digital processing technologies such as digital signal processors, FPGAs, and CPUs become more complex and powerful, product and feature differentiation among vendors has significantly increased. As a result, designers need to develop rigorous approaches to evaluate the technologies available from different military defense electronics vendors.

Evaluating Competing Criteria

Developing a system design for government projects typically requires a defense contractor to evaluate and make system decisions based on documents such as a request for proposal (RFP), statement of work (SOW), and concept of operations (CONOP) as shown in Figure 1. From these documents, a contractor must assess system alternatives while maximizing the customer’s expected system goals, objectives, and capabilities. As with any complex design, there may be competing goals and objectives, so a structured method of evaluating criteria, priorities, and alternatives is needed to support design decisions.

The analytical hierarchical process (AHP) is a commonly used multi-criteria decision analysis (MCDA) method that can be used to evaluate design alternatives. AHP is favored over other MCDA methods due to its structured mathematical approach and ease of use.

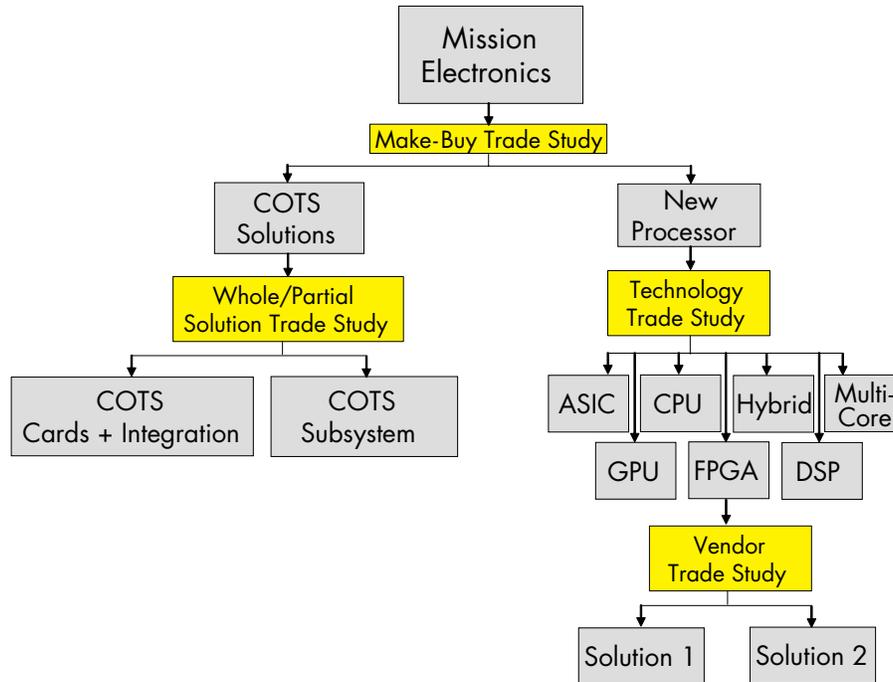
Figure 1. Systems Requirements Mapping



When evaluating customer goals and objectives for a military electronics design project using AHP, engineers face a number of architectural decision points to determine how the system will be developed. At each decision point, engineers orchestrate a trade study to evaluate their options and choose the best path for their system. Decision criteria can include everything from mission performance, cost, design risk, schedule, maintenance, and logistics, to a growing list of additional considerations such as maintainability, reliability, and manufacturability.

Each type of trade study has unique issues, options, and selection criteria, so engineers cannot approach them all the same way. For example, Figure 2 shows four decision points for a mission electronics design project, each of which must be approached differently.

Figure 2. Different Types of Trade Studies in Defense Electronics Programs



This white paper provides potential FPGA users a methodology for determining which programmable logic solutions best fit a project’s military or program requirements. It can also be used as a template for government, consultants, and advisors when questioning defense contractors about technology and the rationale behind their selection of programmable logic devices.

FPGA Trade Study Approach

A FPGA selection trade study can either focus on the specific capabilities of the technology or vendor, or on specific device candidates that may include multiple devices from a technology or vendor or even across vendors. In either case, one of the first steps is to define the selection criteria you will use, set the minimum requirements, and qualify or disqualify devices from consideration based on these requirements. Devices or vendors that do not meet these minimum requirements should be excluded from consideration.

Selection criteria that are likely to be considered for a military program include device availability, device utilization, power, productivity, quality and reliability, past performance, design reuse, packaging, performance, I/O bandwidth, security and anti-tamper requirements, and cost. While not all are applicable for every project, these criteria can be used to identify which FPGA vendors meet key project requirements. In addition, designers can work directly with the FPGA vendors to determine specialized criteria such as 15+-year device life-cycle support.

Device Availability

Military contractors need to be confident that production devices are available when needed for design to support critical proposal demonstrations to win contracts and follow-on production delivery. Considerations include how realistic the vendor’s schedule is, test chip results and progress, whether the vendor has a history of on-time device delivery or schedule slips, who their manufacturing (fabrication and packaging) partners are, and what their leadership standing in the market is to reduce risk for board mounting, integration, and testing.

Device Utilization

FPGA logic cell utilization efficiency can vary widely based on device geometry, as well as the type of design and distribution of design resources (e.g., memories, digital signal processors, etc.). Requirements can be based on previous program metrics, or on prototyping efforts, but usually engineers will have to generate their own data. This factor can also be evaluated in conjunction with others such as power or cost because high device utilization can lead to a lower power or less costly FPGA. Using 40-nm technology provides device utilization advantages with greater low-power advantages. The 40-nm process also brings larger densities for further integration. Not meeting expected device utilization increases development and part-count uses, delaying critical military applications to the warfighter.

Power

Most military applications are portable, thus are sensitive to power. These applications can range from battery-operated radios, enhanced night-vision goggles, to large arrays of FPGAs processing secure data and large bandwidth radar signals. Total power (static and dynamic) of an FPGA can be measured with a power estimator, or with in-progress power estimation methods using an FPGA prototype design. If the design has been prototyped in an FPGA, the design can be used to assess input parameters for power estimators from multiple vendors. Power consumption can be influenced by device utilization: because some devices use logic elements more efficiently, they can pack more logic into a smaller device that consumes less power. A low-power process also brings lower power, as seen in Altera® Cyclone® III FPGAs. In addition, process tweaks can provide low-power advantages as well as architecture changes, demonstrated by Altera's Programmable Power Technology in Stratix® IV FPGAs.

Productivity

Design productivity is probably the most difficult category to measure when selecting an FPGA. This refers to the company design practices, design tool maturity, and verification practices and capabilities that distinguish one FPGA supplier from another. When few independent assessments of design productivity exist, engineers need to rely on internal data or qualitative assessments of the design tools. Design productivity has a significant impact on the development cost of a military system. Using incremental compilation and a team-based design approach provides further productivity advantages. Development tools such as Altera's Quartus® II design software, which is deployed in the early phases of the architecture design, provide more efficient utilization and the ability to meet performance and power goals. Familiarity with typical military design flows also enhances productivity, with a combination of FPGA-based tools and standard third-party synthesis and simulation tools.

Quality and Reliability

Due to the harsh environments many military applications are exposed to, high quality and long-term reliable FPGAs will allow these applications to meet the expected operation under any environmental circumstances. Device quality can be based on either a quantitative and qualitative assessment of device capabilities for the application, or a compliance matrix with specific government-derived maintenance or replaceability goals. Device vendors collect and maintain data on all new and mature products. Providing industrial and military temperature support further enhances the long-term reliability of the FPGAs to the exposed environment.

Past Performance

Past performance is essential in government source selection, but should be applicable to FPGA vendor capabilities, as well. For programs where development costs and technical support are critical risk drivers, however, this category may be a logical requirement. Meeting schedules for each roadmap milestone and producing bug-free devices is critical.

Design Reuse

Design reuse, which may be a separate criteria or part of the development cost, refers to the reusable logic blocks available from FPGAs, algorithms, and IP that can be leveraged from previous designs. Reuse reduces risk and cost, and improves design assurance, so is an important and effective decision factor.

Packaging

FPGAs can effect size and weight, and varies by design, but can include issues such as limited board space, pin-count requirements, and heat-dissipation limitations. It can be a critical limiting factor that may restrict the designer to fewer vendors. Moving down to the next technology node allows smaller die, thus smaller packaging options. Reliable packaging also influences the quality of the signal integrity and the easy of board mounting to insure operational reliability in harsh environments.

Performance

Processing power is an important metric being assessed for advanced sensor applications, and can include on-chip/off-chip bandwidth, raw processing capability, or processing capability per watt of power. The importance of this factor varies, but it is often in the top half of consideration. Stratix IV FPGAs provide leading performance without penalizing the designer with too much power.

I/O Bandwidth

Advanced systems such as radar, electronic warfare, and ISR applications that require high on-chip/off-chip processing power will require common transceiver architectures and robust signal integrity. Continuous reuse of robust and proven common transceiver technology with performance enhancements for each new technology meeting speeds of up to 11.3 Gbps. Reducing risk by providing popular industry-standard protocols and low simultaneous switching noise and superior eye quality. Altera provides the industry's broadest portfolio of 40-nm FPGAs and ASICs with transceivers.

Security and Anti-Tamper Requirements

The built-in security support and anti-tamper capabilities of an FPGA are often a key factor for equipment that may be lost in the battlefield or earmarked for export. However, security dependencies are best considered separately from other criteria because national security concerns may outweigh cost concerns. Performing joint assessments with government agencies is important to provide the security level of the anti-tamper features of the FPGA.

Cost

Cost can be a central design criterion or a final decision-maker after other requirements have been met. In many low-volume applications, product cost may not be a significant decision factor. Development cost, qualification cost, hardware cost, and testing cost are also significant cost factors but can be offset by using proven FPGA technology such as Altera's Stratix, Arria®, and Cyclone series FPGAs.

Switching Costs

Switching costs are a significant consideration for some applications. In some cases, "switching" refers to moving a current design from another device such as a DSP processor to an FPGA, or from one FPGA vendor to another. In other cases, switching cost simply refers to the start-up cost when a design organization does not have the experience or tools in place to develop their application with a chosen FPGA vendor.

Switching costs are typically an independent variable assessed separately from a vendor trade study, and often requires vendor support for evaluation. But investing in easy-to-use tools and bug-free devices lowers the switching cost significantly. In addition, the productivity of tools can reduce engineering costs, thus justifying the switch. The payoff of a switch based on compelling criteria advantages, such as to Altera, will be realized in the long term, benefiting from lower development costs, reliable vendor, improved support, and robust roadmaps.

Developing Benchmarks and Measurements

The methodology used to measure selection criteria may vary widely. This section includes various measurements to help evaluate the qualitative aspects of the criteria. Examples include time until delivery for device availability, results with prototypes, research, or prior experience for device utilization, static power data from vendor early power estimators for device power, percentage of design that can be reused from previous work for design reuse, and the amount of throughput for processing bandwidth.

Because most defense engineers who routinely perform make/buy evaluations and select among component vendors as part of systems engineering activity have expertise in weighting criteria, a full description is not included here. However, this white paper describes an iterative weighting method now taught in graduate engineering programs as part of the AHP. Although this process has been the subject of countless articles, theses, and academic journals, utilizing the process at a basic level is very simple.

The AHP is based on pairwise criteria comparisons, making the evaluation of many dissimilar criteria easier to evaluate because only two criteria are evaluated at a time. First, build a pairwise comparison table to reflect the number of decision criteria, as shown in [Table 1](#), and assign the relative weights. The weighting scale used in this table ranges from 1 to 9, where 1 indicates that there is no preference between the two criteria (i.e., that they are equally important) and 9 indicates that one factor is critically important and strongly preferred over the other.

Table 1. Sample Pairwise Criteria

First Criterion	Second Criterion	Scale	Reason
Criterion 1	Criterion 2	1 to 9	Include explanation for comparison scale.
Criterion 1	Criterion 3	1 to 9	Include explanation for comparison scale.
Criterion 2	Criterion 3	1 to 9	Include explanation for comparison scale.

This process enables every factor to be examined in isolation with every other factor. [Table 2](#) summarizes a sample ranking of device selection criteria. The color of the ranking indicates which factor is preferred when weighed against the others, while the number indicates the strength of preference.

Table 2. Example of Pairwise Weightings Using AHP

Criteria	Device Utilization	Power	Cost	Productivity	Quality and Reliability	Past Performance	Design Reuse	Packaging	Performance
Device availability	8	4	9	2	6	2	2	4	4
Device utilization		4	2	8	4	6	6	4	4
Power			6	4	6	1	2	2	4
Cost				8	4	6	6	4	2
Productivity					6	2	1	4	6
Quality and reliability						6	6	2	1
Past performance							1	2	4
Design reuse								4	6
Packaging									1

Results

Once a designer determines whether cost and security will be part of the study or independent variables, and sets the relative importance of the selection variables, the results can be weighted using widely available spreadsheet algorithms or AHP-based software. The numeric inputs from [Table 2](#) were used to compute the weights shown in [Table 3](#), including a raw score for each vendor on a scale of 1 to 10. The weightings are determined by a pairwise comparison spreadsheet, which gives all of the numbers shown in the first column of [Table 3](#), using all of the numeric inputs from [Table 2](#). Spreadsheets that compute these numbers are publicly available.

Table 3. Trade Study Result With Weightings, Scores, and Final Recommendation

Criteria	Weight	Solution 1		Solution 2	
		Raw	Weighted	Raw	Weighted
Device availability	0.23	9	2.07	4	0.92
Device utilization	0.02	8	0.16	7	0.14
Power	0.10	9	0.90	6	0.60
Cost	0.02	6	0.12	9	0.18
Productivity	0.20	6	1.20	3	0.60
Quality and reliability	0.04	9	0.36	8	0.32
Past performance	0.12	8	0.96	5	0.60
Design reuse	0.13	5	0.65	9	1.17
Packaging	0.09	6	0.54	6	0.54
Performance	0.04	8	0.32	6	0.24
Total			7.28		5.31

A trade study includes this type of table as a final result, plus documents the rationale behind the pairwise ratings, the raw scores given to each vendor, and the metrics used. It also includes a sensitivity analysis that identifies which key decisions (criteria weightings or raw vendor scores) could result in reversing the recommendation. For example, the device availability in this example is so heavily weighted and shows such a large differential between vendor raw scores that a small change in device availability or customer schedule could result in a different trade study result.

Conclusion

The results of the trade study should give the program and engineering manager confidence when selecting a FPGA technology. More importantly, using trade studies disciplines engineering organizations to correlate government inputs with the technology choices made in system design. Documented vendor-source trade studies improve the quality of system documentation offered to government customers, and combine quantitative and decision data in a way that is accessible to customer and designer alike.

It is important for trade studies are performed to reduce risk in FPGA technology selection. The obvious winning technology will have attributes of driving the technology node to 40 nm and beyond, innovation in low-power technology while meeting performance requirements, robust embedded technology such as transceivers, DSP blocks, and security, and productivity tools to complement the technology leadership. These attributes determine a low-risk selection that results in the military contractor winning the proposal and delivering on the required capabilities of the proposal.

Further Information

Guidance

- *Architecture and Component Selection for SDR Applications:*
www.altera.com/literature/wp/wp-01026.pdf
- *Military Productivity Factors in Large FPGA Designs:*
www.altera.com/literature/wp/wp-01067-military-productivity-large-fpga.pdf
- *Military Benefits of the Managed Risk Process at 40 nm:*
www.altera.com/literature/wp/wp-01063-military-benefits-managed-risk-process-40nm.pdf
- *Stratix III FPGAs vs. Xilinx Virtex-5 Devices: Architecture and Performance Comparison:*
www.altera.com/literature/wp/wp-01007.pdf

Benchmarking

- Benchmarking Methodology:
www.altera.com/products/devices/performance/benchmark/per-benchmarkmeth.html
- *FPGA Performance Benchmarking Methodology:*
www.altera.com/literature/wp/wpfpgapbm.pdf
- *Guidance for Accurately Benchmarking FPGAs:*
www.altera.com/literature/wp/wp-01040.pdf

Comparison Tools

- PowerPlay Early Power Estimators (EPE) and Power Analyzer:
www.altera.com/support/devices/estimator/pow-powerplay.jsp
- Open Cores Organization IP Benchmarking Tools:
www.opencores.org

Analytical Hierarchical Process

- Wikipedia:
http://en.wikipedia.org/wiki/Analytic_Hierarchy_Process
- Saaty, T.L., *The Analytic Hierarchy Process*, McGraw-Hill International, New York, NY, USA, 1977.

Acknowledgements

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