Remote Radio Heads and the evolution towards 4G networks

Christian F. Lanzani[*], **Georgios Kardaras**[†], **Deepak Boppana**[‡]

Abstract

Distributed base stations with remote radio head (RRH) capability greatly help mobile operators to resolve cost, performance, and efficiency challenges when deploying new base stations on the road to fully developed 4G networks. Multi-mode radios capable of operating according to GSM, HSPA, LTE, and WiMAX standards and advanced software configurability are key features in the deployment of more flexible and energy-efficient radio networks. This white paper describes the key market and technology requirements for RRHs and how Radiocomps state-of-the-art WiMAX/LTE RRH and intellectual property (IP) core solutions, combined with latest FPGA technology from Altera, helps design compact, green, and full-featured applications for mobile network solutions.

Keywords: LTE, WiMAX, Remote Radio Head, OBSAI, CPRI, CFR, DPD, DSP, SRC, Radiocomp ApS, Altera, StratixIV GX, ArriaII GX, DTU, FPGA.

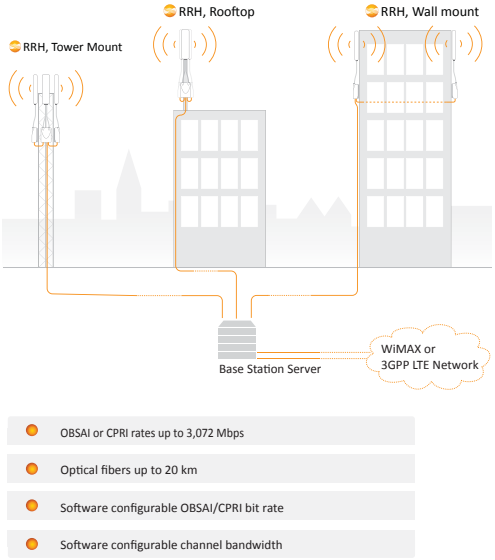

Figure 1: Distributed Wireless Base Station system.

INTRODUCTION

Wireless and mobile network operators face the continuing challenge of building networks that effectively manage high data-traffic growth rates. Mobility and an increased level of multimedia content for end users require end-to-end network adaptations that support both new services and the increased demand for broadband and flat-rate Internet access. In addition, network operators must consider the most cost-effective evolution of the networks towards 4G. Wireless and mobile technology standards are evolving towards higher bandwidth requirements for both peak rates and cell-throughput growth. The latest standards supporting this are HSPA+, WiMAX, and LTE.

The network upgrades required to deploy networks based on these standards must balance the limited availability of new spectrum, leverage existing spectrum, and ensure operation of all desired standards. This all must take place at the same time during the transition phase, which usually spans many years. Distributed open base station architecture concepts (Figure 1) have evolved in parallel with the evolution of the standards to provide a flexible, cheaper, and more scalable modular environment for managing the radio access evolution. For example, the Open Base Station Architecture Initiative (OBSAI) and the Common Public Radio Interface (CPRI) standards introduced standardized interfaces separating the Base Station server and the remote radio head (RRH) part of a base station by an optical fiber.

II - RRH SYSTEM REQUIREMENTS

The RRH concept constitutes a fundamental part of a state-of-the-art base station architecture. RRH-based system implementation is driven by the need to reduce both CAPEX and OPEX consistently, which allows a more optimized, energy-efficient, and greener base deployment. Figure 2 illustrates an architecture where a 2G/3G/4G base station is connected to RRHs over optical fibers. Either CPRI or OBSAI may be used to carry RF data to the RRH to cover a three-sector cell.

The RRH incorporates a large number of digital interfacing and processing functions as depicted in Figure 3. It also includes high-performance, efficient, and frequency-agile analog functions, all packaged into a

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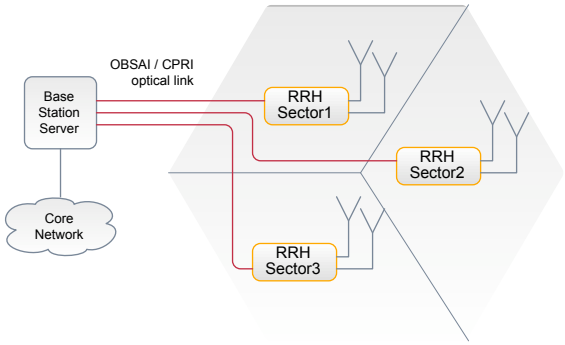

Figure 2: Three-Sector Wireless Call using RRH.

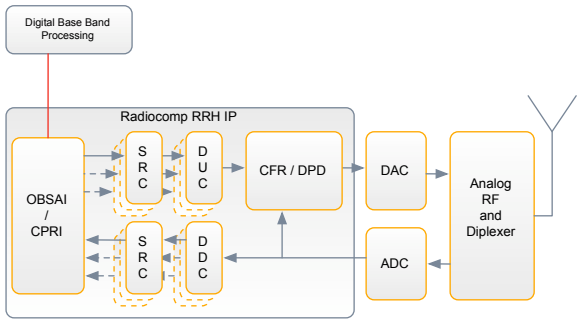

Figure 3: RRH System Architecture.

low-weight (9.7 Kg) device with a small mechanical footprint. The key advantages of using RRHs such as Radiocomps are listed in Table 1.

- **Smaller footprint.** Easier installation, reduced wind load, lower site rental costs, optimized coverage.
- **Flexibility in Software**. Remote upgrades and frequency-agile operations, easier capacity upgrades.
- **Higher performance.** High power efficiency, spectral emissions requirements, sensitivity, capacity
- **Multi-mode operations.**Combined and concurrent multi-standard operations reduce equipment needs.
- **Flexible multi-carrier capability.** Frequency agility, easier capacity upgrades

The most recent OFDMA-based standardsWiMAX and LTEinclude 20 MHz wideband radio channels for both Time Division Duplexing (TDD) and Frequency Division Duplexing (FDD) operational modes. The throughput is enhanced by multiple-in/multiple-out (MIMO) antenna techniques. Both 2x2 and 4x4 MIMO systems are attractive solutions meeting the small footprint requirements of the radio module. This is achieved by combining the energy-efficient radio module with advanced internal cable less geometry.

III - MULTI-RATE DSP APPLICATIONS FOR RRH

It is highly desirable to support multiple radio channel bandwidths per channel, e.g., WiMAX 5, 7, 8.75, 10, and 20 MHz in one radio platform, using only pure software reconfiguration. Moreover, it is highly desirable to support multiple channels concurrently in a multi-carrier system fashion. To achieve this, the designer must choose between using a different clock domain for each rate and using one single-clock domain with software flexibility. The single-clock domain technique is more elegant and takes advantage of advanced digital signal processing (DSP) techniques for converting each rate into a common system rate. Together these techniques are called sample rate conversion (SRC), and when combined with multi-channel digital upconversion (DUC) and digital downconversion (DDC),, they enable multiple sample rates to be processed concurrently in the same application and in the same clock domain of the digital-to-analog converter (DAC) or analog-to-digital converter (ADC). This method enables flexibility by supporting both single-clock and multiple-clock techniques simultaneously. As an example, the LTE and WiMAX standards define a selection for a number of channels with instantaneous bandwidths up to 20 MHz. In multi-mode radios supporting OFDMA/WCDMA modulation schemes, a flexible SRC greatly helps to make software-defined operations possible. Test results of Radiocomps SRC intellectual property (IP) shows that sampling noise added to a WiMAX signal with a sampling rate of 11.2 MHz to 122.88 MHz can be kept below 74 dB, thus providing higher system performance together with software flexibility.

IV - CFR CREST FACTOR REDUCTION

An OFDM signal has a large peak-to-average envelope power ratio, which results in significant distortion when passed through a non-linear device such as a power amplifier (PA). The objective of the crest factor reduction (CFR) technique is to reduce the peaks of the OFDM signal to a satisfactory level to ensure better usage of the PA. Due to the signal's reduced dynamic range, it is possible to operate at higher average power and hence closer to the PAs saturation point when combined with digital pre-distortion (DPD). A well-known effective CFR technique is the peak windowing approach, where power peaks exceeding a certain threshold are clipped and smoothed by filtering. The filtering mitigates unwanted out-of-band spectral products caused by the sharp signal edges of conventional clipping. Peak windowing approaches may offer several decibels of improvement, with 3 to 7 dBs of

improvement to the complementary cumulative distribution function (CCDF) demonstrated. Major factors to be considered are the window and filter selection, as well as the output power-clipping threshold. Note, however, that clipping inevitably will cause a distortion of the signal. Thus, it is necessary always to look for the trade-off between acceptable error vector magnitude (EVM) levels and extra dBs of linear improvement obtained via CFR. The EVM requirement for WiMAX is as low as 2.8%, while the requirement for LTE is 8% for 64QAM modulation. Peak windowing works in the time domain and uses less logical resource than spectral analysis. A spectral analysis uses the more costly fast Fourier transform (FFT) and inverse FFT (IFFT) functions to benefit from working directly in the spectrum. Peak windowing uses around one-tenth of the hardware signal processing resources compared to spectral analysis. CFR techniques often are combined with a DPD block to achieve high performance in the RF PA. The CFR block first cancels the peaks, thereby preventing the high peak signal from driving the PA into the non-linear operation region of the RF PA. In contrast, the DPD block extends the linear operation region (detailed analysis in next section) and the RF PA operates close to the saturation levels.

V - DPD DIGITAL PRE-DISTORTION

Trying to align a non-linear device such as a transmitter PA is a well-known challenge. With DPD, the PA operates in its highest efficiency region resulting in higher transmission power levels. Pre-distortion techniques have been developed for different domains of the transmission chain between baseband and the RF/analog domains, each of which has a number of advantages and restrictions. One of the most effective and commonly used approaches is DPD, mainly because of its flexibility, limited hardware design, and its software configurability. An effective DPD compensates for the nonlinearity of the transmitter PA, also taking into consideration any transistor memory effects and system temperature variations. The commonly used DPD techniques can be classified into feed-forward and feedback techniques. In the feed-forward techniques, a static look-up table (LUT) is calculated and stored in the FPGA memory. It is not updated at any point of the system's operation. This method is simple but lacks flexibility due to the absence of a feedback path. Once a feedback path is available, the LUT can be updated and adaptation algorithms can monitor and adjust the table entries.

Feedback techniques, as shown in Figure 4, are ideal for developing modules in a low footprint compared to RF pre-distortion techniques, which require hardware changes and additional RF components. Moreover, they are suitable for previously built systems because the feedback path RF-ADC-FPGA exists in most SDR implementations. Finally, another great advantage of these modules is their ability to adapt as well as to be configured and upgraded remotely. For feedback DPD, the typical choices are to a table, a polynomial approach, and a mixed approach. The DPD corrects the nonlinearity in the PA, which causes intermodulation distortion and leads to spectral re-growth. DPD also enables efficient use of the PA transistors since it extends the linear region, taking advantage of the normally prohibited higher power nonlinear region. A mixed approach using both polynomial and LUT methods is proposed. In implementation, the approximation that a polynomial can achieve is better suited to deal with wideband PAs due to memory effects. The effectiveness of the polynomial approach is limited by its order. Increasing the polynomial order also increases complexity and hardware usage. For fine resolution, LUT sizes grow, and the adaptation time slows. Typically, the LUT approach has been used in narrowband memory for less nonlinear solutions. However, the limited range of a LUT can be useful, especially for the higher output power regions that must achieve the highest levels of linearity. For certain parts of the nonlinear transfer function, it is possible that a polynomial of a rather high degree is needed. The benefits of both techniques are exploited by combining a LUT where the polynomial linearity reaches its correction limit due to lack of orders. The hardware resources of memory and multipliers therefore are kept as low as possible for a high degree of linearity. These techniques are used to correct both amplitude and phase of baseband input IQ samples. Radiocomps DPD solution makes efficient use of the feedback technique by taking advantage of both the polynomial and the LUT-based approaches, giving results as in Figure 5, and optimized for logical resources usage in conjunction with Radiocomps CFR IP.

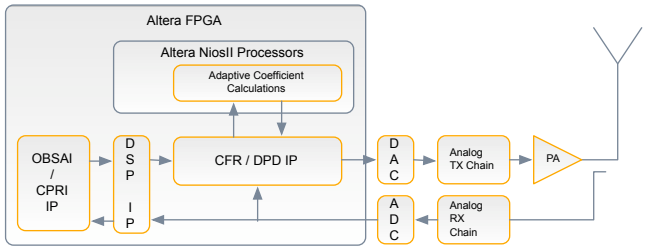

Figure 4: FPGA-Based Combined CFR/DPD Architecture.

VI - HIGH-SPEED ADC/DACs

High sampling rates are required when increasing the channel bandwidth to 20MHz. In addition, fifth-order harmonics are needed to process the DPD. These high sampling rates make safely routing high-speed digital lines between ADC and DAC and logic devices a chal-

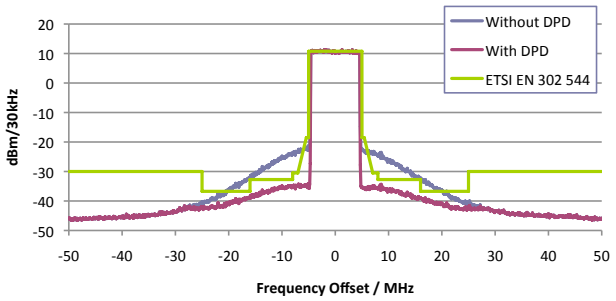

Figure 5: Radiocomp's DPD Measurement Results with a WiMAX 10MHz OFDMA Signal.

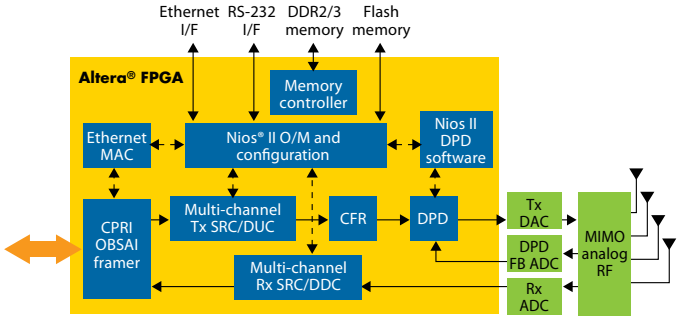

Figure 6: RF SoC Implementation With Alteras 40-nm Arria II GX and Stratix IV GX FPGAs.

lenge. Here a poor layout will result in digital switching noise feeding back into the conversion stage with a degradation of the overall system performance. The latest generation of ADC and DAC solutions, such as the JEDEC204 standard, defines a high-speed, single-pair link between the ADC and the FPGA or processor using bit encoding, synchronization, and alignment to achieve the high performance. Using such JEDEC-enabled devices to lower the amount of parallel digital lanes into a multi-channel radio card design, thus lowering and simplifying the PCB layout, and in turn increasing reliability and time to market.

VII - FPGA-BASED RF/RRH SOC IMPLEMENTATION

Alteras broad portfolio of 40nm transceiver FPGAs and ASICs, combined with easy-to-use software tools and IP, offers a variety of system-on-chip (SoC) implementation options for RRH applications. With channel bandwidth up to 20MHz, MIMO antenna configurations, and multi-mode support, implementation of the signal processing functionality in the RRH requires a highly integrated, flexible, and power-efficient silicon platform. Figure 6 illustrates how the entire digital functionality in a RRH can be integrated into a single Altera 40nm FPGA, resulting in a low-cost, low-power compact RRH solution. With more than 200K logic elements (LEs), 700 18x18 multipliers and 10Mbits of embedded memory, Arria II GX FPGAs offer a low-cost, low-power SoC option for RRHs requiring up to 3.75Gbps transceiver support. For example, a single-sector, a 2x2 MIMO configuration with functions such as CPRI/OBSAI, DUC/DDC, CFR, and DPD can be implemented in a single Arria II GX FPGA.

For systems that support 4x4 MIMO schemes or require greater than 3.75Gbps transceiver support, Alteras Stratix IV FPGA serves as a high-performance SoC implementation platform. With up to 530K LEs, greater than 1200 18x18 multipliers and 20Mbits of embedded RAM, Stratix IV FPGAs take performance to a new level. With transceivers up to 8.5Gbps, Stratix IV FPGAs offer a future-proof platform capable of supporting 6.144Gbps CPRI/OBSAI rates and higher.

RRH designs have very stringent size and weight requirements, and the lack of forced airflow places a challenging requirement in terms of power consumption. With unique low-power consumption features such as Programmable Power Technology and Selectable Core Voltage, Stratix IV GX FPGAs meet these allowable power-consumption levels. The high density of Stratix IV GX FPGAs also provides unprecedented levels of integration, enabling single-chip solutions for multiple antenna-based systems, with further cost, size, and power-consumption reduction via risk-free seamless migration to HardCopy IV GX ASICs. Altera also offers a variety of IP and reference designs for multiple standards including LTE, WiMAX, WCDMA, TD-SCDMA, etc. The combination of interface IP such as CPRI and OBSAI, along with optimized designs for DUC/DDC and CFR, help improve productivity and accelerate time to market. Alteras CFR for OFDM reference design is a high-performance solution capable of achieving a Peak to Average Power Ratio (PAPR) reduction up to 5dB, while meeting the EVM constraints for WiMAX/LTE. Alteras advanced blockset library, an enhancement to the DSP Builder software tool, has a unique synthesis technology that optimizes the high-level, unregistered netlist into a pipelined register transfer level (RTL), then optimizes it for a target device and desired clock rate. The benefits of the advanced blockset-based design methodology include:

- Automatic timing-driven FPGA implementation from Simulink
- Push-button flow to create multi-channel, multi-antenna DUC/DDC designs
- System-level constraint-driven design methodology to improve productivity
- Fast multi-channel design implementation
- Automates control plane for time-division multiplexed (TDM) data paths
- Efficiently pipelines multi-channel data paths

Alteras Nios II embedded processor can be used to implement the DPD adaptation algorithm instead of an external DSP block, thus reducing bill of materials (BOM) and board size. Time-critical software algorithms can be accelerated by adding custom instructions to the Nios II processor instruction set. The Nios II processor also can handle all initialization, configuration, status monitoring, operation, and maintenance functionality over Ethernet and RS-232 interfaces.

VIII - CONCLUSION

This white paper has described the architecture and benefits of a distributed wireless base station system. Advanced RRH internal architectures with DSP techniques also are illustrated. The architecture leverages the latest Radiocomp and Altera IP cores, coupled with the latest generation of Alteras 40nm FPGAs, and showed how this effective combination reduces the footprint and enhance the flexibility of RRH solutions and applications, thereby delivering best-in-class performances and efficiencies.

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ABOUT RADIOCOMP

Denmark-based Radiocomp is an industry-leading provider of remote radio heads and optical interfacing and advanced signal processing subsystems for LTE and WiMAX mobile networks. Learn more at www.radiocomp.com.

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