Overcome High-Speed I/O Verification Challenges with Stratix V On-Die Instrumentation

This document discusses verification and debug of high-speed I/O using the on-die instrumentation (ODI) features of the Altera 28-nm Stratix® V device. In line with Moore's law, I/O technology trends continue to double in speed and data rates every two to three years. As the speed and data rates of I/Os increase, new verification and test challenges emerge. This white paper describes the challenges of verifying high-speed links, and how Altera's 28-nm Stratix V ODI technology overcomes these challenges, and describes the ODI applications.

Introduction

As more transistors are integrated on a single chip, more functions and capabilities are possible in each chip. Transistors are also smaller and faster, enabling faster gate, faster switch speed, and smaller interconnect transport delays. As the logic, memory, and computing functions on a chip advance, I/O speed must also increase to improve overall chip efficiency.

Most I/Os with data rates higher than 1 Gbps adopt a serializer/deserializer (SERDES) architecture. I/Os with data rates of 5 Gbps and higher require equalization to compensate for frequency-dependent loss caused by the channel. This equalization is accomplished using a transmitter (TX)-based equalizer or a receiver (RX)-based equalizer, or both. I/Os with data rates of 10 Gbps and above need both TX and RX equalizations to compensate for loss caused by the channel in backplane applications. I/Os of higher data rates, such as 28 Gbps, need more advanced architectures and circuit blocks, which can be challenging to verify and test. The ODI technology in Altera's 28-nm Stratix V FPGAs can address many of the challenges faced by conventional external measurement equipment to achieve a cost-optimized, high-speed, high performance link channel design.

High-Speed Link Verification Challenges

The main challenges for high-speed link verification and test are as follows:

■ Accessibility—Certain characteristics, such as gain frequency responses for the continuous-time linear equalizer (CTLE), tap coefficients for the feed-forward equalizer (FFE), and decision-feedback equalizer (DFE), cannot be tested. This is because these circuit blocks reside in the device without access to conventional external instruments.

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■ Fault coverage—Data rates higher than 10 Gbps require linear equalizers such as the FFE and CTLE, and adaptive equalizers such as the DFE, to compensate the channel loss. This requirement is especially important for backplane or longer channel applications. In addition, data-edge referenced pulse-width deterministic jitter (DJ) and random jitter (RJ) are the new requirements for jitter testing. These conditions imply that a new test hardware or methodology is necessary for a high fault coverage that can comply with these new data rate and jitter parameter requirements.

■ Test interface impairments—At higher data rates, the test interface introduces signal distortions (that is, intersymbol interference (ISI)) due to frequency dependent loss that can penalize the margin and quality of the device under test (DUT). The impedance mismatch between the test instrument, test interface, and DUT can also introduce reflection. Both ISI and reflection can penalize the DUT margin quality and are not easily removable.

■ Accuracy—The accuracy requirements for testing high-speed I/Os are very strict. In the past, only expensive integrated circuit technologies, such as gallium arsenide (GaAs), indium phosphide (InP), and silicon germanium (SiGe), would be able to meet the requirements. However, recent advancements in nano-scale, CMOS-based LC oscillators are able to provide timing accuracy down to the sub picosecond levels, making CMOS-based design and manufacturing technology a good candidate for high-speed testing.

■ Cost—High-speed, high-performance, and high-accuracy instruments are expensive. On the other hand, the CMOS process is less expensive, making the CMOS process at nano-scale a good choice for enabling cost-effective standalone and embedded instruments.

Stratix V 28-Gbps ODI Technology

Altera's Stratix V FPGA ODI technology can overcome many of the challenges of high-speed I/O testing. High-speed I/O testing covers three major areas:

■ Signal quality testing for TX—includes eye diagram, jitter, and noise tests

■ RX testing—includes stressed eye, jitter tolerance, and sensitivity tests

■ Link-level testing—includes bit error rate (BER), link jitter, and noise margin tests

High-speed I/O testing can be managed using the generic ODI architecture or additional circuit blocks, such as the 28-nm/28-Gbps on-chip signal quality monitoring circuitry (EyeQ) or 28-nm/28-Gbps pattern and jitter generation. The Transceiver Toolkit in Altera's Quartus ®II software provides a complete GUI-based transceiver signal integrity utility.

Generic ODI Architecture

A transceiver TX that has the required capabilities can test the RX, and vice versa. With additional functionality, circuit blocks, and improved accuracy, an FPGA transceiver can become an integrated general-purpose, high-performance, high-speed I/O tester.

Figure 1 shows a generic ODI architecture that consists of two blocks. In the measurement block, signals from the DUT are split into three: one goes to the data sampler that provides the scope function, one to the error detector, and one to the clock recovery unit (CRU). The CRU provides the clock-timing signal, thus eliminating the external clock or trigger needed in conventional scope or bit-error rate test (BERT) instruments. The embedded memory stores the measured data and bit error samples and is accessible by the embedded CPU. The algorithms using memory and CPU hardware resources perform calibration.

In the generation block, the embedded clock generator provides pattern-generation timing. This block also contains phase and amplitude modulators that generate jitter and noise over the data pattern. The jitter and noise-modulated data pattern mimics a lossy channel and the associated ISI generation. Finally, an internal ODI loopback provides baseline calibration for external DUT path loopback calibration.

Figure 1. Generic FPGA-Based ODI
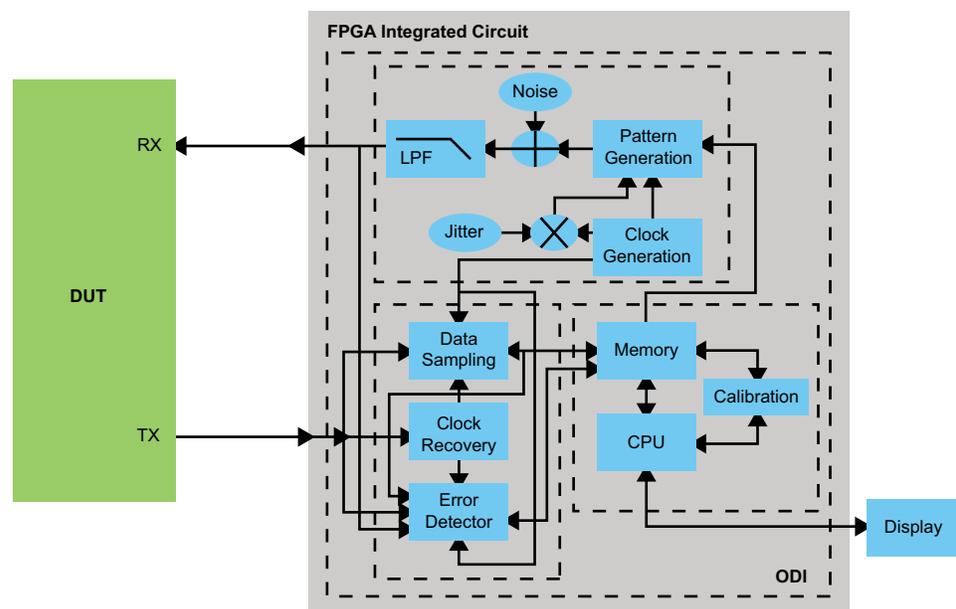
28-nm/28-Gbps EyeQ Feature

The measurement architecture implementation leverages the advantages of the existing transceiver circuit blocks. Some additional circuit blocks provide complete test functionality. Figure 2 shows the 28-nm/28-Gbps ODI measurement block diagram. This architecture provides both 2-dimentional (2D) scope and BER measurement capabilities up to 28 Gbps.

The measurement circuit block is in parallel with the nominal clock and data recovery circuit block. All blocks interact with each other to achieve the overall measurement objectives. The incoming signal is duplicated and fed into the measurement sampler B. Programmable reference voltage levels and sampling time are also fed into sampler B. A phase interpolator (PI) takes the recovered clock and delays its phase in a controllable manner to generate the measurement sampling time. A 2D eye diagram is measured by sweeping the reference timing and voltage levels of sampler B. Clock

and data recovery produces nominal data with an optimal clock timing and reference voltage (for example, a point at the center of the data eye). Directly comparing the data sample and measured sample provides error checking and in-rate or serial BER measurement as a function of sampling time and reference voltage. This is sometimes called a "vector-less" BER measurement, as it does not require prior data pattern knowledge. Hence, it is suitable for live-traffic BER measurement and monitoring.

Alternatively, the measured sample can also be fed to a multiplexer, then to the deserializer, and subsequently compared against the expected data bits in the FPGA core to provide parallel BER measurement. As such, this architecture can measure both bit error and symbol error simultaneously. Collecting enough measurement samples at various sampling times and voltage levels enables the generation of both eye and BER contours.

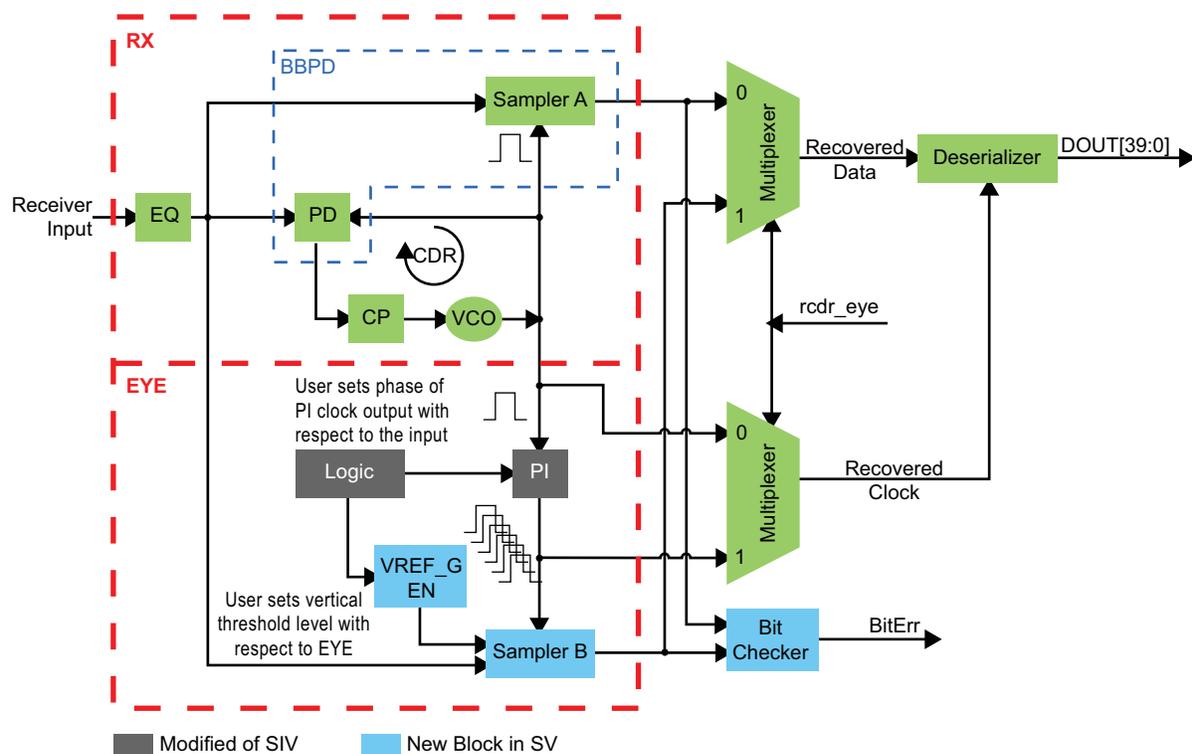**Figure 2. EyeQ Architecture with 2D Scope and BERT Capabilities**

Figure 3 shows details of the time and voltage resolutions of the EyeQ feature. This example has 64 differential threshold voltage levels and 32 sampling clock steps per unit interval (UI), providing 2,048 pixels for the 2D eye and BER contour measurement. Since this is a referenced-to-recovered clock measurement, its phase aligns to the data phase, leaving the PI as a key block to determine the timing accuracy. A digitally assisted calibration helps to achieve timing accuracy.

Figure 3. 2D Eye Measurement

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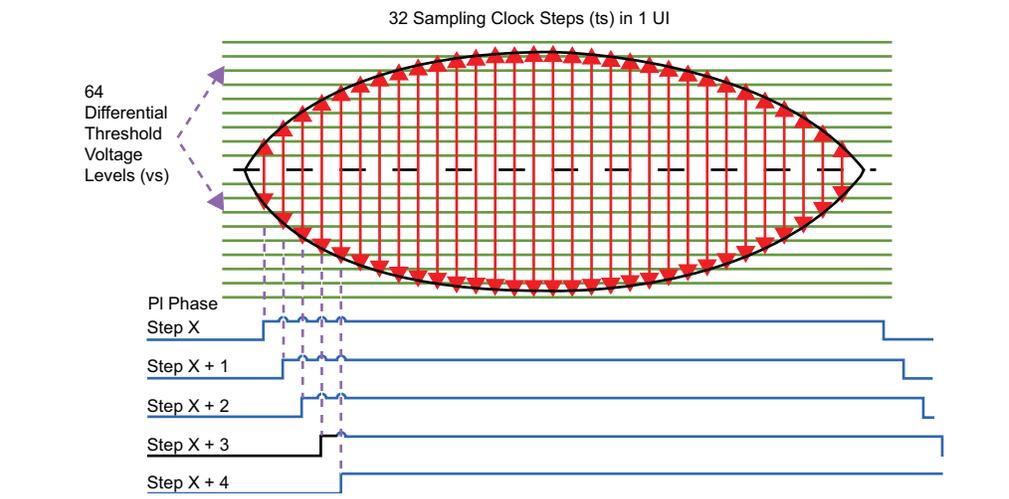
28-nm/28-Gbps Pattern and Jitter Generation

The pattern and jitter generation architecture also utilizes existing transceiver circuit blocks and preserves its accuracy. The intent of this implementation is to cover a wide range of jitter modulation frequencies for various applications. A dual frequency-band jitter generation architecture accommodates both low- and high-frequency jitter generation capabilities. Figure 4 shows the low-frequency generation architecture.

Figure 4. Low-Frequency Jitter Generation
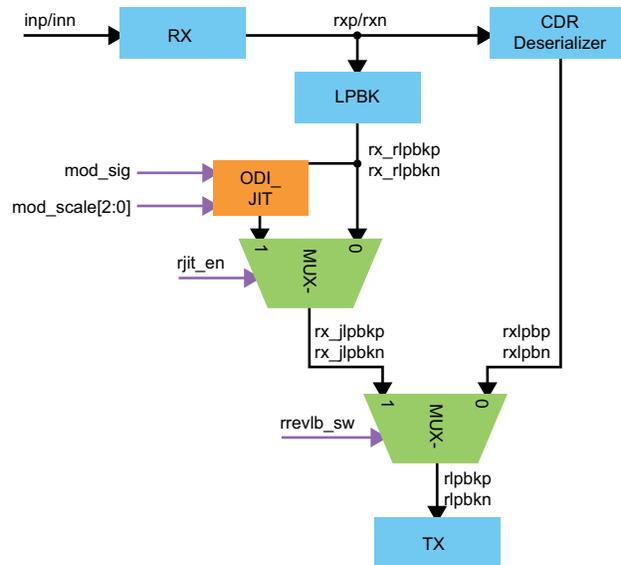
It is important to avoid adding any loading to the critical paths of the transceiver's TX and RX. A good place to introduce the modulator is in the loopback path. In this case, the data pattern can be the data received by the RX, which can either come from another TX of the FPGA transceiver, or from external signals sources such as an instrument pattern generator or another device in the link system. The low-frequency modulation uses a digital-delay chain to provide low-frequency and high-modulation magnitudes. As the modulator is digital-based, it is scalable and provides small silicon area and low power consumption advantages.

The low-frequency modulator is a four-port block. The data pattern or carrier signal comes from the receiver. Modulation is another input signal, along with the modulation-signal scaling control input. The modulation frequency is typically lower than 10 MHz, while the maximum modulation voltage swing is in the range of 100 – 200 mV. The maximum jitter modulation magnitude at 10 Gbps can be higher than 5 UI (for example, 500 ps). Figure 5 shows the high-frequency jitter and pattern generation architecture.

Figure 5. High-Frequency Jitter Generation
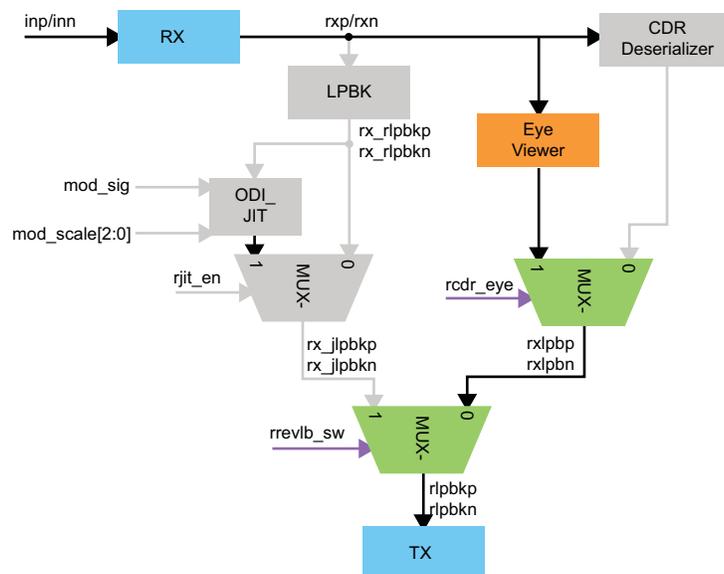
In this architecture, the PI and sampler generate the modulated signals. The PI is known to provide high-frequency modulation with an amplitude of up to 1 UI. In this architecture, the measurement circuit control logic provides the required modulation jitter source. The PI is also a digital circuit, providing both area and power consumption advantages just like in the low-frequency jitter and pattern generation architecture.

The high-frequency jitter and pattern generation architecture can have a maximum modulation frequency up to 10 MHz, with a maximum modulation jitter amplitude up to 1 UI. A PI step control internally generates the modulation signal.

Software for ODI

The ODI feature within the Transceiver Toolkit is part of the Quartus II software. The ODI feature allows users to quickly test, validate, debug, and improve the functionality and performance of the given design and implementation. The Transceiver Toolkit can help to identify, resolve, or alleviate issues related to signal integrity, jitter, and noise. The same applies to eye-diagram and BER issues related to the transceiver link.

Timing and voltage margin and sensitivity can be determined during the bring-up and mission modes, enabling adaptive and high-performance link operations.

Stratix V FPGA ODI Applications

Altera's Stratix V embedded ODI has a wide range of applications. Although any applications using Stratix V FPGAs can utilize ODI for high-speed test and measurement purposes, ODI plays an important role in high-speed I/O link validation and diagnostics, live-link data quality monitoring, and test and measurement OEMs.

High-Speed I/O Link Validation and Diagnostics

It is common for a high-speed link initially to perform below the expected level. The Stratix V ODI can help identify the problems from the TX, RX, and their combinations with the link channel. Figure 6 provides an example with two links. The Stratix V ODI is on one side, and the TX and RX ports are on the other side.

Figure 6. Stratix V ODI Application in Link Validation and Debug
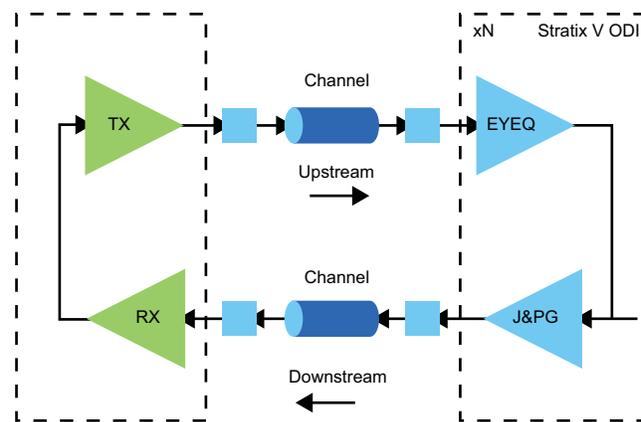
For the upstream link, the EyeQ feature conducts validation, tests, and jitter- and noise-margin determination for the TX channel. For the downstream link, jitter and pattern generation performs validation, stress and tolerance tests, and jitter- and noise- margin and sensitivity determination for the RX channel. If a loopback path exists between the TX and RX of the other end, then the EyeQ and jitter and pattern generation capabilities of the Stratix V FPGA side can test both the TX and RX under nominal and stressed conditions. In addition, the embedded ODI does not require a probe, thus eliminating additional signal distortions introduced by invasive probes. The ODI architecture scales to channels to enable the parallel test, validation, and debug of the multiple-lane link to provide better test throughput and efficiency.

Live-Link Data Quality Monitoring

Live-link data quality varies depending on environmental factors such as temperature, humidity, and pressure. Network system operators prefer non-invasive and low-cost methods to monitor the link data quality and take appropriate actions to prevent the loss of data. The vector-less BER measurement capability of the Stratix V FPGA's ODI is suitable for live-link data quality monitoring, as it does not require any prior knowledge of the data traffic and clock and pattern trigger signals. This method also meets the non-invasive and low-cost requirements of such data quality monitoring.

Test and Measurement OEMs

FPGAs are widely used as an important component in laboratory test and measurement instruments, as well as automated test equipment (ATE) for high-volume manufacture (HVM) and system-on-a-chip (SoC) characterization tests. With high-speed test capabilities of EyeQ and J&PG, Stratix V FPGAs have a wider role in high-speed I/O, analog, mixed-signal, memory, and digital test and measurement OEMs.

Conclusion

The verification and test challenges for high-speed I/Os include accessibility, fault coverage, test interface impairments, accuracy, throughput, and cost. The Stratix V ODI technology provides a solution to many of these challenges, especially for data rates of 10 Gbps, to as high as 28 Gbps.

The applications for the 28-nm/28 Gbps Stratix V FPGA ODI include high-speed link system validation, test, and debug; live network traffic data quality monitoring, and test and measurement OEMs. The Stratix V FPGA ODI is ideal for high-speed I/O link tests due to its high fault coverage, throughput, and parallelism and low-cost advantages.

Further Information

- Information on 28nm Stratix V FPGAs and transceivers:
  http://www.altera.com/stratix-v/stxv-index.jsp

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Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
February 2011	1.0	Initial release.