

PCI Express® (PCIe®) Gen2 performance is no longer a “high-end” (read expensive) standard to support. With the certification of the Altera® Cyclone® V FPGA family, PCIe Gen2x4, design engineers now have a low cost alternative for their PCIe Gen2 applications.

## Introduction

PCIe technology operates in all segments of the electronics industry from industrial and medical to consumer and server applications, as a motherboard-level interconnect (to link motherboard-mounted peripherals), a passive backplane interconnect, and as an expansion card interface for add-in boards.

Since its introduction by the PCI Special Interest Group (PCI-SIG) in 2003, the PCIe specification has continued to evolve to higher data rates and broader widths. Once the domain of high-end processors and soft intellectual property (IP) cores in FPGAs, the specification has evolved to the inclusion of hard IP cores within the FPGAs. Historically, support for these advanced speeds and throughput has been the domain of the high-performance and midrange FPGAs. Altera first offered a hard PCIe IP block in Stratix® IV FPGAs (2008), but now supports PCIe Gen2x4 IP in even the low-cost Cyclone V FPGAs, enabling smaller package implementations and fewer power rails, and lowering total power consumption while taking advantage of the performance gain.

## Reducing Implementation Cost of PCIe Gen2

To achieve a PCIe-Gen2-x-4-lanes-(20 Gbps) level of performance, engineers were forced to use high-performance or midrange FPGAs such as Stratix or Arria® devices. Only these devices provided the transceiver speeds needed to support the PCIe Gen2 standard, but this level of performance comes with significant costs, both direct and indirect. By integrating PCIe Gen2 support into a low-cost platform, such as Cyclone V FPGAs, Altera significantly reduces the total cost of ownership for PCIe Gen2 to the design engineer.

Direct costs typically refer to the silicon and packaging costs. Cyclone V FPGAs enjoy the reduced cost benefits of TSMC’s 28 nm LP (28LP) process. By utilizing wirebond package technology, these FPGAs realize additional cost savings. In total, low-cost Cyclone V FPGAs can reduce direct costs by up to an order of magnitude compared to midrange and high-end FPGAs.

Indirect costs are the less obvious costs associated with implementing a particular design, such as the number of voltage rails, number of printed circuit board (PCB) layers, PCB space, cooling requirements, and length of design time. As shown in [Table 1](#), Cyclone V FPGAs are developed with these hidden costs in mind, so they use as few as two power rails, come in small packages (11 x11 mm), low pin counts (to reduce PCB layers), and consume limited power to reduce cooling requirements. Additionally, Altera's integrated PCIe hard IP blocks and Avalon® memory-mapped (Avalon-MM) architecture reduce design time, accelerating time to market with higher levels of abstraction and proven IP blocks.

**Table 1. Advantages of Cyclone V PCIe Gen2 IP**

	Cyclone V GT FPGA	40 nm FPGA	Improvement
Product Class	Low cost	Midrange	Lowest system and power
List Price	x	10x	Less than 10% of the price
Packaging	11 mm sq	29 mm sq	Size reduction (85% less area)
Voltage Rails	2	5	Power and layout simplification

## PCIe Hard IP Reduces Development Time

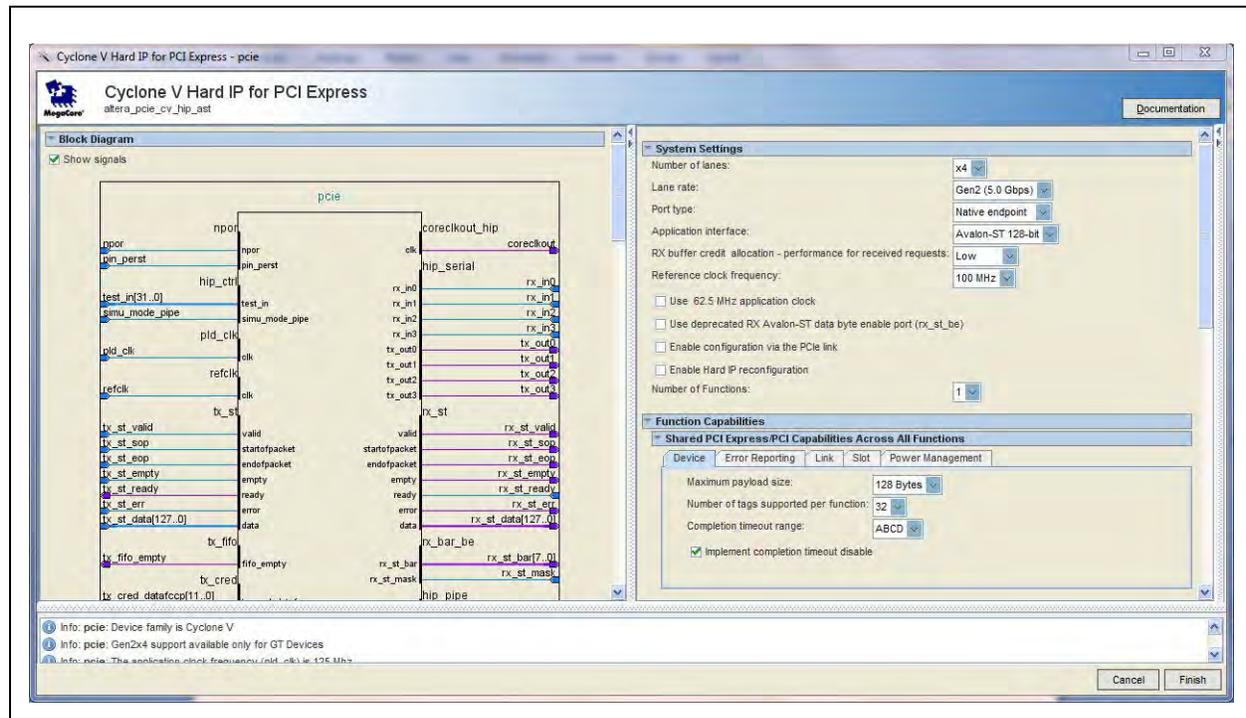
The PCIe hard IP in Cyclone V FPGAs supports both rootport and endpoint with multifunction support configurations for Gen 1.x from 25K LEs and Gen2.1 from 77K LEs, in compliance with the PCIe Base Specification 2.1. Using a configurable hard IP block, rather than array logic, reduces the gate count and enables faster timing closure. [Table 2](#) lists the configurations allowed for each Cyclone V device's hard IP blocks on the top and bottom transceiver banks.

**Table 2. PCIe Bandwidth**

PCI Specification	Line Rate	Encoding Scheme	Maximum Theoretical Bandwidth
Gen1.x	2.5 Gbps	8B/10B = 20%	2.0 Gbps
Gen2.1	5.0 Gbps	8B/10B = 20%	4.0 Gbps

The PCIe hard IP core itself is configured using the Altera MegaWizard™ GUI, shown in [Figure 1](#), which allows users to customize the lane rates and widths, along with other PCIe specific characteristics such as payload size and credit buffer allocations. One unique option is the application-side interface. Altera provides two options for how the user's application accesses the hard PCIe protocol stack: Avalon Streaming (Avalon-ST) or Avalon-MM. The Avalon-ST interface provides access to the full bandwidth available on the PCIe link—however, the user's application logic behind the hard IP must perform the tasks of encoding and decoding all of the transaction layer packets (TLPs).

Figure 1. PCIe Hard IP Core MegaWizard GUI



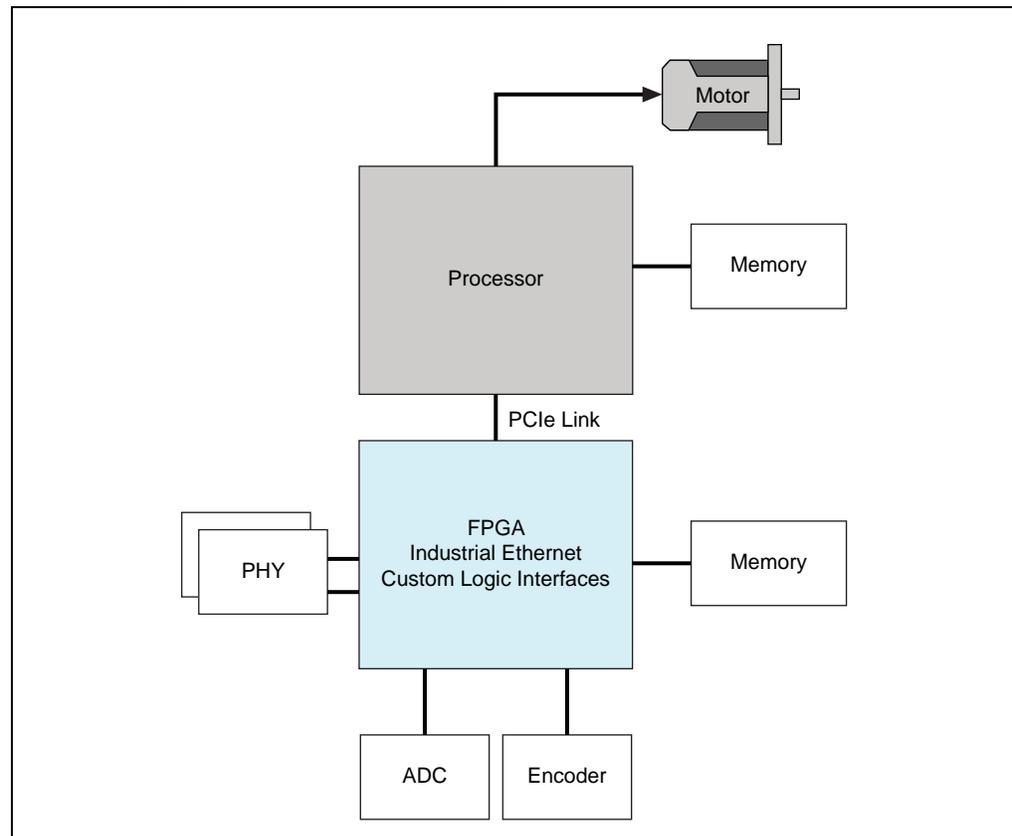
Implementing a design of this sort requires a reasonable understanding of the PCIe protocol—and even then, it can be quite time consuming to build and test. Alternatively, users can take advantage of the Avalon-MM interface, which provides a standard interface with simple data, address, and control signals. All TLP encoding and decoding is performed by this interface, so the user logic behind the hard IP is vastly simplified. Expert users who require every bit of bandwidth possible have the Avalon-ST option, whereas users who can afford a small sacrifice in bandwidth can save significant engineering resources by using the Avalon-MM interface.

In 2010, Intel launched their next-generation Atom (Tunnel Creek) device, a single-chip CPU that targets industrial control, military, medical, and automotive applications. The processor embeds a limited set of peripherals such as a memory controller and UARTs. Additional interfaces are added to the I/O hub behind the PCIe link. These peripherals and interfaces makes the whole family extremely flexible and scalable, and very attractive to the embedded market. Other industry-standard processors, with embedded ARM®, MIPS and PowerPC cores, have adopted PCIe as well.

Custom I/O hubs can be built with Cyclone V FPGAs, and the multifunction support enables designers to use standard OS software drivers to share PCIe link bandwidth among the peripherals in the FPGA. Without multifunction support, the customization of software drivers to achieve this sharing is a major development effort.

Designers can reduce system cost by integrating several single-function endpoints into one multifunction endpoint. In cases where customers are asking for multiple PCIe endpoints in a single FPGA, multifunction support can potentially reduce their costs by eliminating the need for multiple soft or hard PCIe cores and integrating them into a single multifunction PCIe endpoint. Such integration could lead to Industrial Ethernet interfaces being included on the FPGA, as shown in [Figure 2](#), thereby giving drive and I/O card suppliers the flexibility to offer a single hardware platform configured to support multiple interfaces.

**Figure 2. Example Industrial PLC Controller Application**

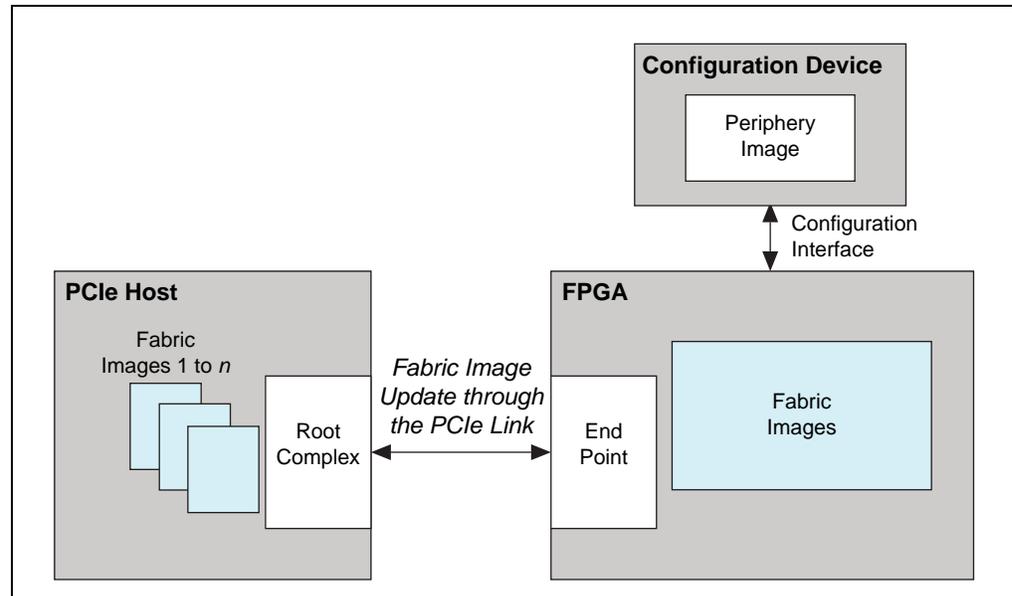


## New PCIe Features in Cyclone V

The Cyclone V hard IP has been architected in such a way that it can be configured and operational prior to the fabric of the FPGA being configured. This autonomous hard IP has two big benefits to users. First, the FPGA configuration scheme no longer has to configure the entirety of the FPGA within 100 ms. (The PCIe specification requires devices to begin PCIe bus enumeration within 100 ms of power being supplied.) Second, the configuration data for the fabric portion of the FPGA can be sent across the PCIe bus, further reducing the costs of the configuration solution and providing the ability to change the entire FPGA fabric functionality without having to bring down the PCIe link.

While the autonomous hard IP, along with the FPGA periphery, must be configured with some sort of on-board non-volatile memory, it can be very small as the configuration file sizes for the hard IP/periphery are also quite small (KBs). After the hard IP and periphery are configured, the PCIe core immediately begins to train with the root port and reach L0. Users can elect to continue configuring the rest of the FPGA from serial flash on the PCB (without being concerned about the 100 ms power-up time) or they can send the fabric configuration bits across the PCIe bus. Further, it is possible to build multiple fabric images (Figure 3) that share the same hard IP and periphery, allowing users to choose between the different fabric designs. Configuring the FPGA across the PCIe bus is called Configuration via Protocol (CvP) using PCIe.

**Figure 3. CvP Image Update**



For CvP, there are three supported modes of operation. In each case, the data rate in CvP is the same as the data rate in the PCIe application.

- *CvP off*—The FPGA is configured via traditional configuration method, and the PCIe link is only used for PCIe applications.
  - 👉 Even with CvP off, users can still elect to enable the autonomous hard IP, which results in the hard IP/periphery being configured first and the link training commencing immediately thereafter, while the rest of the fabric of the FPGA is still configured via the traditional configuration method.
- *CvP initialization and update mode*—The PCIe link is utilized for the initial fabric configuration, fabric image, and also the PCIe application.
- *CvP update-only mode*—The PCIe link is used for fabric update and for the PCIe application.

This method of configuration has the advantages of lower cost by use of small configuration PROM and reduction in the number of dedicated FPGA configuration pins. But it is important to remember that CvP cannot be implemented when the hard IP is configured as a rootport, it must be an endpoint. In addition, designers must use the hard IP core located at the bottom side of the die, the GXB\_L0 bank, as it has the connections to the internal configuration logic.

## Conclusion

As the low-cost family member of Altera's 28 nm product portfolio, the adoption of PCIe Gen2 hard IP in Cyclone V FPGAs enables an increase of data throughput while maintaining the lowest system cost and power, thereby enabling design engineers to implement high-performance PCIe Gen2 designs at a greatly reduced system cost.

## Further Information

- *Cyclone V Device Handbook:*  
[www.altera.com/literature/hb/cyclone-v/cyclone5\\_handbook.pdf](http://www.altera.com/literature/hb/cyclone-v/cyclone5_handbook.pdf)
- *User Guide: Cyclone V Hard IP for PCI Express:*  
[www.altera.com/literature/ug/ug\\_c5\\_pcie.pdf](http://www.altera.com/literature/ug/ug_c5_pcie.pdf)
- *User Guide: Configuration via Protocol (CvP) Implementation in Altera FPGAs:*  
[www.altera.com/literature/ug/ug\\_cvp.pdf](http://www.altera.com/literature/ug/ug_cvp.pdf)
- PCI Express Base Specification 2.1:  
[www.pcisig.com/home](http://www.pcisig.com/home)
- Cyclone V GT FPGA Development Kit:  
[www.altera.com/products/devkits/altera/kit-cyclone-v-gt.html](http://www.altera.com/products/devkits/altera/kit-cyclone-v-gt.html)

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- Jeff Wimmatt, Product Marketing Engineer, Low-Cost and Midrange FPGAs, Altera Corporation

## Document Revision History

Table 3 shows the revision history for this document.

**Table 3. Document Revision History**

Date	Version	Changes
April 2013	1.1	Added item to "Further Information".
March 2013	1.0	Initial release.