White Paper

Lower Costs in Broadcasting Applications With Integration Using FPGAs

Introduction

In broadcasting production and delivery systems, digital video data is transported using one of two serial interface formats: video serial digital interface (SDI) for uncompressed data, and asynchronous serial interface (ASI) for compressed data. In the video production environment, video and audio data are primarily transported using SDI as defined by the Society of Motion Picture and Television Engineers (SMPTE).

Video production equipment may support standard-definition (SD) digital video formats, high-definition (HD) digital video formats, or both. SD video is transmitted at SDI rates of 270, 360, or 540 Mbps while HD video is transmitted at the SDI rate of 1.485 Gbps or 1.485/1.001 Gbps. With its superior visual quality, HD video represents the future of digital video broadcasting. As a result of the growing demand for HD video, there is an increasing need for hardware that can handle the larger data throughput required by HD technology.

Within the digital video delivery environment, data is primarily transported as a single-program transport stream (SPTS) or a multi-program transport stream (MPTS) at 270 Mbps using ASI, which is defined by the Digital Video Broadcasting (DVB) Consortium.

While broadcast equipment developers have traditionally used ASSPs for implementing SDI and DVB-ASI functions, these interfaces can also be implemented in programmable logic devices (PLDs), using the logic and other embedded resources available in PLDs to build the required individual digital functions. By using programmable logic instead of ASSPs, broadcast equipment developers can significantly reduce overall costs. In some cases, the programmable logic equivalent can be less than one-tenth of the ASSP cost on a per-ASI channel or per-SDI port basis.

Programmable Logic-Based Solutions for SDI

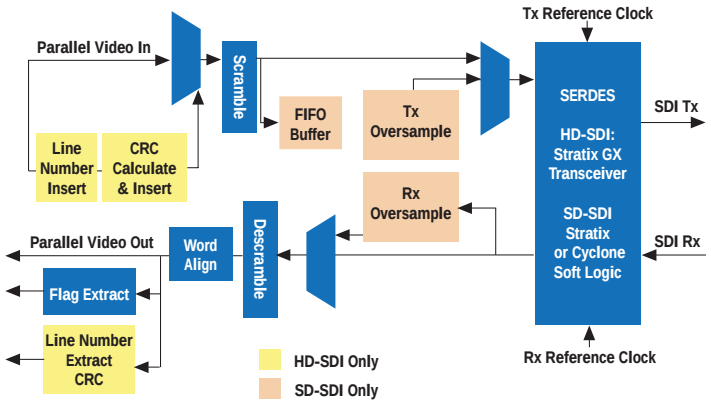
To achieve the 270-Mbps data rate required by SDI and DVB-ASI, a programmable solution needs to offer:

- LVDS I/Os
- Sufficient logic capacity
- Data recovery capability
- PLLs to generate CLK

The Altera® Cyclone™ series and Stratix® series FPGAs provide these features. For HD-SDI data rates, PLDs with embedded SERDES technology, clock-data recovery, and integrated high-speed transceiver channels such as Altera's Stratix GX series FPGAs are required.

Figure 1 shows the elements required to implement SD-SDI and HD-SDI functions in Altera programmable logic. The SD-SDI solution shows an oversampling scheme implemented in logic elements (LEs) to recover data. LEs, the basic building blocks of Altera FPGAs, are indicated as “soft logic” in the SERDES block. In the HD-SDI solution, the embedded SERDES and CDR circuitry perform the clock and data recovery functions.

Figure 1. PLD-Based SDI Solution Elements

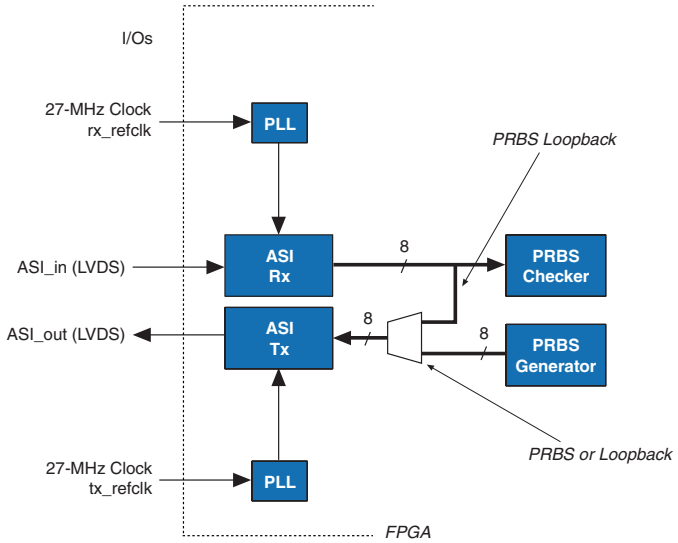


Additional functions in the HD-SDI solution include line-number insertion and cyclic redundancy check (CRC) calculation on the transmitter side, and line number extraction and cyclic redundancy checking on the receiver side. The line number insertion and extraction blocks refer to the data included in each SDI video line to indicate the current line number as defined by SMPTE292M section 5.4. The CRC blocks support SMPTE292M section 5.5, which defines a code included in the chroma and luma channels for each HD-SDI video line.

Programmable Logic-Based Solutions for DVB-ASI

The data rates required for DVB-ASI can be accomplished using FPGAs that offer LVDS I/Os for the ASI receiver and transmitter, as well as PLLs for the input receiver and transmitter reference clocks. Altera's Cyclone, Stratix, and Stratix GX series FPGAs include these features. Figure 2 shows the elements required to implement DVB-ASI in an FPGA, including a loopback path where the transmitter is coupled with the receiver and a pseudo-random binary sequence (PRBS) checker and PRBS generator for built-in test operations.

Figure 2. DVB-ASI Implementation in Programmable Logic—Block Diagram



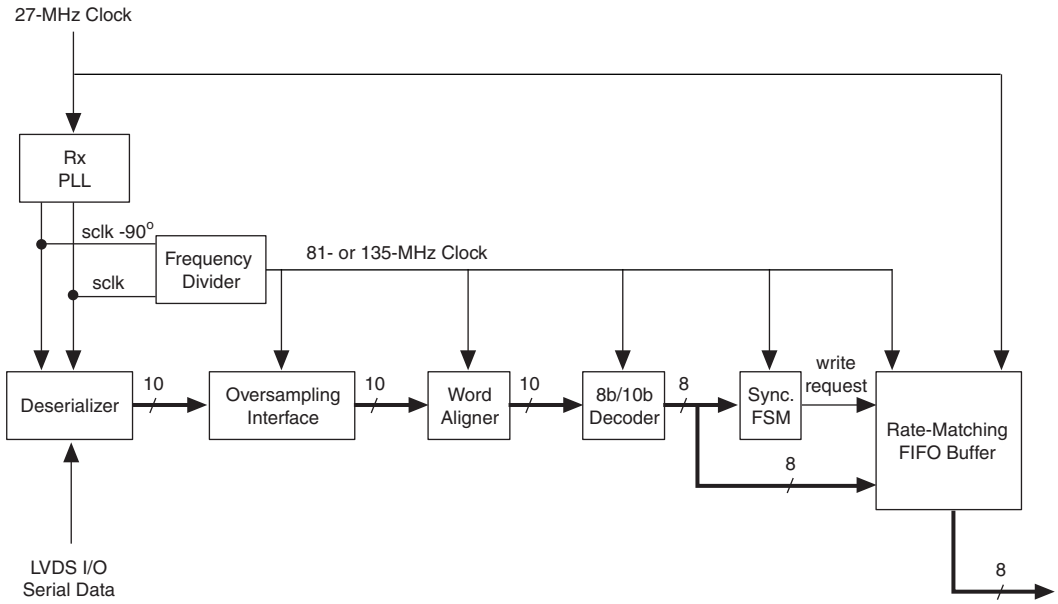
The ASI receiver consists of:

- Deserializer that converts the incoming serial data into 10-bit wide parallel data
- Oversampling interface for data recovery and bit-synchronization
- Word aligner

- 8b/10b encoder to convert the 10-bit parallel data into 8-bit wide raw data
- Synchronization state machine to detect word synchronization or synchronization loss
- Rate-matching FIFO buffer that rate matches between the incoming bitrate and the transmit or system clock rate

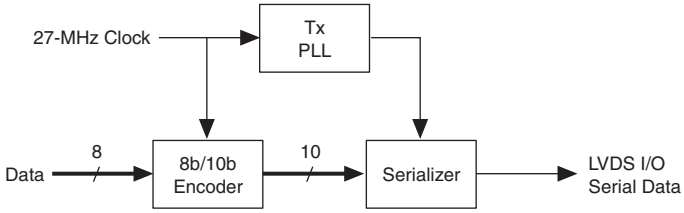
Figure 3 shows the ASI receiver elements.

Figure 3. ASI Receiver Block Diagram



The ASI transmitter consists of an 8b/10b encoder for converting an 8-bit wide word to a 10-bit wide word, as well as a serializer that converts a 10-bit parallel word into a serial data output format. A 10-bit shift register loaded at the word rate from the encoder and unloaded at the bitrate of the LVDS output buffer is implemented for that function. A PLL that multiplies a 27-MHz reference clock by ten provides the bitrate clock and enables jitter-controlled ASI transmit serialization. The ASI transmitter elements are shown in Figure 4.

Figure 4. ASI Transmitter Block Diagram



Low Cost SDI and DVB-ASI Implementation in Programmable Logic

Implementing the elements shown in these SDI and ASI solutions uses few resources in an Altera FPGA. For example, a single ASI channel requires less than 1,000 LEs. In Altera's Cyclone II FPGA, this corresponds to a cost of less than US$1 per channel—a substantially lower cost than existing ASSP solutions, which can cost upwards of US$10 or US$15 per channel or more, depending on the exact device.

With SDI, a single full-duplex port for 10-bit SD-SDI data can be implemented in an Altera FPGA in as few as 400 LEs. For 10-bit SD-SDI data in an Altera Cyclone II FPGA, this translates to a cost per port that is also substantially lower than existing ASSP-based solutions, which can cost US$30 or US$40 per port or more. With 20-bit HD-SDI data, the logic accompanying the transceiver channel requires about 1,000 LEs, which when implemented in a

Stratix GX device results in a cost per port that is equal or lower than the cost-per-port implementation in ASSPs. When the additional integration benefits of programmable logic are included, the Stratix GX-based solution for SDI becomes even more compelling.

Programmable Logic Integration Delivers Additional Benefits

In typical applications, DVB-ASI and SDI functions comprise only a portion of the total functionality of any given piece of broadcast equipment. For example, DVB-ASI is generally used in broadcast headend systems, where other signal processing operations such as video multiplexing, compression, modulation and demodulation, time-slot multiplexing, and encoding and decoding are also required. These operations require digital signal processing (DSP) functions such as forward-error correction (FEC), filtering, interleaving, quadrature amplitude modulation (QAM) mapping, and Viterbi and Reed-Solomon decoding. These functions can be implemented efficiently using the available resources within Altera FPGAs, including LEs, multipliers in Cyclone II devices, and DSP blocks in Stratix devices.

By enabling the integration of these functions into fewer devices, an FPGA-based solution further reduces development costs, board space, and system complexity. The flexibility of FPGAs also allows developers to customize the interface between each of the elements in their design, enabling them to add features and differentiating qualities with little development time. Designers can also achieve the exact number of ASI channels or SDI ports desired with a single programmable device, whereas relying on an ASSP might force them to use multiple discrete devices.

Available Reference Designs Speed Implementation

Altera's SDI and DVB-ASI solution reference designs are currently available for public download. Characterization reports for these reference designs implemented in Altera FPGAs are available from Altera upon request. In the SDI reference design, three SMPTE-recommended jitter parameters are evaluated:

- Jitter generator—A device or system that produces a serial digital signal (in this case, HD-SDI) containing sinusoidal jitter of a certain amplitude and frequency. The generated jitter can also be non-sinusoidal.
- Receive jitter tolerance—The peak-to-peak amplitude of the sinusoidal jitter that causes performance degradation when applied at the device or system input.
- Jitter transfer—The jitter on the output of the device or system resulting from the applied input jitter.

The DVB-ASI standard does not provide any specification for the jitter tolerance, but the following jitter parameters have been evaluated for Altera's DVB-ASI reference design:

- Jitter generation of the transmitter
- Jitter tolerance of the receiver
- Sensitivity of the receiver
- Output amplitude and edge rate

These reference designs can be readily demonstrated using the Altera Cyclone Video Demonstration Board and Stratix GX Serial Video Demonstration Instruction Board. See "Resources" for more information on obtaining board demonstrations.

Ease RoHS Transition With Altera Lead-Free Products

Altera maintains one of the most extensive lead-free product offerings in the industry, with over 1200 products in lead-free packages. As a preeminent supplier of environmentally friendly programmable logic solutions, Altera has shipped over 25 million lead-free products since 2002. Altera's lead-free devices comply with the maximum concentration restrictions, as required in the EU Directive on the Restriction of Hazardous Substances ("RoHS Directive") No.2002/95 with respect to lead (Pb), mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE). Help ease your RoHS transition by integrating non-compliant ASSPs with Altera's PLDs.

Conclusion

Altera's programmable logic-based solutions for DSB-ASI and SDI can significantly lower the cost of broadcast equipment development compared to ASSP-based solutions. Integration of the DVB-ASI and SDI functions into fewer devices further reduces cost, board space, and complexity. Tested solutions for these interfaces are readily available from Altera for demonstration and implementation. See "Resources" for information on where to download reference designs and how to request solution demonstrations.

Customer Success Stories

- *Miranda Technologie*s Adopts Altera Stratix GX Devices for SDI and HD-SDI Capabilities
  www.altera.com/corporate/news_room/releases/releases_archive/2004/products/nr-miranda_release.html
- TANDBERG Television Adopts Altera Stratix II Devices and Nios® II Embedded Processors to Deliver DVB-ASI
  www.altera.com/corporate/news_room/releases/releases_archive/2004/products/nr-tandberg.html

Resources

For additional information, refer to the following resources on the Altera website.

- More System Integration Solutions
  www.altera.com/technology/integration/int-index.html
- Customer Applications of Programmable Logic in Broadcast Products
  www.altera.com/broadcastsuccess
- ASI Reference Design
  www.altera.com/solutions/refdesigns/sys-sol/broadcast/ref-asi.html
- SDI Reference Design
  www.altera.com/solutions/refdesigns/sys-sol/broadcast/ref-sdi.html
- AN 339: SDI Reference Design for Stratix GX Devices
  www.altera.com/literature/an/an339.pdf
- AN 344: ASI Reference Design
  www.altera.com/literature/an/an344.pdf
- AN 356: SDI Reference Design for Cyclone & Stratix Devices
  www.altera.com/literature/an/an356.pdf

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