White Paper

Single-Resistor RSDS Solution for Cyclone II Devices

Introduction

The reduced swing differential signaling (RSDS) interface is used in flat-panel displays to implement the data transfer between the timing controller and the column drivers. The Altera® Cyclone™ II FPGA family is well suited to this interface due to its logic density, flexible I/O buffers, and low price. The Cyclone II device can implement the timing function and output the required RSDS signals to interface with the column driver.

This white paper explains how to implement the interface using a single external resistor. The single resistor solution makes the board design simple, less expensive, and more reliable. Altera's characterization of the single resistor RSDS solution was developed to meet today's RSDS speed requirements of 170 Mbps. This document covers the board-level circuit needed to create the correct signal levels according to RSDS specification and Quartus software support. Altera has verified this design through both simulation and board correlation.

RSDS Specification

The RSDS specification was developed by National Semiconductor Corporation for LDI (LVDS Display Interface), and is defined for use in chip-to-chip applications between the TCON (timing controller) and the column drivers on display panels. Characterization and simulations for Cyclone II devices were performed to meet National Semiconductor's RSDS Interface Specification. Table 1 shows these RSDS electrical characteristics.

Table 1. RSDS Electrical Characteristics for Cyclone II Devices

Symbol	Parameter	Min	Typical	Max	Units
V_{CCIO}	I/O supply voltage	2.375	2.5	2.625	V
V_{OD}	Differential output voltage	100	200	600	mV
V_{OS}	Output offset voltage	0.5	1.2	1.5	V
V_{TH}	Differential threshold			+/- 100	mV

Figures 1 and 2 show the RSDS receiver and transmitter signal waveforms, and explain the different electrical voltage levels involved in RSDS specification.

Figure 1. Receiver Input Signal Level Waveforms for RSDS

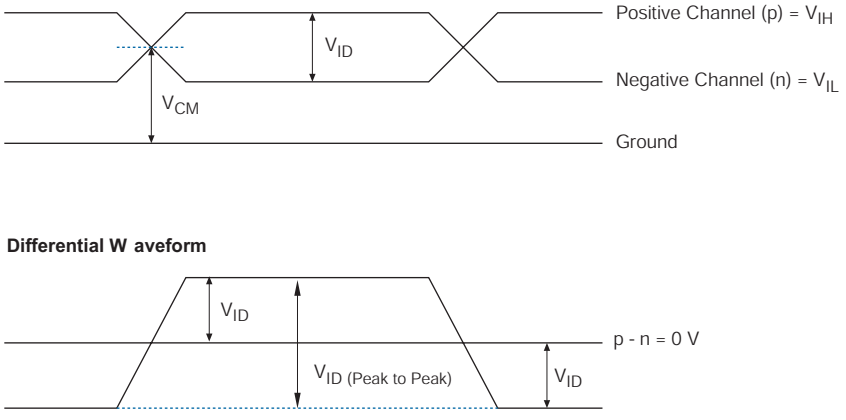
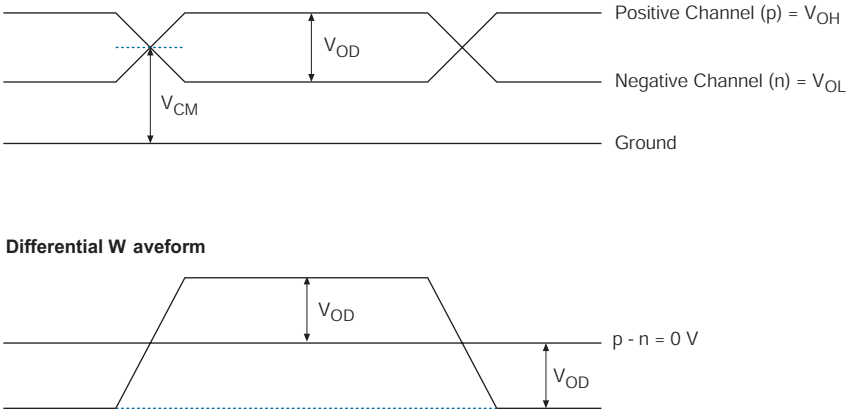


Figure 2. Transmitter Output Signal Level Waveforms for RSDS



Cyclone II FPGAs support all three bus configuration types defined by the RSDS specification:

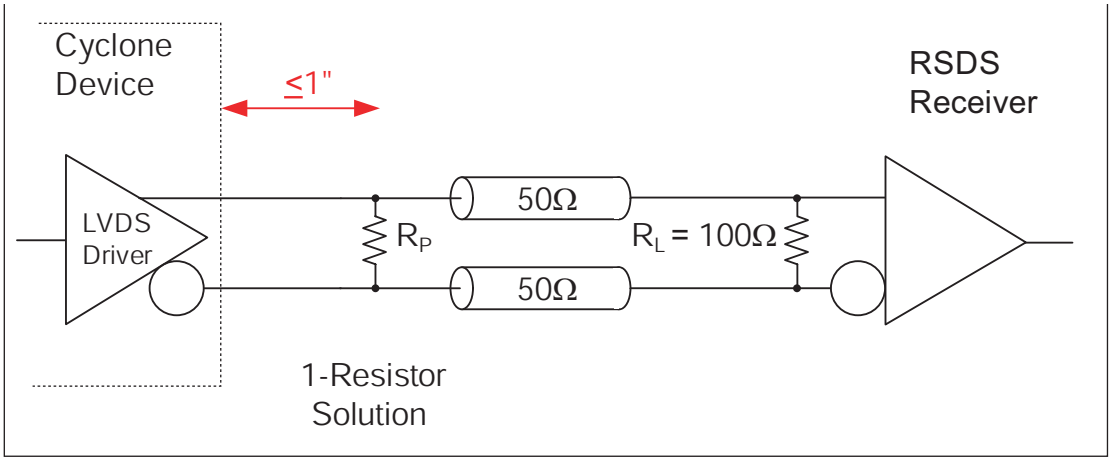
- Type 1 - Multi-drop bus with double termination
- Type 2 - Multi-drop bus with single end termination
- Type 3 - Double multi-drop bus with single termination

More information on RSDS bus configuration types can be found in the RSDS specification section of the National Semiconductor website.

Designing With RSDS

Cyclone II devices do not have differential drivers. To create the differential signal the device uses two adjacent I/Os as a differential pair along with an external on-board parallel resistor. The I/O bank in which the RSDS I/Os reside should be supplied with a 2.5-V power supply. (Refer to the software section on how to enable single resistor RSDS I/Os in Quartus development software.) To transmit an RSDS signal, an external resistor (R_P) is connected in parallel between the two adjacent I/O pins on the board as shown in Figure 1. The recommended value of the resistor for all RSDS bus configurations is 100Ω (tolerance of 1%). Altera has verified this design through simulation and board correlation. A copy of the characterization data can be obtained by contacting Altera.

Figure 3. RSDS Resistor Network

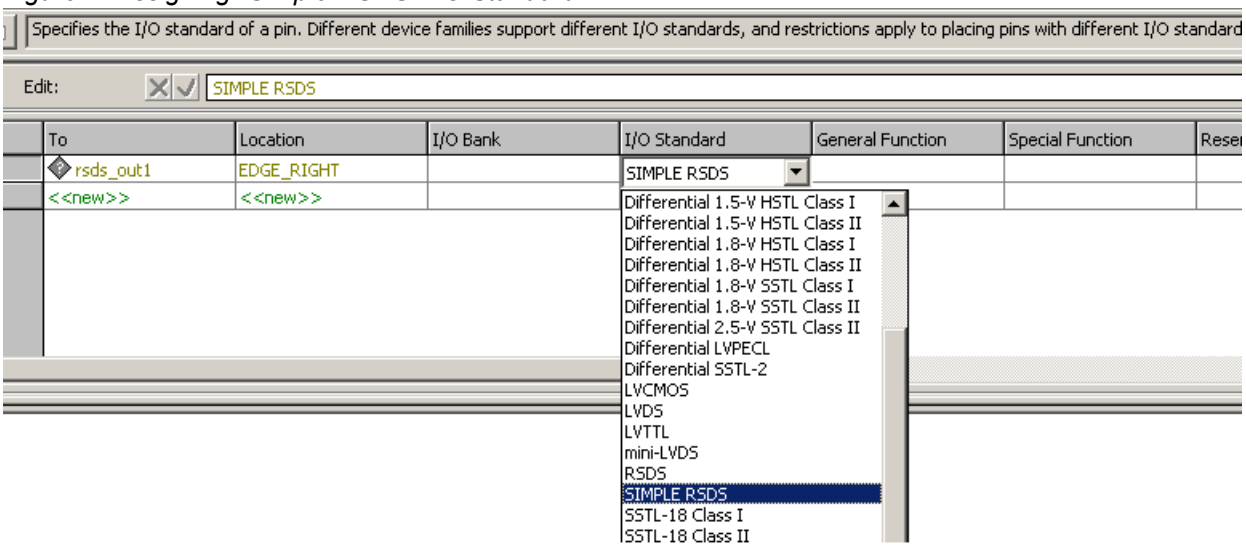


Quartus Software Support

Support for single resistors will be available in Quartus development software version 5.1. To assign single-resistor RSDS I/O standards:

1. Select the pins to be assigned RSDS I/O standards and go to those pins within the Assignments section.
2. In the I/O standard option, select "simple RSDS" as shown in Figure 4.
3. Save and compile.

Figure 4. Assigning "Simple RSDS" I/O Standard



Summary

This document describes how to implement single resistor RSDS I/Os in Altera's Cyclone II devices and the benefits of doing so. Cyclone II devices support multiple I/O standards such as LVDS, RSDS, and mini-LVDS typically used in flat panel display applications. Along with these flexible I/Os, the logic density, dedicated memory interfaces, and internal memory of these devices makes them an ideal choice for implementing the timing controller functionality. Altera also offers design examples and reference design boards to implement and prototype most of the display interfaces.

Additional Resources

- National Semiconductor's RSDS Specification: **www.national.com/appinfo/fpd/0,2132,943,00.html**

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