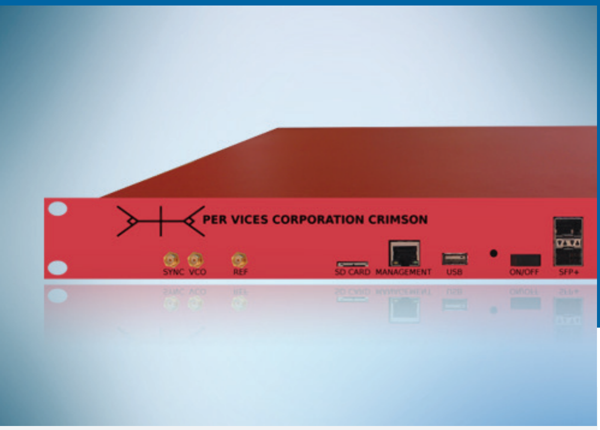
DESIGN SOLUTION: A CUSTOMER SUCCESS STORY




# Forging a Single Agile Radio Platform for Signal Intelligence and Public Safety

*By **Brandon Malatest**, COO, Per Vices*

## The Design Team:

Per Vices, based in Toronto, Ontario, develops revolutionary hardware/software systems for a wide range of markets including communications, security analysis, defense, and public safety.

## Challenge:

Military applications such as signal intelligence, IED countermeasures, and electronic warfare, as well as communications systems for public-safety responders have many common requirements. But today's point-solution approach to hardware and software increases costs, and often leads to critical communications lapses in emergency situations. The flexibility to span these applications on a common platform cannot be achieved at required performance simply by moving baseband functions into software.

## Solution:

A single programmable platform that can cover a huge range of frequencies, modulation techniques and baseband processing algorithms allows a single hardware base to span a wide range of military and public-safety needs. A unique approach to combining software and programmable logic in baseband processing achieves the required flexibility and performance within the power, size, and cost constraints of mobile systems.

## The Project: Crimson Software-Defined Radio

In today's technology landscape two quite different application areas—one spanning military signal intelligence, countermeasures, and electronic warfare and the other comprising communications for public-safety first responders—have needs that sound very different, but at their root are very similar. Military organizations need agile radios that can scan a broad band, detect and analyze signals, and in some applications jam them. Such situations come up in electronic surveillance, battlefield communications and countermeasures, measures to defeat improvised explosive devices (IEDs), and a wide range of electronic-warfare applications. All of the systems to meet these needs are structurally similar, but quite different in functional specifics. There currently exist multiple hardware and software combined solutions required for each different application. This results in different hardware (and therefore training) for applications in signals intelligence, communications, counter IED, and (counter) electronic warfare.

The situation for civilian first responders sounds quite different. This problem, best explained as the inability of first responders from different agencies to communicate among themselves, is both challenging and life-threatening. Interoperability today is limited by incompatible radio systems that operate on different frequency bands and/or use different protocols, requiring ad-hoc bridges between networks.

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The solution to both sets of problems would be a radio transceiver platform that was software-configurable over a vast range of frequencies, modulation schemes, and baseband processing algorithms. Per Vices has developed a software-defined radio (SDR) platform to meet these needs. Crimson provides the flexibility these use cases require, with a form-factor and energy consumption appropriate for the role. We have completed the design and development of a wide-band, flexible hardware platform operating from DC up to 6GHz with four independently controllable receive and four independently controllable transmit chains each having very high RF bandwidth (up to 322MHz per chain).

## The Design Challenge

With Per Vices, we use a single piece of hardware which enables different software applications to be executed on the platform for functionality as a signals intelligence platform, communications device, counter IED product, and (counter) electronic warfare solution. Achieving this design required overcoming a number of technical barriers, including development of an extraordinarily wide-band RF front end and up/down-converters and use of very high-bandwidth data converters to bridge the analog and digital domains.

But perhaps the greatest challenge lay in the baseband digital processing. We found that while software is an appropriate medium for expressing the full range of baseband algorithms users might require, software executing on a conventional CPU is simply not fast enough or energy-efficient enough to meet the real-time requirements of these applications. It was necessary to have a hardware implementation for critical parts of these algorithms.

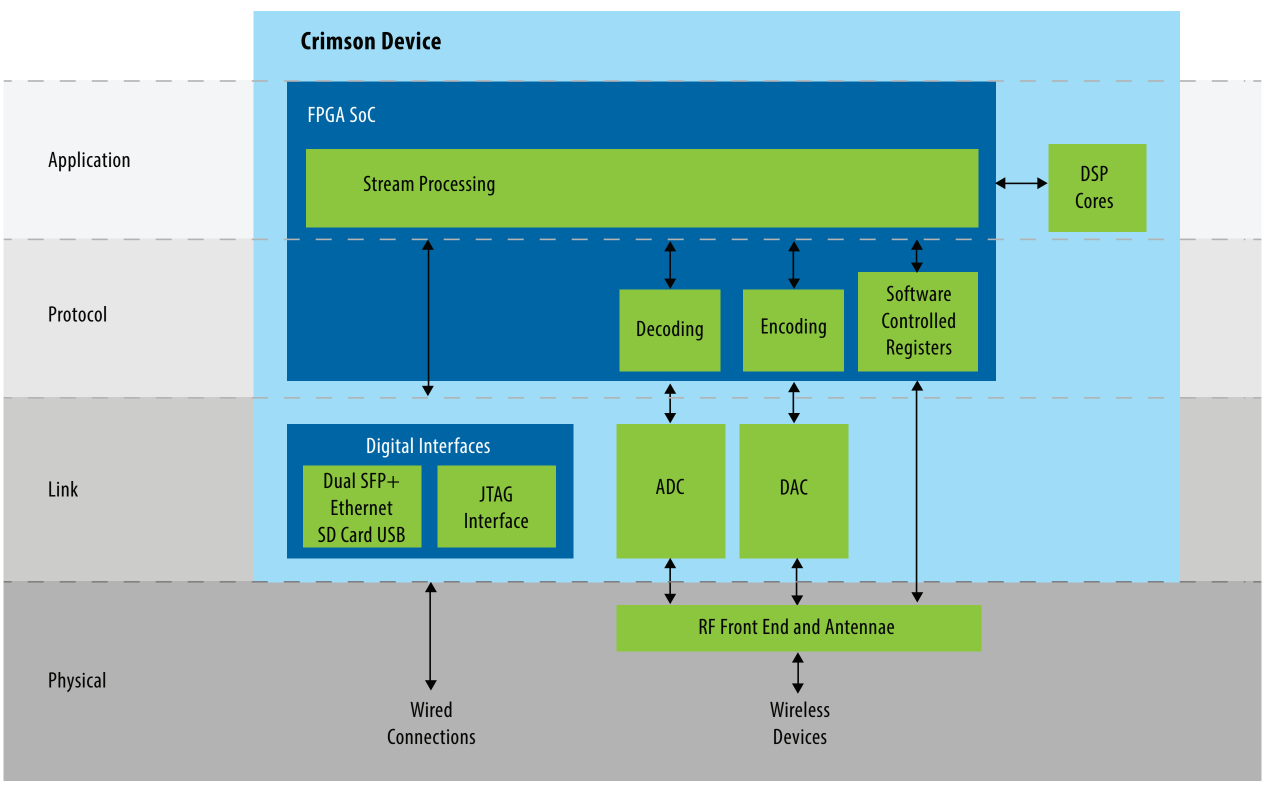
But the traditional approach—dedicated hardware for each application—gives up all the advantages of SDR. Per Vices needed another alternative.

# The Design Solution

Per Vices's current product, the Crimson Transceiver, is a Software Defined Radio (SDR) capable of arbitrary signal processing, concurrent demodulation of wide band RF signals, and the ability to transparently substitute for existing wireless devices. Whereas traditional wireless technology requires dedicated hardware designed for a dedicated purpose, the value of our products lies in decoupling hardware design from the application. We enable hardware capabilities to be arbitrarily exploited by software applications. This is analogous to the evolution of computers, from mechanical calculators whose design defined purpose to mobile phones whose utility is defined by the software applications they run.

The Crimson hardware platform comprises a set of dedicated physical and link-layer interfaces and an FPGA SoC that provides both embedded CPUs and programmable logic for digital signal processing and application-dependent stream processing (Figure 1). The FPGA not only provides digital signal processing chains, but makes it possible to develop an application in software and then accelerate critical portions in configurable hardware without making physical changes to the hardware platform. This capability delivers the flexibility the intended markets require.

Figure 1: The Crimson system block diagram

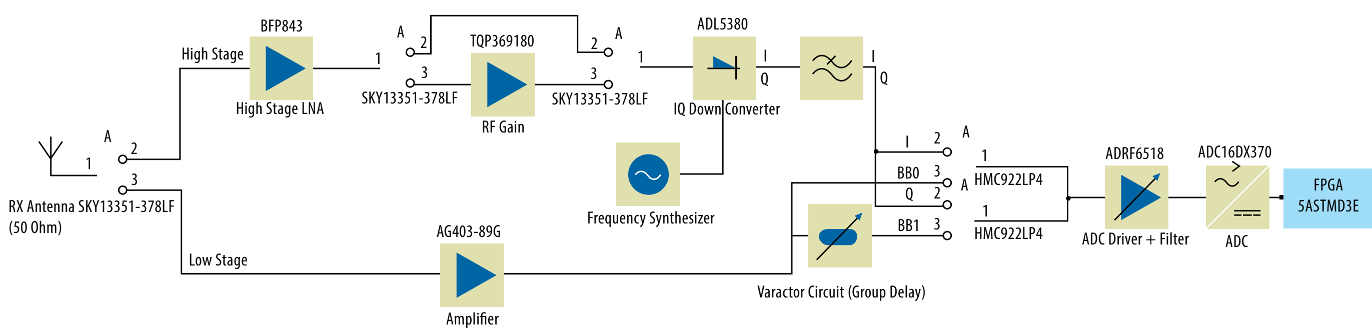


# Theory of Operation

## RX Chain Overview

The signal is first sampled from the antenna which is connected to the SMA connector on the Crimson (Figure 2). The analog signal is fed through an RF switch based on the frequency of the signal being sampled. High band is reserved for signals greater than 500 MHz, and the low band is reserved for signals less than 500 MHz. Crimson currently supports signals up to 6 GHz. Within the respective RF chains (high and low), the RX chain filters the analog signal and divides it into I and Q channels for advanced signal processing on the FPGA. The high band offers an LNA for weaker signals, and a frequency mixer for desired intermediate frequencies prior to signal processing. The low band offers a varactor circuit to fine tune the delay between the I and Q channel. An ADC driver is common between both bands (high and low) prior to the ADC. The ADC will send the data across to the DSP chain within the FPGA at a rate of 322 MSPS using the JESD serial interface. The DSP chain will downsample the samples resulting in an adjusted final sample rate. The frequency of the signal can be adjusted prior to decimation.

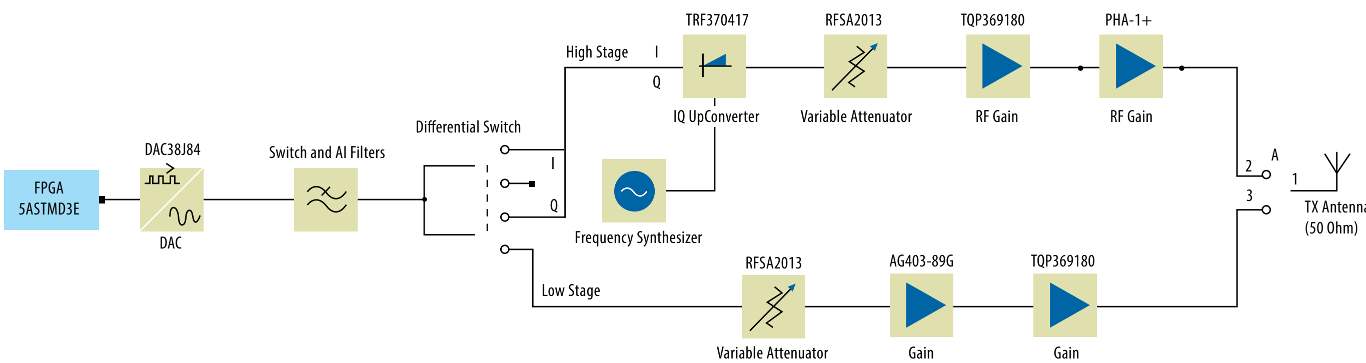
Figure 2: The Crimson receiver chain



## TX Chain Overview

The digital signal produced by application-dependent circuitry in the FPGA gets interpolated through the DSP chain on the FPGA (Figure 3). The interpolation can go up to a maximum of 322 MSPS and can be frequency-adjusted prior to DAC conversion. The digital signal is sent to the RF frontend using the JESD serial interface, providing the DAC both I and Q channel values. The analog signal passes through an RF switch for high band or low band selection. The high band is reserved for signals greater than 500 MHz and the low band is reserved for signals under 500 MHz. The high band offers a frequency mixer for up-conversion up to a maximum of 6 GHz.

Figure 3: The Crimson transmitter chain



### Digital Board Overview

The digital board houses the FPGA with the SoC ARM Cortex-A9 Processor hard processing system and interface for JESD communication between the boards. The digital board is required for communicating with the RX and TX board, and retrieves all of the clocks through the Synth board. The digital board supports 20Gbps I/O to the host system using dual 10GbE, and digital down/up conversion on the FPGA with Per Vices DSP IP cores. The ADC and DAC chains are hardware running on the Arria V ST FPGA, and include a series of filters before signals feed to and from the 10GbE SFP + Port.

### Clock (Frequency Synthesizer) Overview

The synth board is used for generating all of the clocks for the Digital, TX, and RX boards. This includes the on-board IC clocks, JESD sysref clock, and synthesizer clocks. A couple of configurations are possible with the synth board. The 10MHz clock reference can be chosen between an internal or external SMA source. The 10MHz steps up to 100MHz with a feedback circuit. This architecture maintains the high 10MHz source precision with low phase noise associated with the 100MHz PLL. The fanout buffer will propagate the 100MHz signal to the other boards (RX, TX, and Digital), and feed an LMK04828 to generate the JESD-compliant signals.

## Results

Per Vices has developed and tested the hardware and is now starting on the software application layer. For the defense applications, we have developed signals intelligence applications for spread spectrum monitoring, emanation reconstruction, (counter) electronic warfare, and signal jamming. In communications we have developed point to point communication using non allocated frequencies. Work is proceeding to produce other applications.

**Altera Corporation**
101 Innovation Drive
San Jose, CA 95134
USA
Telephone: (408) 544 7000
**www.altera.com**

**Altera European Headquarters**
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 494 602 000

**Altera European Trading Company Ltd.**
Building 2100
Cork Airport Business Park,
Cork, Republic of Ireland
Telephone: +353 21 454 7500

**Altera Japan Ltd.**
Shinjuku i-Land Tower 32F
6-5-1, Nishi Shinjuku
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
**www.altera.co.jp**

**Altera International Ltd.**
Unit 11- 18, 9/F
Millennium City 1, Tower 1
388 Kwun Tong Road
Kwun Tong
Kowloon, Hong Kong
Telephone: (852) 2945 7000
**www.altera.com.cn**

**Altera Corporation Technology Center**
Plot 6, Bayan Lepas Technoplex
Medan Bayan Lepas
11900 Bayan Lepas
Penang, Malaysia
Telephone: 604 636 6100