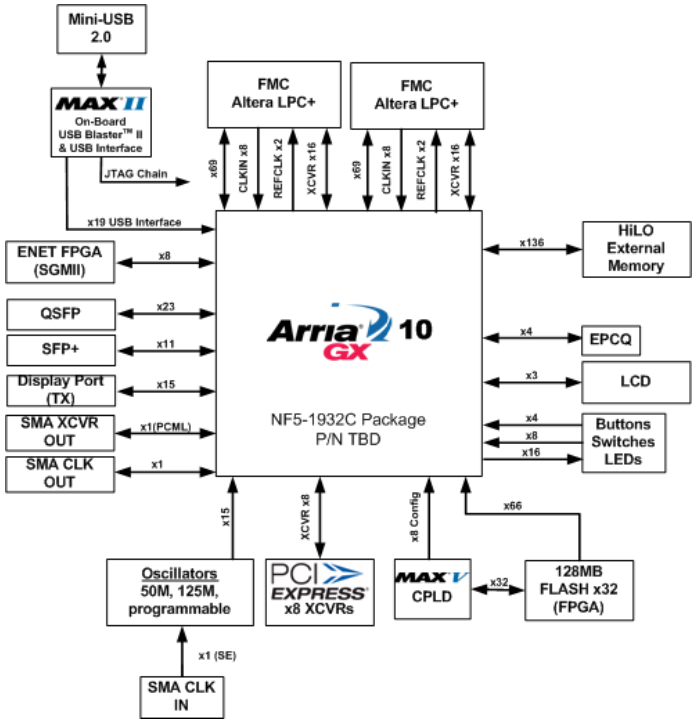
NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0321301-E3
Gerber Files	110-0321301-E3
PCB Design Files	120-0321301-E3
Assembly Drawing	130-0321301-E3
Fab Drawing	140-0321301-E3
Schematic Drawing	150-0321301-E3
PCB Film	160-0321301-E3
Bill of Materials	170-0321301-E3
Schematic Design Files	180-0321301-E3
Functional Specification	210-0321301-E3
PCB Layout Guidelines	220-0321301-E3
Assembly Rework	320-0321301-E3

2. 1516 Parts, 84 Library Parts, 1524 Nets, 7856 Pins

Arria 10 FPGA Development Kit



REV	DATE	PAGES	DESCRIPTION

PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Rev. History	37	Power1 A10 VCC ET4040 (2)
2	Clock Diagram	38	Power2 - A10 VCCRAM
3	PCI Express Edge Connector	39	Power2 - A10 VCCR GXB
4	Arria 10 GX Bank 2	40	Blank Page
5	Arria 10 GX Bank 3A-3D	41	Power3 - A10 VCCPT/1.8V
6	Arria 10 GX Bank 3E-3H	42	Power4 - A10 VCCIO 1.8V
7	Arria 10 Configuration	43	Power4 - A10 VCCIO FMCA
8	Arria 10 Clocks	44	Power4 - A10 VCCIO FMCB
9	PLL	45	Power4 - A10 VCCIO MEM
10	PLL2	46	Arria 10 Power
11	Arria 10 XCVR Left (B1)	47	Arria 10 Ground
12	Arria 10 XCVR Right (B4)	48	Decoupling
13	5M2210 System Controller	49	Power-Down Discharge
14	Flash	50	
15	10/100/1000 Ethernet PHY	51	
16	EMI Connector Map	52	
17	External Memory Interface	53	
18	DisplayPort (x4)	54	
19	FMC Port A	55	
20	FMC Port B	56	
21	QSFP	57	
22	SFP+	58	
23	SDI Transmit/Receive	59	
24	User IO	60	
25	On-Board USB Blaster II -1	61	
26	On-Board USB Blaster II -2	62	
27	Power Tree	63	
28	Power Sequence Diagram	64	
29	Voltage & Temperature Sense	65	
30	Power Sequence Control	66	
31	Power - Select Power Input	67	
32	Power - DCin to 3.3V	68	
33	Power - 3.3V & 5.0V		
34	Power - MEM_VDD & 2.5V		
35	Power1 - A10 VCC		
36	Power1 A10 VCC ET4040 (1)		

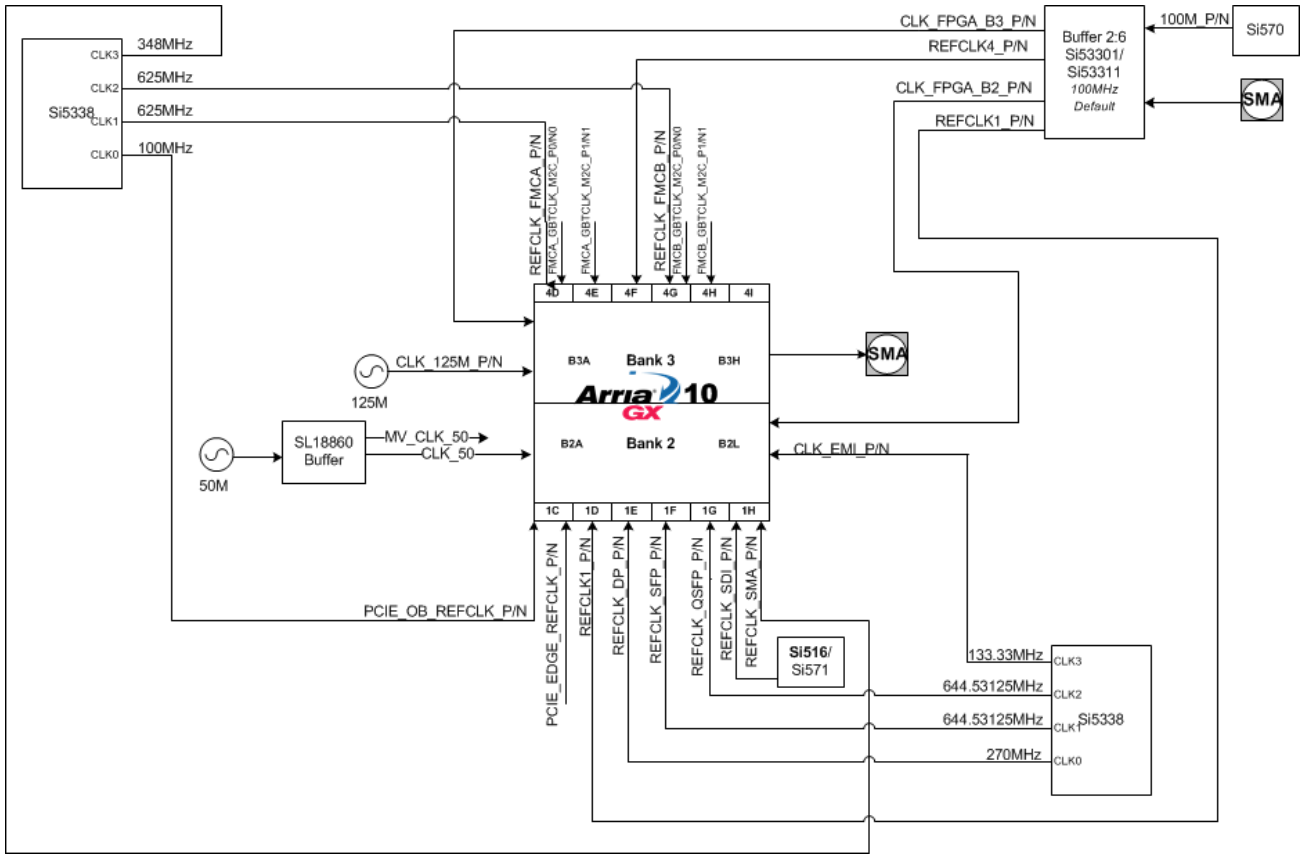
Altera Corporation, 101 Innovation Dr., San Jose CA 95134

Title: **Arria 10 GX FPGA Development Kit**

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 1 of 49

Clock Diagram

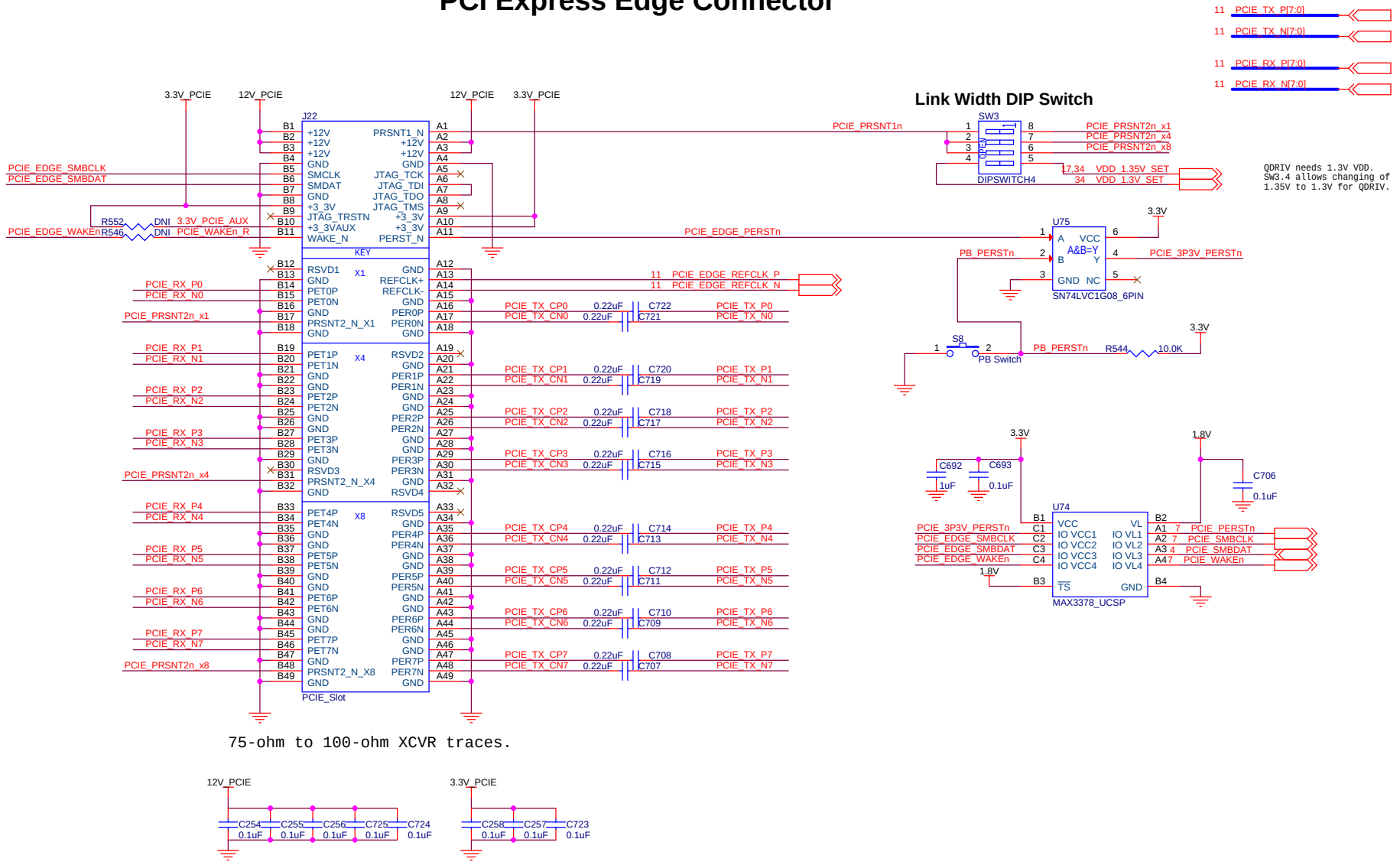


Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 2 of 49

PCI Express Edge Connector



75-ohm to 100-ohm XCVR traces.

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 3 of 49

Arria 10 GX Bank 2

U28C

ARRIA 10 - BANK 2I-2L

QSFP_LP_MODE	AK34	IO,LVDS2I_1P,DQ12L	BANK-2I		
QSFP_INTERRUPTn	AL34	IO,LVDS2I_1N,DQ12L			
DP_HOT_PLUG	AM30	IO,LVDS2I_2P,DQ12L			
CLOCK_SDA	AN30	IO,LVDS2I_2N,DQ12L			
	AL32	IO,LVDS2I_3P,DQ12L			
DP_RETURN	AL33	IO,LVDS2I_3N,DQ12L			
DP_CONFIG2	AK32	IO,LVDS2I_5P,DQ12L			
DP_CONFIG1	AK31	IO,LVDS2I_5N,DQ12L			
	AM31	IO,LVDS2I_6P,DQ12L			
	AM32	IO,LVDS2I_6N,DQ12L			
DP_AUX_CH_P	AN34	IO,LVDS2I_4P,DQS12L	VCCIO = 1.8V		
ENABLE ARRIA 10 OCT -> DP_AUX_CH_N	AM35	IO,LVDS2I_4N,DQSN12L			
	AR32	IO,LVDS2I_7P,DQ13L			
	AP32	IO,LVDS2I_7N,DQ13L			
	AT37	IO,LVDS2I_8P,DQ13L			
PCIE_SMBDAT	AU37	IO,LVDS2I_8N,DQ13L			
	AP34	IO,LVDS2I_9P,DQ13L			
	AP33	IO,LVDS2I_9N,DQ13L			
100, 1% R449 RZQ_B2I	AR34	IO,RZQ_2I,LVDS2I_11P,DQ13L		IO,RZQ_2K,LVDS2K_11P,DQ5L	J34 24 RZQ_B2K
SFP_TX_DISABLE	AR35	IO,LVDS2I_11N,DQ13L		IO,LVDS2K_11N,DQ5L	H34 MEM_ADDR_CMD12
SFP_MOD0_PRSNTn	AT30	IO,LVDS2I_14P,DQ14L		IO,LVDS2K_14P,DQ6L	J33 MEM_ADDR_CMD8
SFP_MOD2_SDA	AR31	IO,LVDS2I_14N,DQ14L		IO,LVDS2K_14N,DQ6L	J32 MEM_ADDR_CMD9
SFP_RS1	AT34	IO,LVDS2I_16P,DQS14L		IO,LVDS2K_17P,DQ6L	N34 MEM_ADDR_CMD2
SFP_TX_FAULT	AT35	IO,LVDS2I_16N,DQSN14L		IO,LVDS2K_17N,DQ6L	M35 MEM_ADDR_CMD3
SFP_RS0	AN31	IO,LVDS2I_17P,DQ14L		IO,LVDS2K_18P,DQ6L	M32 MEM_ADDR_CMD0
SFP_MOD1_SCL	AP31	IO,LVDS2I_17N,DQ14L		IO,LVDS2K_18N,DQ6L	L32 MEM_ADDR_CMD1
QSFP_SDA	AU31	IO,LVDS2I_18P,DQ14L		IO,LVDS2K_16P,DQS6L	L34 MEM_ADDR_CMD4
SFP_RX_LOS	AU30	IO,LVDS2I_18N,DQ14L		IO,LVDS2K_16N,DQSN6L	K34 MEM_ADDR_CMD5
QSFP_MOD_PRSn	AU36	IO,LVDS2I_19P,DQ15L		IO,LVDS2K_19P,DQ7L	U32 MEM_ADDR_CMD30
QSFP_MOD_SELn	AU35	IO,LVDS2I_19N,DQ15L		IO,LVDS2K_19N,DQ7L	T32 MEM_ADDR_CMD31
QSFP_SCL	AV34	IO,LVDS2I_20P,DQ15L		IO,LVDS2K_20P,DQ7L	R30 MEM_CLK_P
QSFP_RSTn	AV35	IO,LVDS2I_20N,DQ15L		IO,LVDS2K_20N,DQ7L	R31 MEM_CLK_N
SDI_MF2_MUTE	AY35	IO,LVDS2I_21P,DQ15L		IO,LVDS2K_21P,DQ7L	U33 MEM_ADDR_CMD20
SDI_TX_SD_HDn	AW34	IO,LVDS2I_21N,DQ15L		IO,LVDS2K_21N,DQ7L	T33 MEM_ADDR_CMD21
DISP_I2C_SCL	AW33	IO,LVDS2I_23P,DQ15L		IO,LVDS2K_23P,DQ7L	R34 MEM_ADDR_CMD22
CLOCK_SCL	AV33	IO,LVDS2I_23N,DQ15L		IO,LVDS2K_23N,DQ7L	P34 MEM_ADDR_CMD23
DISP_I2C_SDA	AY34	IO,LVDS2I_24P,DQ15L		IO,LVDS2K_24P,DQ7L	T34 MEM_ADDR_CMD28
DISP_SPISS	BA35	IO,LVDS2I_24N,DQ15L		IO,LVDS2K_24N,DQ7L	T35 MEM_ADDR_CMD27
SDI_MF0_BYPASS	AW32	IO,LVDS2I_22P,DQS15L		IO,LVDS2K_22P,DQS7L	N33 MEM_ADDR_CMD24
SDI_MF1_AUTO_SLEEP	AY32	IO,LVDS2I_22N,DQSN15L		IO,LVDS2K_22N,DQSN7L	P33 MEM_ADDR_CMD25
MEM_DQB0	AC31	IO,LVDS2J_1P,DQ8L	BANK-2J	IO,LVDS2L_1P,DQ0L	D26 MEM_DQA6
MEM_DQB4	AD31	IO,LVDS2J_1N,DQ8L		IO,LVDS2L_1N,DQ0L	E26 MEM_DMA0
MEM_DQB6	AD33	IO,LVDS2J_2P,DQ8L		IO,LVDS2L_2P,DQ0L	A28 MEM_DQA1
MEM_DQB5	AD32	IO,LVDS2J_2N,DQ8L		IO,LVDS2L_2N,DQ0L	A27 MEM_DQA2
MEM_DMB0	AB32	IO,LVDS2J_3P,DQ8L		IO,LVDS2L_3P,DQ0L	B28 MEM_DQA0
MEM_DQB1	AB31	IO,LVDS2J_3N,DQ8L		IO,LVDS2L_3N,DQ0L	B27 MEM_DQA3
MEM_DQB3	Y31	IO,LVDS2J_5P,DQ8L		IO,LVDS2L_5P,DQ0L	D27 MEM_DQA4
MEM_DQB2	W31	IO,LVDS2J_5N,DQ8L		IO,LVDS2L_5N,DQ0L	E27 MEM_DQA5
MEM_QKB_P0	Y30	IO,LVDS2J_6P,DQ8L		IO,LVDS2L_6P,DQ0L	C28 MEM_QKA_P0
QDR4 QKB_P0 -> MEM_DQB7	AA30	IO,LVDS2J_6N,DQ8L		IO,LVDS2L_6N,DQ0L	D28 MEM_DQA7 <- QDR4 QKA_P0
MEM_DQSB_P0	Y32	IO,LVDS2J_4P,DQS8L		IO,LVDS2L_4P,DQS0L	B26 MEM_DQSA_P0
MEM_DQSB_N0	AA32	IO,LVDS2J_4N,DQSN8L	VARIABLE EMI VCCIO (1.2V, 1.35V, 1.5V)	IO,LVDS2L_4N,DQSN0L	C26 MEM_DQSA_N0
MEM_DQB8	AE31	IO,LVDS2J_7P,DQ9L		IO,LVDS2L_7P,DQ1L	F28 MEM_DQA15
MEM_DQB9	AE32	IO,LVDS2J_7N,DQ9L		IO,LVDS2L_7N,DQ1L	F27 MEM_DQA13
MEM_DQB10	AE30	IO,LVDS2J_8P,DQ9L		IO,LVDS2L_8P,DQ1L	G28 MEM_DQA12
MEM_DQB11	AF30	IO,LVDS2J_8N,DQ9L		IO,LVDS2L_8N,DQ1L	G27 MEM_DMA1
MEM_DQB12	AG33	IO,LVDS2J_9P,DQ9L		IO,LVDS2L_9P,DQ1L	H25 MEM_DQA9
MEM_DQB14	AH33	IO,LVDS2J_9N,DQ9L		IO,LVDS2L_9N,DQ1L	G25 MEM_DQA8
MEM_DQB32	AF32	IO,RZQ_2J,LVDS2J_11P,DQ9L		IO,RZQ_2L,LVDS2L_11P,DQ1L	J28 MEM_DQA32
MEM_DQB13	AG32	IO,LVDS2J_11N,DQ9L		IO,LVDS2L_11N,DQ1L	K27 MEM_DQA14
MEM_DQB18	W32	IO,LVDS2J_14P,DQ10L		IO,LVDS2L_14P,DQ2L	D31 MEM_DQA16
MEM_DQB17	W33	IO,LVDS2J_14N,DQ10L		IO,LVDS2L_14N,DQ2L	C31 MEM_DQA19
MEM_DQB21	W35	IO,LVDS2J_17P,DQ10L		IO,LVDS2L_17P,DQ2L	E30 MEM_DQA21
MEM_DMB2	Y35	IO,LVDS2J_17N,DQ10L		IO,LVDS2L_17N,DQ2L	E31 MEM_DQA17
MEM_QKB_P1	V33	IO,LVDS2J_18P,DQ10L		IO,LVDS2L_18P,DQ2L	E29 MEM_QKA_P1
QDR4 QKB_P1 -> MEM_DQB23	V34	IO,LVDS2J_18N,DQ10L		IO,LVDS2L_18N,DQ2L	D29 MEM_DQA23 <- QDR4 QKA_P1
MEM_DQSB_P2	AA34	IO,LVDS2J_16P,DQS10L		IO,LVDS2L_16P,DQS2L	C30 MEM_DQSA_P2
MEM_DQSB_N2	AA33	IO,LVDS2J_16N,DQSN10L		IO,LVDS2L_16N,DQSN2L	C29 MEM_DQSA_N2
MEM_DQB31	AD34	IO,LVDS2J_19P,DQ11L		IO,LVDS2L_19P,DQ3L	F30 MEM_DMA3
MEM_DMB3	AC34	IO,LVDS2J_19N,DQ11L		IO,LVDS2L_19N,DQ3L	F29 MEM_DQA31
MEM_DQB33	AB33	IO,LVDS2J_20P,DQ11L		IO,LVDS2L_20P,DQ3L	K29 MEM_DQA29
MEM_DQB30	AC33	IO,LVDS2J_20N,DQ11L		IO,LVDS2L_20N,DQ3L	J29 MEM_DQA30
MEM_DQB28	AD35	IO,LVDS2J_21P,DQ11L		IO,LVDS2L_21P,DQ3L	K31 MEM_DQA27
MEM_DQB29	AE34	IO,LVDS2J_21N,DQ11L		IO,LVDS2L_21N,DQ3L	K30 MEM_DQA24
MEM_DQB26	AJ33	IO,LVDS2J_23P,DQ11L		IO,LVDS2L_23P,DQ3L	G30 MEM_DQA26
MEM_DQB25	AJ34	IO,LVDS2J_23N,DQ11L		IO,LVDS2L_23N,DQ3L	G31 MEM_DQA33
MEM_DQB27	AH34	IO,LVDS2J_24P,DQ11L		IO,LVDS2L_24P,DQ3L	H29 MEM_DQA28
MEM_DQB24	AH35	IO,LVDS2J_24N,DQ11L		IO,LVDS2L_24N,DQ3L	H30 MEM_DQA25
MEM_DQSB_P3	AF33	IO,LVDS2J_22P,DQS11L		IO,LVDS2L_22P,DQS3L	L30 MEM_DQSA_P3
MEM_DQSB_N3	AF34	IO,LVDS2J_22N,DQSN11L		IO,LVDS2L_22N,DQSN3L	L29 MEM_DQSA_N3

10AX115F1932C

Stratix 5 RZQ
100-ohm for 50-ohm RT or 25-ohm RS.

CLOCK INTERFACE
- 9 CLOCK_SDA
- 9 CLOCK_SCL

DISPLAYPORT INTERFACE
- 18 DP_HOT_PLUG
- 18 DP_RETURN
- 18 DP_AUX_CH_P
- 18 DP_AUX_CH_N
- 18 DP_CONFIG1
- 18 DP_CONFIG2
- 24 DISP_I2C_SCL
- 24 DISP_I2C_SDA
- 24 DISP_SPISS

QSFP INTERFACE
- 21 QSFP_MOD_SELn
- 21 QSFP_RSTn
- 21 QSFP_SCL
- 21 QSFP_SDA
- 21 QSFP_INTERRUPTn
- 21 QSFP_MOD_PRSn
- 21 QSFP_LP_MODE

SFP+ INTERFACE
- 22 SFP_RS0
- 22 SFP_RS1
- 22 SFP_TX_DISABLE
- 22 SFP_RX_LOS
- 22 SFP_TX_FAULT
- 22 SFP_MOD0_PRSNTn
- 22 SFP_MOD1_SCL
- 22 SFP_MOD2_SDA

SDI INTERFACE
- 13,23 SDI_MF2_MUTE
- 13,23 SDI_MF0_BYPASS
- 13,23 SDI_MF1_AUTO_SLEEP
- 13,23 SDI_TX_SD_HDn

PCIe INTERFACE
- 3 PCIE_SMBDAT

MEMORY INTERFACE
- 8,17 MEM_ADDR_CMD[31:0]
- 17 MEM_CLK_P
- 17 MEM_CLK_N
- 17 MEM_DQ_ADDR_CMD[8:0]
- 17 MEM_DQS_ADDR_CMD_P
- 17 MEM_DQS_ADDR_CMD_N
- 8,17 MEM_DMA[3:0]
- 8,17 MEM_DQA[33:0]
- 8,17 MEM_DQSA_P[3:0]
- 8,17 MEM_DQSA_N[3:0]
- 17 MEM_QKA_P[1:0]
- 8,17 MEM_DMB[3:0]
- 8,17 MEM_DQB[33:0]
- 8,17 MEM_DQSB_P[3:0]
- 8,17 MEM_DQSB_N[3:0]
- 17 MEM_QKB_P[1:0]

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 4 of 49

Arria 10 Bank 3A-3D

U28D

ARRIA 10 - BANK 3A-3D

		BANK-3A		BANK-3C		
FM_D28	AP22	IO,LVDS3A_1P,DQ60R		IO,LVDS3C_1P,DQ52R	AU10	FMCA_SCL
FM_D20	AP23	IO,LVDS3A_1N,DQ60R		IO,LVDS3C_1N,DQ52R	AV10	FMCA_SDA
FM_D16	AT25	IO,LVDS3A_2P,DQ60R		IO,LVDS3C_2P,DQ52R	AU11	FMCA_LA_TX_P9
FM_D27	AR25	IO,LVDS3A_2N,DQ60R		IO,LVDS3C_2N,DQ52R	AU12	FMCA_LA_TX_N9
FM_D26	AT23	IO,LVDS3A_3P,DQ60R		IO,LVDS3C_3P,DQ52R	AW13	FMCA_LA_TX_P4
FM_D22	AT24	IO,LVDS3A_3N,DQ60R		IO,LVDS3C_3N,DQ52R	AV13	FMCA_LA_TX_N4
FM_D12	AP26	IO,LVDS3A_5P,DQ60R		IO,LVDS3C_5P,DQ52R	AV11	FMCA_LA_TX_P2
FM_D15	AR26	IO,LVDS3A_5N,DQ60R		IO,LVDS3C_5N,DQ52R	AW11	FMCA_LA_TX_N2
FM_D24	AU23	IO,LVDS3A_6P,DQ60R		IO,LVDS3C_6P,DQ52R	AY10	FMCA_LA_TX_P10
FM_D30	AU22	IO,LVDS3A_6N,DQ60R		IO,LVDS3C_6N,DQ52R	AY11	FMCA_LA_TX_N10
FM_D25	AR24	IO,LVDS3A_4P,DQS60R		IO,LVDS3C_4P,DQS52R	AW12	FMCA_LA_RX_P9
FM_D19	AP24	IO,LVDS3A_4N,DQSN60R		IO,LVDS3C_4N,DQSN52R	AY12	FMCA_LA_RX_N9
		VCCIO = 1.8V		FMCA VARIABLE VCCIO DEFAULT 1.8V (1.2V, 1.5V, 1.8V)		
FM_D14	BA25	IO,LVDS3A_7P,DQ61R		IO,LVDS3C_7P,DQ53R	AR9	FMCA_LA_TX_P7
FM_D4	AY25	IO,LVDS3A_7N,DQ61R		IO,LVDS3C_7N,DQ53R	AT9	FMCA_LA_TX_N7
FM_D6	AY24	IO,LVDS3A_8P,DQ61R		IO,LVDS3C_8P,DQ53R	AT13	FMCA_LA_RX_P6
FM_D13	BA24	IO,LVDS3A_8N,DQ61R		IO,LVDS3C_8N,DQ53R	AU13	FMCA_LA_RX_N6
FM_D2	AU25	IO,LVDS3A_9P,DQ61R		IO,LVDS3C_9P,DQ53R	AU8	FMCA_LA_RX_P8
FM_D7	AV25	IO,LVDS3A_9N,DQ61R		IO,LVDS3C_9N,DQ53R	AT8	FMCA_LA_RX_N8
FM_D11	AW22	RZQ_3A,LVDS3A_11P,DQ61R		IO,RZQ_3C,LVDS3C_11P,DQ53R	AP14	RZQ_B3C
FLASH_RDYBSYn0	AY22	IO,LVDS3A_11N,DQ61R		IO,LVDS3C_11N,DQ53R	AP13	
FLASH_ADVn	BC25	IO,LVDS3A_14P,DQ62R		IO,LVDS3C_14P,DQ54R	BD13	
FLASH_CLK	BB25	IO,LVDS3A_14N,DQ62R		IO,LVDS3C_14N,DQ54R	BD12	
FLASH_WEn	BD26	IO,LVDS3A_17P,DQ62R		IO,LVDS3C_17P,DQ54R	BC14	
FLASH_OEn	BC26	IO,LVDS3A_17N,DQ62R		IO,LVDS3C_17N,DQ54R	BD14	
FM_D1	BA22	IO,LVDS3A_18P,DQ62R		IO,LVDS3C_18P,DQ54R	BC13	
FLASH_CEn0	BB22	IO,LVDS3A_18N,DQ62R		IO,LVDS3C_18N,DQ54R	BB13	
FLASH_CEn1	BB23	IO,LVDS3A_16P,DQS62R		IO,LVDS3C_16P,DQS54R	BB12	
FLASH_RESETn	BA23	IO,LVDS3A_16N,DQSN62R		IO,LVDS3C_16N,DQSN54R	BB11	
FM_D3	BD21	IO,LVDS3A_19P,DQ63R		IO,LVDS3C_19P,DQ55R	BC16	FMCA_GA0
FM_D5	BD22	IO,LVDS3A_19N,DQ63R		IO,LVDS3C_19N,DQ55R	BB16	
FM_D29	BC19	IO,LVDS3A_20P,DQ63R		IO,LVDS3C_20P,DQ55R	BD17	
FM_D23	BD19	IO,LVDS3A_20N,DQ63R		IO,LVDS3C_20N,DQ55R	BD16	FMCA_GA1
FM_D17	BA19	IO,LVDS3A_21P,DQ63R		IO,LVDS3C_21P,DQ55R	BA15	FMCA_LA_RX_P12
FM_D18	BA20	IO,LVDS3A_21N,DQ63R		IO,LVDS3C_21N,DQ55R	BA14	FMCA_LA_RX_N12
FM_D8	BC21	IO,LVDS3A_23P,DQ63R		IO,LVDS3C_23P,DQ55R	BC18	FMCA_LA_TX_P15
FM_D9	BB21	IO,LVDS3A_23N,DQ63R		IO,LVDS3C_23N,DQ55R	BD18	FMCA_LA_TX_N15
FM_D10	BC20	IO,LVDS3A_24P,DQ63R		IO,LVDS3C_24P,DQ55R	BB17	FMCA_LA_RX_P13
FM_D0	BB20	IO,LVDS3A_24N,DQ63R		IO,LVDS3C_24N,DQ55R	BB18	FMCA_LA_RX_N13
FM_D31	BA17	IO,LVDS3A_22P,DQS63R		IO,LVDS3C_22P,DQS55R	BB15	FMCA_LA_TX_P12
FM_D21	BA18	IO,LVDS3A_22N,DQSN63R		IO,LVDS3C_22N,DQSN55R	BC15	FMCA_LA_TX_N12
		BANK-3B		BANK-3D		
FMCA_LA_RX_P4	AR16	IO,LVDS3B_1P,DQ56R		IO,LVDS3D_1P,DQ48R	AJ11	USB_DATA0
FMCA_LA_RX_N4	AP16	IO,LVDS3B_1N,DQ56R		IO,LVDS3D_1N,DQ48R	AK12	USB_DATA1
FMCA_LA_TX_P11	AU18	IO,LVDS3B_2P,DQ56R		IO,LVDS3D_2P,DQ48R	AL12	FM_A3
FMCA_LA_TX_N11	AT18	IO,LVDS3B_2N,DQ56R		IO,LVDS3D_2N,DQ48R	AL13	FM_A11
FMCA_LA_TX_P3	AT17	IO,LVDS3B_3P,DQ56R		IO,LVDS3D_3P,DQ48R	AK14	FM_A25
FMCA_LA_TX_N3	AU17	IO,LVDS3B_3N,DQ56R		IO,LVDS3D_3N,DQ48R	AJ14	FM_A20
FMCA_LA_TX_P5	AT14	IO,LVDS3B_5P,DQ56R		IO,LVDS3D_5P,DQ48R	AH10	FM_A15
FMCA_LA_TX_N5	AR14	IO,LVDS3B_5N,DQ56R		IO,LVDS3D_5N,DQ48R	AH11	FM_A12
FMCA_LA_RX_P3	AR15	IO,LVDS3B_6P,DQ56R		IO,LVDS3D_6P,DQ48R	AJ12	FM_A19
FMCA_LA_RX_N3	AT15	IO,LVDS3B_6N,DQ56R		IO,LVDS3D_6N,DQ48R	AJ13	FM_A23
FMCA_LA_TX_P6	AR17	IO,LVDS3B_4P,DQS56R		IO,LVDS3D_4P,DQS48R	AH13	FM_A21
FMCA_LA_TX_N6	AP17	IO,LVDS3B_4N,DQSN56R		IO,LVDS3D_4N,DQSN48R	AH14	FM_A18
		FMCA VARIABLE VCCIO DEFAULT 1.8V (1.2V, 1.5V, 1.8V)		VCCIO = 1.8V		
FMCA_LA_RX_P14	AY17	IO,LVDS3B_7P,DQ57R		IO,LVDS3D_7P,DQ49R	AF12	FM_A24
FMCA_LA_RX_N14	AW17	IO,LVDS3B_7N,DQ57R		IO,LVDS3D_7N,DQ49R	AE12	FM_A6
FMCA_LA_RX_P1	AV14	IO,LVDS3B_8P,DQ57R		IO,LVDS3D_8P,DQ49R	AG12	FM_A22
FMCA_LA_RX_N1	AW14	IO,LVDS3B_8N,DQ57R		IO,LVDS3D_8N,DQ49R	AG11	FM_A14
FMCA_LA_TX_P14	AY16	IO,LVDS3B_9P,DQ57R		IO,LVDS3D_9P,DQ49R	AF14	FM_A16
FMCA_LA_TX_N14	AW16	IO,LVDS3B_9N,DQ57R		IO,LVDS3D_9N,DQ49R	AF15	FM_A17
FMCA_LA_RX_P10	AY15	IO,RZQ_3B,LVDS3B_11P,DQ57R		IO,RZQ_3D,LVDS3D_11P,DQ49R	AE14	USB_RESETn
FMCA_LA_RX_N10	AY14	IO,LVDS3B_11N,DQ57R		IO,LVDS3D_11N,DQ49R	AE15	USB_WRn
FMCA_LA_RX_P5	AW18	IO,LVDS3B_14P,DQ58R		IO,LVDS3D_14P,DQ50R	AL15	USB_OEn
FMCA_LA_RX_N5	AV18	IO,LVDS3B_14N,DQ58R		IO,LVDS3D_14N,DQ50R	AK15	USB_RDn
FMCA_LA_TX_P8	AV19	IO,LVDS3B_17P,DQ58R		IO,LVDS3D_17P,DQ50R	AL19	USB_DATA6
FMCA_LA_TX_N8	AW19	IO,LVDS3B_17N,DQ58R		IO,LVDS3D_17N,DQ50R	AL20	USB_DATA7
FMCA_LA_TX_P16	AV20	IO,LVDS3B_18P,DQ58R		IO,LVDS3D_18P,DQ50R	AM17	USB_DATA4
FMCA_LA_TX_N16	AU20	IO,LVDS3B_18N,DQ58R		IO,LVDS3D_18N,DQ50R	AL17	USB_DATA5
FMCA_LA_RX_P7	AU21	IO,LVDS3B_16P,DQS58R		IO,LVDS3D_16P,DQS50R	AM15	USB_ADDR0
FMCA_LA_RX_N7	AV21	IO,LVDS3B_16N,DQSN58R		IO,LVDS3D_16N,DQSN50R	AL14	USB_ADDR1
FMCA_LA_TX_P13	AT19	IO,LVDS3B_19P,DQ59R		IO,LVDS3D_19P,DQ51R	AN11	USB_DATA2
FMCA_LA_TX_N13	AT20	IO,LVDS3B_19N,DQ59R		IO,LVDS3D_19N,DQ51R	AN10	USB_DATA3
FMCA_LA_RX_P11	AP21	IO,LVDS3B_20P,DQ59R		IO,LVDS3D_20P,DQ51R	AL10	FM_A8
FMCA_LA_RX_N11	AR21	IO,LVDS3B_20N,DQ59R		IO,LVDS3D_20N,DQ51R	AK11	FM_A26
FMCA_LA_RX_P2	AP18	IO,LVDS3B_21P,DQ59R		IO,LVDS3D_21P,DQ51R	AN13	FM_A4
FMCA_LA_RX_N2	AN19	IO,LVDS3B_21N,DQ59R		IO,LVDS3D_21N,DQ51R	AM13	FM_A5
FMCA_LA_RX_P0	AR20	IO,LVDS3B_23P,DQ59R		IO,LVDS3D_23P,DQ51R	AP11	FM_A10
FMCA_LA_RX_N0	AR19	IO,LVDS3B_23N,DQ59R		IO,LVDS3D_23N,DQ51R	AR10	FM_A9
FMCA_LA_TX_P0	AR22	IO,LVDS3B_24P,DQ59R		IO,LVDS3D_24P,DQ51R	AM12	FM_A2
FMCA_LA_TX_N0	AT22	IO,LVDS3B_24N,DQ59R		IO,LVDS3D_24N,DQ51R	AM11	FM_A1
FMCA_LA_TX_P1	AN20	IO,LVDS3B_22P,DQS59R		IO,LVDS3D_22P,DQS51R	AN15	FM_A7
FMCA_LA_TX_N1	AP19	IO,LVDS3B_22N,DQSN59R		IO,LVDS3D_22N,DQSN51R	AN14	FM_A13

10AX115F1932C

R352 100, 1%

FLASH/FM BUS

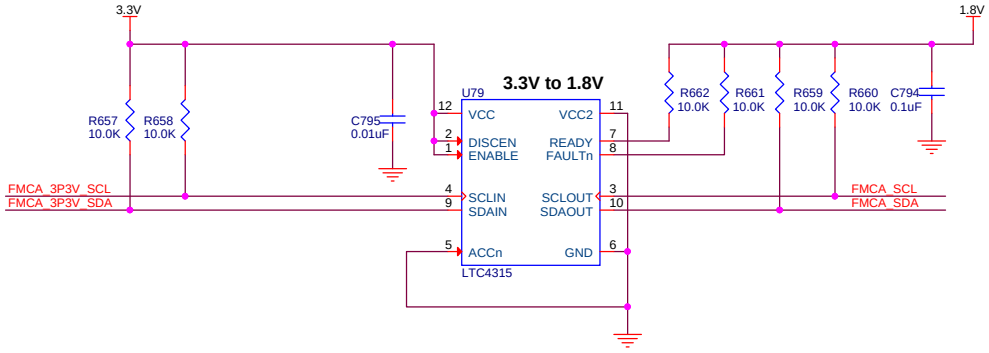
13,14 FM_D[31:0]
13,14 FM_A[26:1]
13,14 FLASH_CLK
13,14 FLASH_RESETn
13,14 FLASH_CEn0
13,14 FLASH_CEn1
13,14 FLASH_OEn
13,14 FLASH_WEn
13,14 FLASH_ADVn
13,14 FLASH_RDYBSYn0

FMC PORT A INTERFACE

19 FMCA_LA_RX_P[14:0]
19 FMCA_LA_RX_N[14:0]
19 FMCA_LA_TX_P[16:0]
19 FMCA_LA_TX_N[16:0]
19 FMCA_GA[1:0]
19 FMCA_3P3V_SDA
19 FMCA_3P3V_SCL

ARRIA 10 USB INTERFACE

26 USB_DATA[7:0]
26 USB_ADDR[1:0]
26 USB_RESETn
26 USB_OEn
26 USB_RDn
26 USB_WRn

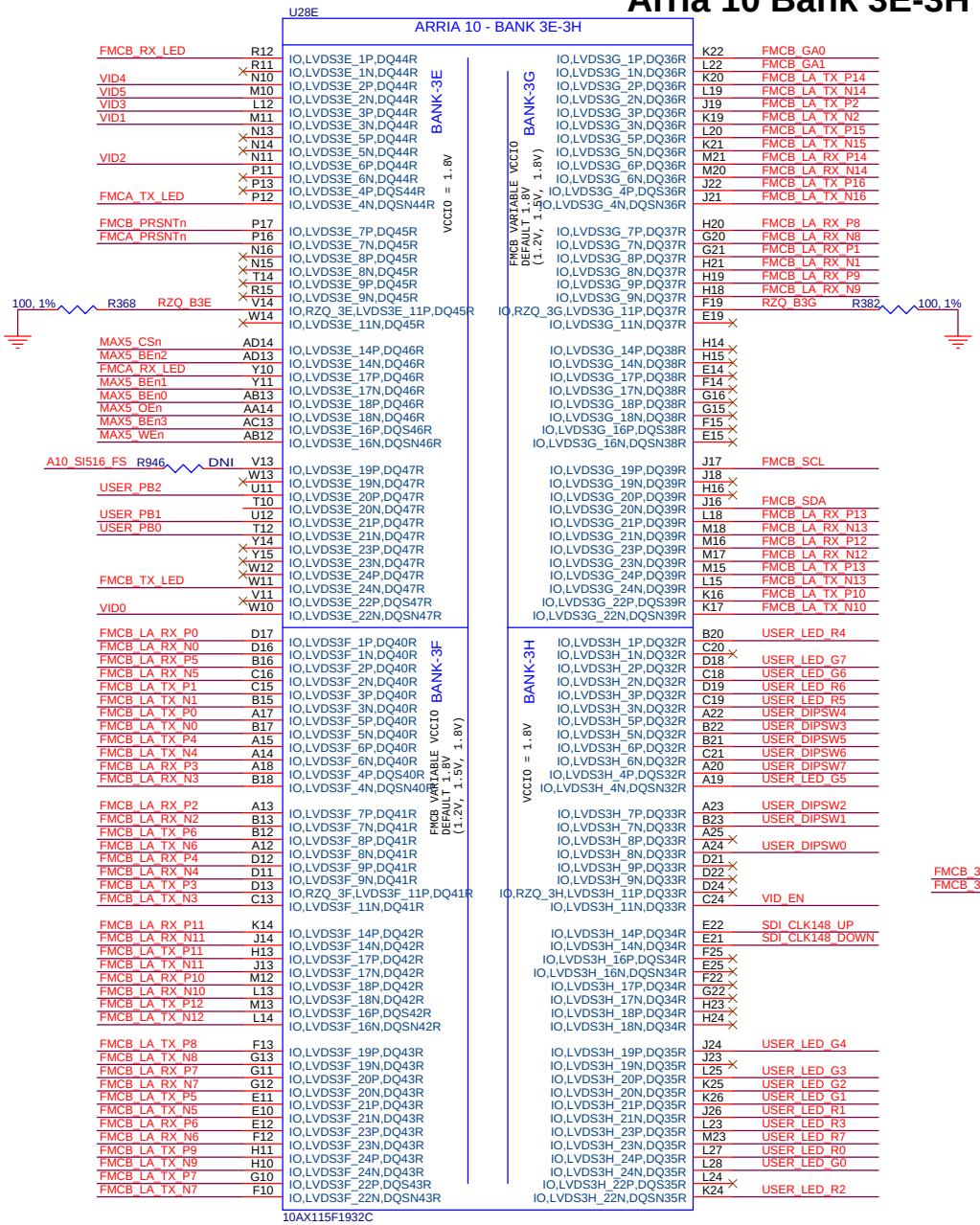


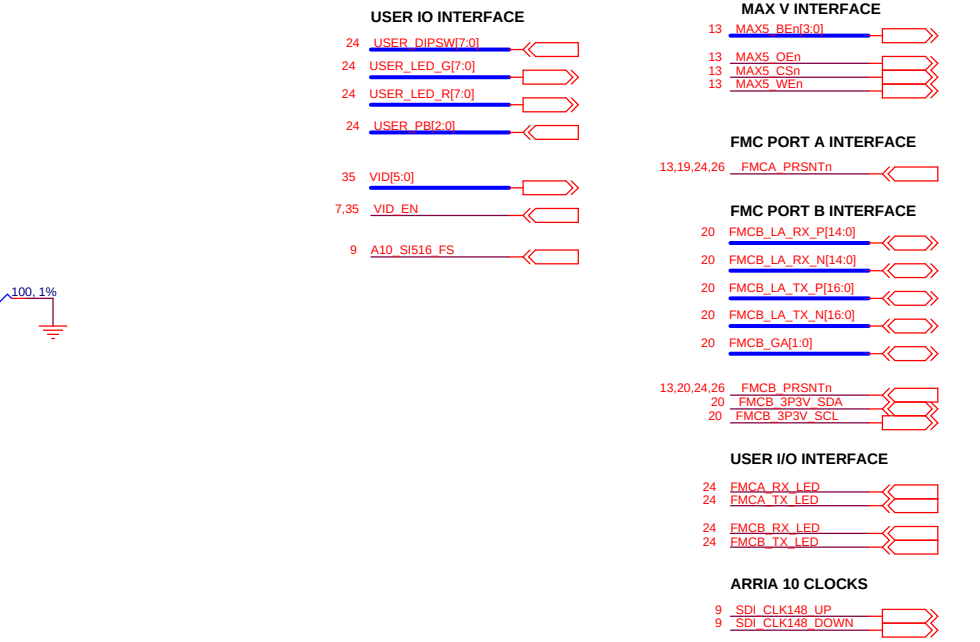
Title: Arria 10 GX FPGA Development Kit

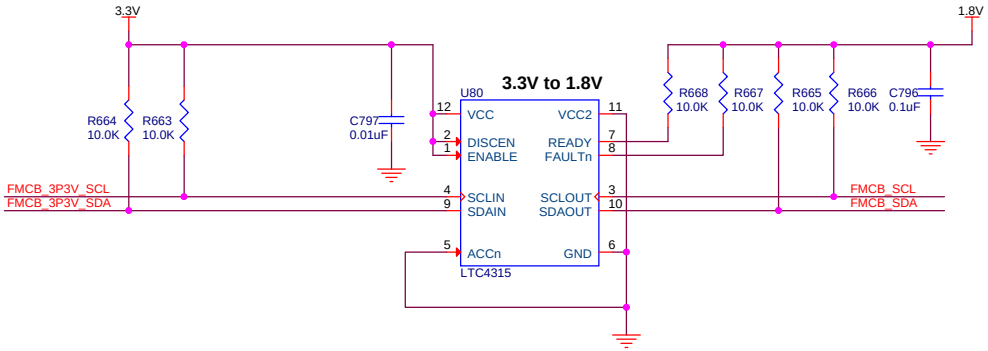
Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 5 of 49

Arria 10 Bank 3E-3H





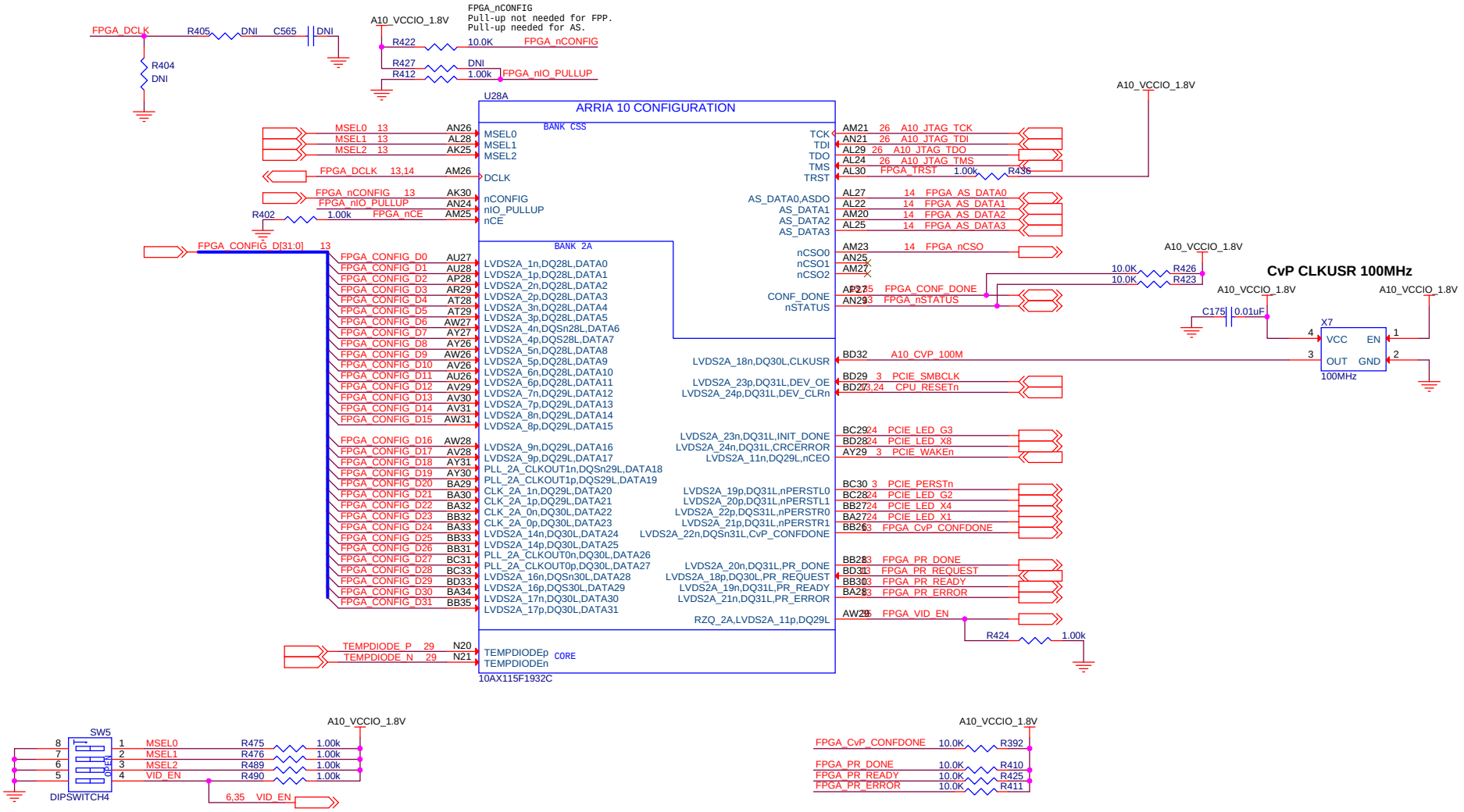


Title: **Arria 10 GX FPGA Development Kit**

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 6 of 49

Arria 10 Configuration



Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 7 of 49

Arria 10 Clocks

U28B

ARRIA 10 CONFIGURATION

BANK-2I — VCCIO = 1.8V

CLK_50	AU33	CLK_2I_0P,DQ14L	PLL_2I_CLKOUT0P,DQ14L	AT32	
	AT33	CLK_2I_0N,DQ14L	PLL_2I_CLKOUT0N,DQ14L	AU32	
R450 100, 1% CLK_FPGA_B2_P	AR36	CLK_2I_1P,DQ13L	PLL_2I_CLKOUT1P,DQS13L	AN33	
CLK_FPGA_B2_N	AR37	CLK_2I_1N,DQ13L	PLL_2I_CLKOUT1N,DQSn13L	AM33	

CAN BE REMOVED FOR ARRIA 10 AND USE OCT ->

BANK-2J — VARIABLE EMI VCCIO (1.2V, 1.35V, 1.5V)

MEM_DQB16	U31	CLK_2J_0P,DQ10L	PLL_2J_CLKOUT0P,DQ10L	W34	MEM_DQB22
MEM_DQB19	V31	CLK_2J_0N,DQ10L	PLL_2J_CLKOUT0N,DQ10L	Y34	MEM_DQB20
MEM_DMB1	AG31	CLK_2J_1P,DQ9L	PLL_2J_CLKOUT1P,DQS9L	AJ32	MEM_DQSB_P1
MEM_DQB15	AH31	CLK_2J_1N,DQ9L	PLL_2J_CLKOUT1N,DQSn9L	AJ31	MEM_DQSB_N1

BANK-2K — VARIABLE EMI VCCIO (1.2V, 1.35V, 1.5V)

MEM_ADDR_CMD10	H31	CLK_2K_0P,DQ6L	PLL_2K_CLKOUT0P,DQ6L	M33	MEM_ADDR_CMD6
MEM_ADDR_CMD11	J31	CLK_2K_0N,DQ6L	PLL_2K_CLKOUT0N,DQ6L	L33	MEM_ADDR_CMD7
R448 100, 1% CLK_EMI_P	F34	CLK_2K_1P,DQ5L	PLL_2K_CLKOUT1P,DQS5L	H33	MEM_ADDR_CMD13
CLK_EMI_N	F35	CLK_2K_1N,DQ5L	PLL_2K_CLKOUT1N,DQSn5L	G32	MEM_ADDR_CMD14

BANK-2L — VARIABLE EMI VCCIO (1.2V, 1.35V, 1.5V)

MEM_DQA20	A30	CLK_2L_0P,DQ2L	PLL_2L_CLKOUT0P,DQ2L	B31	MEM_DQA18
MEM_DMA2	A29	CLK_2L_0N,DQ2L	PLL_2L_CLKOUT0N,DQ2L	B30	MEM_DQA22
MEM_DQA10	G26	CLK_2L_1P,DQ1L	PLL_2L_CLKOUT1P,DQS1L	H28	MEM_DQSA_P1
MEM_DQA11	H26	CLK_2L_1N,DQ1L	PLL_2L_CLKOUT1N,DQSn1L	J27	MEM_DQSA_N1

BANK-3A — VCCIO = 1.8V

R403 100, 1% CLK_125_P	BD24	CLK_3A_0P,DQ62R	PLL_3A_CLKOUT0P,DQ62R	BC23	ENET_TX_P
CLK_125_N	BC24	CLK_3A_0N,DQ62R	PLL_3A_CLKOUT0N,DQ62R	BD23	ENET_TX_N
R406 100, 1% ENET_RX_P	AV24	CLK_3A_1P,DQ61R	PLL_3A_CLKOUT1P,DQS61R	AW23	ENET_RESETn
ENET_RX_N	AW24	CLK_3A_1N,DQ61R	PLL_3A_CLKOUT1N,DQSn61R	AV23	FLASH_RDYBSYn1

CAN BE REMOVED FOR ARRIA 10 AND USE OCT ->

CAN BE REMOVED FOR ARRIA 10 AND USE OCT ->

BANK-3B — FMCA VARIABLE VCCIO DEFAULT 1.8V (1.2V, 1.5V, 1.8V)

R383 100, 1% FMCA_CLK_M2C_P0	AY20	CLK_3B_0P,DQ58R	PLL_3B_CLKOUT0P,DQ58R	AW21	
FMCA_CLK_M2C_N0	AY19	CLK_3B_0N,DQ58R	PLL_3B_CLKOUT0N,DQ58R	AY21	
R369 100, 1% FMCA_LA_RX_CLK_P0	AV15	CLK_3B_1P,DQ57R	PLL_3B_CLKOUT1P,DQS57R	AV16	
FMCA_LA_RX_CLK_N0	AU15	CLK_3B_1N,DQ57R	PLL_3B_CLKOUT1N,DQSn57R	AU16	

BANK-3C — FMCA VARIABLE VCCIO DEFAULT 1.8V (1.2V, 1.5V, 1.8V)

R353 100, 1% FMCA_CLK_M2C_P1	BA12	CLK_3C_0P,DQ54R	PLL_3C_CLKOUT0P,DQ54R	BB10	
FMCA_CLK_M2C_N1	BA13	CLK_3C_0N,DQ54R	PLL_3C_CLKOUT0N,DQ54R	BA10	
R336 100, 1% FMCA_LA_RX_CLK_P1	AT10	CLK_3C_1P,DQ53R	PLL_3C_CLKOUT1P,DQS53R	AP12	
FMCA_LA_RX_CLK_N1	AR11	CLK_3C_1N,DQ53R	PLL_3C_CLKOUT1N,DQSn53R	AR12	

BANK-3D — VCCIO = 1.8V

USB_FPGA_CLK	AM18	CLK_3D_0P,DQ50R	PLL_3D_CLKOUT0P,DQ50R	AM16	USB_FULL
ENET_MDIO	AL18	CLK_3D_0N,DQ50R	PLL_3D_CLKOUT0N,DQ50R	AN16	USB_EMPTY
ENET_MDC	AF13	CLK_3D_1P,DQ49R	PLL_3D_CLKOUT1P,DQS49R	AE11	USB_SCL
ENET_INTn	AG13	CLK_3D_1N,DQ49R	PLL_3D_CLKOUT1N,DQSn49R	AD12	USB_SDA

BANK-3E — VCCIO = 1.8V

MAX5_CLK	AB11	CLK_3E_0P,DQ46R	PLL_3E_CLKOUT0P,DQ46R	AA13	S5_MSEL4
S5_MSEL3	AC11	CLK_3E_0N,DQ46R	PLL_3E_CLKOUT0N,DQ46R	Y12	STRATIX V MSEL PINS.
R14	U13	CLK_3E_1P,DQ45R	PLL_3E_CLKOUT1P,DQS45R	T13	CAN BE DELETED IN REV B
P14		CLK_3E_1N,DQ45R	PLL_3E_CLKOUT1N,DQSn45R		

S5_MSEL3 — R305 DNI / R307 1.00k — A10_VCCIO_1.8V — R306 1.00k / R308 DNI

BANK-3F — FMCB VARIABLE VCCIO DEFAULT 1.8V (1.2V, 1.5V, 1.8V)

R349 100, 1% FMCB_CLK_M2C_P0	J12	CLK_3F_0P,DQ42R	PLL_3F_CLKOUT0P,DQ42R	K11	
FMCB_CLK_M2C_N0	K12	CLK_3F_0N,DQ42R	PLL_3F_CLKOUT0N,DQ42R	J11	
R333 100, 1% FMCB_LA_RX_CLK_P0	C11	CLK_3F_1P,DQ41R	PLL_3F_CLKOUT1P,DQS41R	C14	
FMCB_LA_RX_CLK_N0	C10	CLK_3F_1N,DQ41R	PLL_3F_CLKOUT1N,DQSn41R	D14	

BANK-3G — FMCB VARIABLE VCCIO DEFAULT 1.8V (1.2V, 1.5V, 1.8V)

R378 100, 1% FMCB_CLK_M2C_P1	F17	CLK_3G_0P,DQ38R	PLL_3G_CLKOUT0P,DQ38R	E16	
FMCB_CLK_M2C_N1	G17	CLK_3G_0N,DQ38R	PLL_3G_CLKOUT0N,DQ38R	E17	
R379 100, 1% FMCB_LA_RX_CLK_P1	G18	CLK_3G_1P,DQ37R	PLL_3G_CLKOUT1P,DQS37R	E20	
FMCB_LA_RX_CLK_N1	F18	CLK_3G_1N,DQ37R	PLL_3G_CLKOUT1N,DQSn37R	F20	

BANK-3H — VCCIO = 1.8V

R391 100, 1% CLK_FPGA_B3_P	F23	CLK_3H_0P,DQ34R	PLL_3H_CLKOUT0P,DQ34R	E24	SMA_CLK_OUT
CLK_FPGA_B3_N	G23	CLK_3H_0N,DQ34R	PLL_3H_CLKOUT0N,DQ34R	F24	
C23	C25	CLK_3H_1P,DQ33R	PLL_3H_CLKOUT1P,DQS33R	C25	
D23		CLK_3H_1N,DQ33R	PLL_3H_CLKOUT1N,DQSn33R	B25	

CAN BE REMOVED FOR ARRIA 10 AND USE OCT ->

10AX115F1932C

1 — J7 — 2 3 4 5 — SMA_CLK_OUT

ETHERNET INTERFACE
15 ENET_RX_P
15 ENET_RX_N
15 ENET_TX_P
15 ENET_TX_N
15 ENET_RESETn
15 ENET_MDIO
15 ENET_MDC
15 ENET_INTn

MEMORY INTERFACE
4,17 MEM_ADDR_CMD[31:0]
4,17 MEM_DMA[3:0]
4,17 MEM_DQA[33:0]
4,17 MEM_DQSA_P[3:0]
4,17 MEM_DQSA_N[3:0]
4,17 MEM_DMB[3:0]
4,17 MEM_DQB[33:0]
4,17 MEM_DQSB_P[3:0]
4,17 MEM_DQSB_N[3:0]

ARRIA 10 CLOCKS
9 CLK_50
9 CLK_125_P
9 CLK_125_N
9 CLK_FPGA_B2_P
9 CLK_FPGA_B2_N
9 CLK_FPGA_B3_P
9 CLK_FPGA_B3_N
10 CLK_EMI_P
10 CLK_EMI_N

FLASH INTERFACE
13,14 FLASH_RDYBSYn1

FMC PORT A INTERFACE
19 FMCA_CLK_M2C_P[1:0]
19 FMCA_CLK_M2C_N[1:0]
19 FMCA_LA_RX_CLK_P[1:0]
19 FMCA_LA_RX_CLK_N[1:0]

FMC PORT B INTERFACE
20 FMCB_CLK_M2C_P[1:0]
20 FMCB_CLK_M2C_N[1:0]
20 FMCB_LA_RX_CLK_P[1:0]
20 FMCB_LA_RX_CLK_N[1:0]

ARRIA 10 USB INTERFACE
25 USB_FPGA_CLK
26 USB_FULL
26 USB_EMPTY
26 USB_SCL
26 USB_SDA

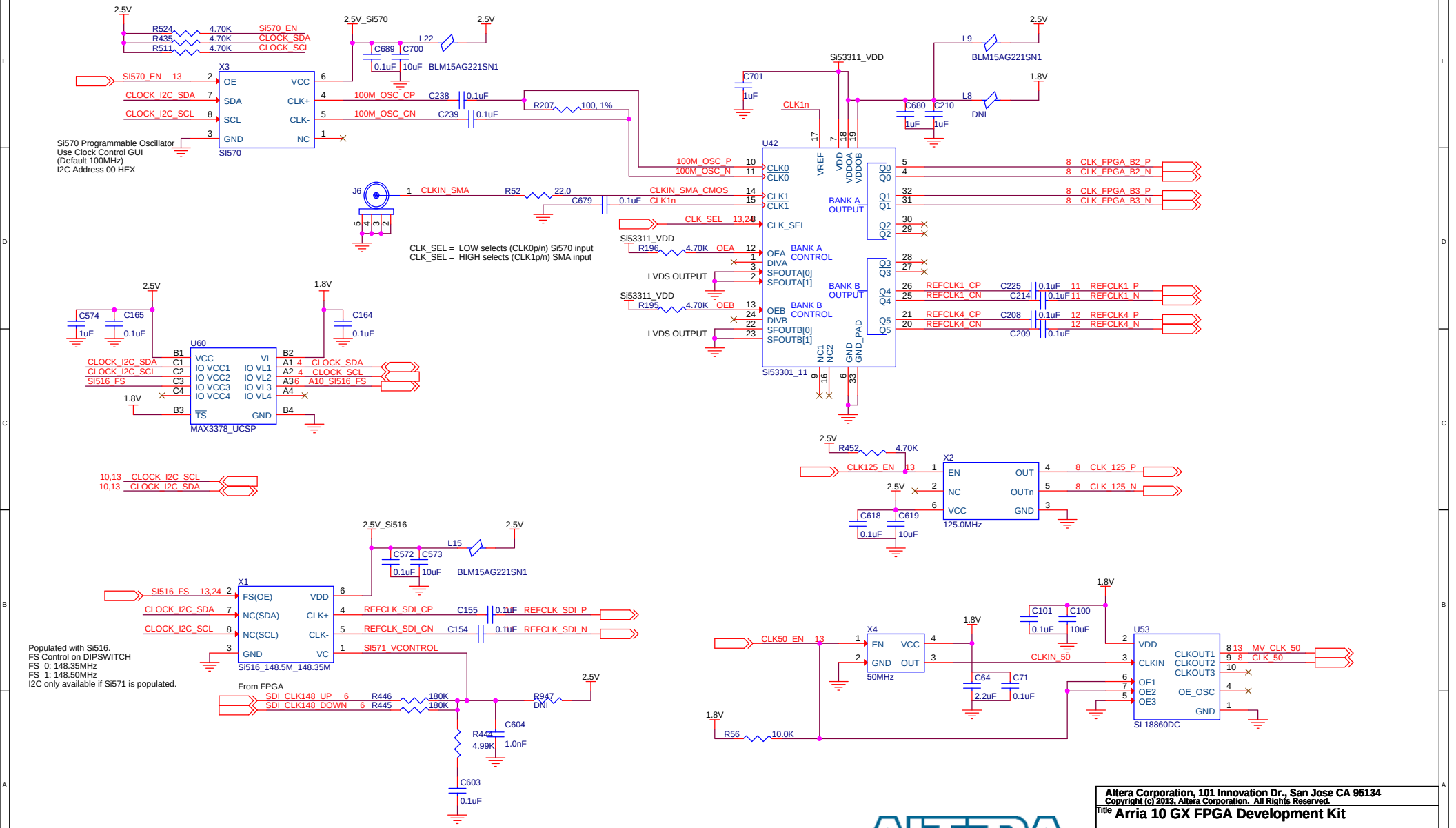
MAX V INTERFACE
13 MAX5_CLK

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 8 of 49

Clocks

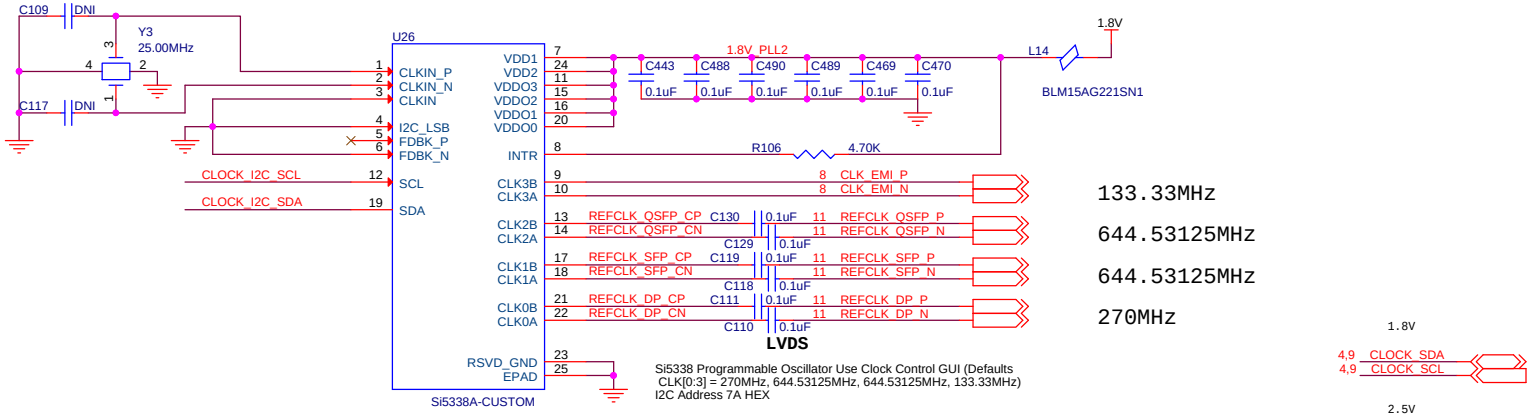


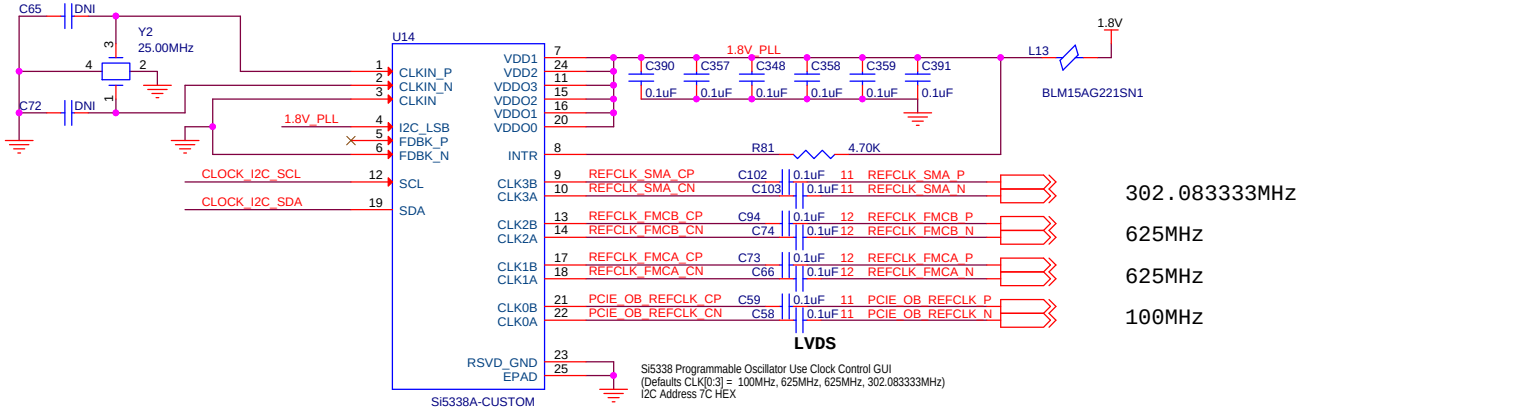
Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 9 of 49

PLL (2)





1.8V
4,9 CLOCK_SDA
4,9 CLOCK_SCL
2.5V
9,13 CLOCK_I2C_SCL
9,13 CLOCK_I2C_SDA

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 10 of 49

Arria 10 Transceivers Left

U28F

ARRIA 10 - LEFT TRANSCEIVER BANK-1C

	AW38	GXBL1C_RX_CH0P,GXBL1C_REFCLK0P	GXBL1C_TX_CH0P	BC38	
	AW37	GXBL1C_RX_CH0N,GXBL1C_REFCLK0N	GXBL1C_TX_CH0N	BC37	
	BA38	GXBL1C_RX_CH1P,GXBL1C_REFCLK1P	GXBL1C_TX_CH1P	BD40	
	BA37	GXBL1C_RX_CH1N,GXBL1C_REFCLK1N	GXBL1C_TX_CH1N	BD39	
	AY40	GXBL1C_RX_CH2P,GXBL1C_REFCLK2P	GXBL1C_TX_CH2P	BB40	
	AY39	GXBL1C_RX_CH2N,GXBL1C_REFCLK2N	GXBL1C_TX_CH2N	BB39	
	AV40	GXBL1C_RX_CH3P,GXBL1C_REFCLK3P	GXBL1C_TX_CH3P	BC42	
	AV39	GXBL1C_RX_CH3N,GXBL1C_REFCLK3N	GXBL1C_TX_CH3N	BC41	
PCIE_RX_P0	AT40	GXBL1C_RX_CH4P,GXBL1C_REFCLK4P	GXBL1C_TX_CH4P	BB44	PCIE_TX_P0
PCIE_RX_N0	AT39	GXBL1C_RX_CH4N,GXBL1C_REFCLK4N	GXBL1C_TX_CH4N	BB43	PCIE_TX_N0
PCIE_RX_P1	AP40	GXBL1C_RX_CH5P,GXBL1C_REFCLK5P	GXBL1C_TX_CH5P	BA42	PCIE_TX_P1
PCIE_RX_N1	AP39	GXBL1C_RX_CH5N,GXBL1C_REFCLK5N	GXBL1C_TX_CH5N	BA41	PCIE_TX_N1
PCIE_EDGE_REFCLK_P	AL37	REFCLK_GXBL1C_CHTP			
PCIE_EDGE_REFCLK_N	AL38	REFCLK_GXBL1C_CHTN			
PCIE_OB_REFCLK_P	AN37	REFCLK_GXBL1C_CHBP			
PCIE_OB_REFCLK_N	AN38	REFCLK_GXBL1C_CHBN			

10AX115F1932C

U28G

ARRIA 10 - LEFT TRANSCEIVER BANK-1D

PCIE_RX_P2	AN42	GXBL1D_RX_CH0P,GXBL1D_REFCLK0P	GXBL1D_TX_CH0P	AY44	PCIE_TX_P2
PCIE_RX_N2	AN41	GXBL1D_RX_CH0N,GXBL1D_REFCLK0N	GXBL1D_TX_CH0N	AY43	PCIE_TX_N2
PCIE_RX_P3	AM40	GXBL1D_RX_CH1P,GXBL1D_REFCLK1P	GXBL1D_TX_CH1P	AW42	PCIE_TX_P3
PCIE_RX_N3	AM39	GXBL1D_RX_CH1N,GXBL1D_REFCLK1N	GXBL1D_TX_CH1N	AW41	PCIE_TX_N3
PCIE_RX_P4	AL42	GXBL1D_RX_CH2P,GXBL1D_REFCLK2P	GXBL1D_TX_CH2P	AV44	PCIE_TX_P4
PCIE_RX_N4	AL41	GXBL1D_RX_CH2N,GXBL1D_REFCLK2N	GXBL1D_TX_CH2N	AV43	PCIE_TX_N4
PCIE_RX_P5	AK40	GXBL1D_RX_CH3P,GXBL1D_REFCLK3P	GXBL1D_TX_CH3P	AU42	PCIE_TX_P5
PCIE_RX_N5	AK39	GXBL1D_RX_CH3N,GXBL1D_REFCLK3N	GXBL1D_TX_CH3N	AU41	PCIE_TX_N5
PCIE_RX_P6	AJ42	GXBL1D_RX_CH4P,GXBL1D_REFCLK4P	GXBL1D_TX_CH4P	AT44	PCIE_TX_P6
PCIE_RX_N6	AJ41	GXBL1D_RX_CH4N,GXBL1D_REFCLK4N	GXBL1D_TX_CH4N	AT43	PCIE_TX_N6
PCIE_RX_P7	AH40	GXBL1D_RX_CH5P,GXBL1D_REFCLK5P	GXBL1D_TX_CH5P	AR42	PCIE_TX_P7
PCIE_RX_N7	AH39	GXBL1D_RX_CH5N,GXBL1D_REFCLK5N	GXBL1D_TX_CH5N	AR41	PCIE_TX_N7
REFCLK1_P	AG37	REFCLK_GXBL1D_CHTP			
REFCLK1_N	AG38	REFCLK_GXBL1D_CHTN			
10.0K R464	AJ37	REFCLK_GXBL1D_CHBP			
	AJ38	REFCLK_GXBL1D_CHBN			

10AX115F1932C

U28H

ARRIA 10 - LEFT TRANSCEIVER BANK-1E

	AG42	GXBL1E_RX_CH0P,GXBL1E_REFCLK0P	GXBL1E_TX_CH0P	AP44	DP_ML_LANE_P0
	AG41	GXBL1E_RX_CH0N,GXBL1E_REFCLK0N	GXBL1E_TX_CH0N	AP43	DP_ML_LANE_N0
	AF40	GXBL1E_RX_CH1P,GXBL1E_REFCLK1P	GXBL1E_TX_CH1P	AM44	DP_ML_LANE_P1
	AF39	GXBL1E_RX_CH1N,GXBL1E_REFCLK1N	GXBL1E_TX_CH1N	AM43	DP_ML_LANE_N1
	AE42	GXBL1E_RX_CH2P,GXBL1E_REFCLK2P	GXBL1E_TX_CH2P	AK44	
	AE41	GXBL1E_RX_CH2N,GXBL1E_REFCLK2N	GXBL1E_TX_CH2N	AK43	
	AD40	GXBL1E_RX_CH3P,GXBL1E_REFCLK3P	GXBL1E_TX_CH3P	AH44	DP_ML_LANE_P2
	AD39	GXBL1E_RX_CH3N,GXBL1E_REFCLK3N	GXBL1E_TX_CH3N	AH43	DP_ML_LANE_N2
	AC42	GXBL1E_RX_CH4P,GXBL1E_REFCLK4P	GXBL1E_TX_CH4P	AF44	DP_ML_LANE_P3
	AC41	GXBL1E_RX_CH4N,GXBL1E_REFCLK4N	GXBL1E_TX_CH4N	AF43	DP_ML_LANE_N3
	AB40	GXBL1E_RX_CH5P,GXBL1E_REFCLK5P	GXBL1E_TX_CH5P	AD44	
	AB39	GXBL1E_RX_CH5N,GXBL1E_REFCLK5N	GXBL1E_TX_CH5N	AD43	
REFCLK_DP_P	AC37	REFCLK_GXBL1E_CHTP			
REFCLK_DP_N	AC38	REFCLK_GXBL1E_CHTN			
10.0K R463	AE37	REFCLK_GXBL1E_CHBP			
	AE38	REFCLK_GXBL1E_CHBN			

10AX115F1932C

U28I

ARRIA 10 - LEFT TRANSCEIVER BANK-1F

SFP_RX_P	AA42	GXBL1F_RX_CH0P,GXBL1F_REFCLK0P	GXBL1F_TX_CH0P	AB44	SFP_TX_P
SFP_RX_N	AA41	GXBL1F_RX_CH0N,GXBL1F_REFCLK0N	GXBL1F_TX_CH0N	AB43	SFP_TX_N
	W42	GXBL1F_RX_CH1P,GXBL1F_REFCLK1P	GXBL1F_TX_CH1P	Y44	
	W41	GXBL1F_RX_CH1N,GXBL1F_REFCLK1N	GXBL1F_TX_CH1N	Y43	
	Y40	GXBL1F_RX_CH2P,GXBL1F_REFCLK2P	GXBL1F_TX_CH2P	V44	
	Y39	GXBL1F_RX_CH2N,GXBL1F_REFCLK2N	GXBL1F_TX_CH2N	V43	
	V40	GXBL1F_RX_CH3P,GXBL1F_REFCLK3P	GXBL1F_TX_CH3P	T44	
	V39	GXBL1F_RX_CH3N,GXBL1F_REFCLK3N	GXBL1F_TX_CH3N	T43	
	U42	GXBL1F_RX_CH4P,GXBL1F_REFCLK4P	GXBL1F_TX_CH4P	P44	
	U41	GXBL1F_RX_CH4N,GXBL1F_REFCLK4N	GXBL1F_TX_CH4N	P43	
	T40	GXBL1F_RX_CH5P,GXBL1F_REFCLK5P	GXBL1F_TX_CH5P	M44	
	T39	GXBL1F_RX_CH5N,GXBL1F_REFCLK5N	GXBL1F_TX_CH5N	M43	
10.0K R462	W37	REFCLK_GXBL1F_CHTP			
	W38	REFCLK_GXBL1F_CHTN			
REFCLK_SFP_P	AA37	REFCLK_GXBL1F_CHBP			
REFCLK_SFP_N	AA38	REFCLK_GXBL1F_CHBN			

10AX115F1932C

U28J

ARRIA 10 - LEFT TRANSCEIVER BANK-1G

QSFP_RX_P0	R42	GXBL1G_RX_CH0P,GXBL1G_REFCLK0P	GXBL1G_TX_CH0P	K44	QSFP_TX_P0
QSFP_RX_N0	R41	GXBL1G_RX_CH0N,GXBL1G_REFCLK0N	GXBL1G_TX_CH0N	K43	QSFP_TX_N0
QSFP_RX_P1	P40	GXBL1G_RX_CH1P,GXBL1G_REFCLK1P	GXBL1G_TX_CH1P	J42	QSFP_TX_P1
QSFP_RX_N1	P39	GXBL1G_RX_CH1N,GXBL1G_REFCLK1N	GXBL1G_TX_CH1N	J41	QSFP_TX_N1
	N42	GXBL1G_RX_CH2P,GXBL1G_REFCLK2P	GXBL1G_TX_CH2P	H44	
	N41	GXBL1G_RX_CH2N,GXBL1G_REFCLK2N	GXBL1G_TX_CH2N	H43	
QSFP_RX_P2	M40	GXBL1G_RX_CH3P,GXBL1G_REFCLK3P	GXBL1G_TX_CH3P	G42	QSFP_TX_P2
QSFP_RX_N2	M39	GXBL1G_RX_CH3N,GXBL1G_REFCLK3N	GXBL1G_TX_CH3N	G41	QSFP_TX_N2
QSFP_RX_P3	L42	GXBL1G_RX_CH4P,GXBL1G_REFCLK4P	GXBL1G_TX_CH4P	F44	QSFP_TX_P3
QSFP_RX_N3	L41	GXBL1G_RX_CH4N,GXBL1G_REFCLK4N	GXBL1G_TX_CH4N	F43	QSFP_TX_N3
	K40	GXBL1G_RX_CH5P,GXBL1G_REFCLK5P	GXBL1G_TX_CH5P	E42	
	K39	GXBL1G_RX_CH5N,GXBL1G_REFCLK5N	GXBL1G_TX_CH5N	E41	
REFCLK_QSFP_P	R37	REFCLK_GXBL1G_CHTP			
REFCLK_QSFP_N	R38	REFCLK_GXBL1G_CHTN			
10.0K R461	U37	REFCLK_GXBL1G_CHBP			
	U38	REFCLK_GXBL1G_CHBN			

10AX115F1932C

U28K

ARRIA 10 - LEFT TRANSCEIVER BANK-1H

SDI_RX_P	H40	GXBL1H_RX_CH0P,GXBL1H_REFCLK0P	GXBL1H_TX_CH0P	D44	SDI_TX_P
SDI_RX_N	H39	GXBL1H_RX_CH0N,GXBL1H_REFCLK0N	GXBL1H_TX_CH0N	D43	SDI_TX_N
	G38	GXBL1H_RX_CH1P,GXBL1H_REFCLK1P	GXBL1H_TX_CH1P	C42	SMA_TX_P
	G37	GXBL1H_RX_CH1N,GXBL1H_REFCLK1N	GXBL1H_TX_CH1N	C41	SMA_TX_N
	F40	GXBL1H_RX_CH2P,GXBL1H_REFCLK2P	GXBL1H_TX_CH2P	B44	
	F39	GXBL1H_RX_CH2N,GXBL1H_REFCLK2N	GXBL1H_TX_CH2N	B43	
	E38	GXBL1H_RX_CH3P,GXBL1H_REFCLK3P	GXBL1H_TX_CH3P	A42	
	E37	GXBL1H_RX_CH3N,GXBL1H_REFCLK3N	GXBL1H_TX_CH3N	A41	
	D40	GXBL1H_RX_CH4P,GXBL1H_REFCLK4P	GXBL1H_TX_CH4P	B40	
	D39	GXBL1H_RX_CH4N,GXBL1H_REFCLK4N	GXBL1H_TX_CH4N	B39	
	C38	GXBL1H_RX_CH5P,GXBL1H_REFCLK5P	GXBL1H_TX_CH5P	A38	
	C37	GXBL1H_RX_CH5N,GXBL1H_REFCLK5N	GXBL1H_TX_CH5N	A37	
REFCLK_SDI_P	L37	REFCLK_GXBL1H_CHTP			
REFCLK_SDI_N	L38	REFCLK_GXBL1H_CHTN			
REFCLK_SMA_P	N37	REFCLK_GXBL1H_CHBP			
REFCLK_SMA_N	N38	REFCLK_GXBL1H_CHBN			

10AX115F1932C

9	REFCLK1_P	
9	REFCLK1_N	
PCIe INTERFACE		
3	PCIE_RX_P[7:0]	
3	PCIE_RX_N[7:0]	
3	PCIE_TX_P[7:0]	
3	PCIE_TX_N[7:0]	
3	PCIE_EDGE_REFCLK_P	
3	PCIE_EDGE_REFCLK_N	
10	PCIE_OB_REFCLK_P	
10	PCIE_OB_REFCLK_N	
DISPLAYPORT INTERFACE		
18	DP_ML_LANE_P[3:0]	
18	DP_ML_LANE_N[3:0]	
10	REFCLK_DP_P	
10	REFCLK_DP_N	
SDI INTERFACE		
9	REFCLK_SDI_P	
9	REFCLK_SDI_N	
23	SDI_RX_P	
23	SDI_RX_N	
23	SDI_TX_P	
23	SDI_TX_N	
QSFP INTERFACE		
21	QSFP_RX_P[3:0]	
21	QSFP_RX_N[3:0]	
21	QSFP_TX_P[3:0]	
21	QSFP_TX_N[3:0]	
10	REFCLK_QSFP_P	
10	REFCLK_QSFP_N	
SFP+ INTERFACE		
22	SFP_RX_P	
22	SFP_RX_N	
22	SFP_TX_P	
22	SFP_TX_N	
10	REFCLK_SFP_P	
10	REFCLK_SFP_N	
SMA INTERFACE		
10	REFCLK_SMA_P	
10	REFCLK_SMA_N	

J16, J15

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 11 of 49

Arria 10 Transceivers Right

U28L

ARRIA 10 - RIGHT TRANSCEIVER BANK-4C

FMCA_DP_M2C_P0 AW7
FMCA_DP_M2C_N0 AW8
GXBR4C_RX_CH0P, GXBR4C_REFCLK0P
GXBR4C_RX_CH0N, GXBR4C_REFCLK0N
GXBR4C_TX_CH0P BC7 FMCA_DP_C2M_P0
GXBR4C_TX_CH0N BC8 FMCA_DP_C2M_N0

FMCA_DP_M2C_P1 BA7
FMCA_DP_M2C_N1 BA8
GXBR4C_RX_CH1P, GXBR4C_REFCLK1P
GXBR4C_RX_CH1N, GXBR4C_REFCLK1N
GXBR4C_TX_CH1P BD5 FMCA_DP_C2M_P1
GXBR4C_TX_CH1N BD6 FMCA_DP_C2M_N1

FMCA_DP_M2C_P2 AY5
FMCA_DP_M2C_N2 AY6
GXBR4C_RX_CH2P, GXBR4C_REFCLK2P
GXBR4C_RX_CH2N, GXBR4C_REFCLK2N
GXBR4C_TX_CH2P BB5 FMCA_DP_C2M_P2
GXBR4C_TX_CH2N BB6 FMCA_DP_C2M_N2

FMCA_DP_M2C_P3 AV5
FMCA_DP_M2C_N3 AV6
GXBR4C_RX_CH3P, GXBR4C_REFCLK3P
GXBR4C_RX_CH3N, GXBR4C_REFCLK3N
GXBR4C_TX_CH3P BC3 FMCA_DP_C2M_P3
GXBR4C_TX_CH3N BC4 FMCA_DP_C2M_N3

FMCA_DP_M2C_P4 AT5
FMCA_DP_M2C_N4 AT6
GXBR4C_RX_CH4P, GXBR4C_REFCLK4P
GXBR4C_RX_CH4N, GXBR4C_REFCLK4N
GXBR4C_TX_CH4P BB1 FMCA_DP_C2M_P4
GXBR4C_TX_CH4N BB2 FMCA_DP_C2M_N4

FMCA_DP_M2C_P5 AP5
FMCA_DP_M2C_N5 AP6
GXBR4C_RX_CH5P, GXBR4C_REFCLK5P
GXBR4C_RX_CH5N, GXBR4C_REFCLK5N
GXBR4C_TX_CH5P BA3 FMCA_DP_C2M_P5
GXBR4C_TX_CH5N BA4 FMCA_DP_C2M_N5

FMCA_GBTCLK_M2C_P0 AL8
FMCA_GBTCLK_M2C_N0 AL7
REFCLK_GXBR4C_CHTP
REFCLK_GXBR4C_CHTN

REFCLK_FMCA_P AN8
REFCLK_FMCA_N AN7
REFCLK_GXBR4C_CHBP
REFCLK_GXBR4C_CHBN

10AX115F1932C

U28O

ARRIA 10 - RIGHT TRANSCEIVER BANK-4F

FMCB_DP_M2C_P0 AA3
FMCB_DP_M2C_N0 AA4
GXBR4F_RX_CH0P, GXBR4F_REFCLK0P
GXBR4F_RX_CH0N, GXBR4F_REFCLK0N
GXBR4F_TX_CH0P AB1 FMCB_DP_C2M_P0
GXBR4F_TX_CH0N AB2 FMCB_DP_C2M_N0

FMCB_DP_M2C_P1 W3
FMCB_DP_M2C_N1 W4
GXBR4F_RX_CH1P, GXBR4F_REFCLK1P
GXBR4F_RX_CH1N, GXBR4F_REFCLK1N
GXBR4F_TX_CH1P Y1 FMCB_DP_C2M_P1
GXBR4F_TX_CH1N Y2 FMCB_DP_C2M_N1

FMCB_DP_M2C_P2 Y5
FMCB_DP_M2C_N2 Y6
GXBR4F_RX_CH2P, GXBR4F_REFCLK2P
GXBR4F_RX_CH2N, GXBR4F_REFCLK2N
GXBR4F_TX_CH2P V1 FMCB_DP_C2M_P2
GXBR4F_TX_CH2N V2 FMCB_DP_C2M_N2

FMCB_DP_M2C_P3 V5
FMCB_DP_M2C_N3 V6
GXBR4F_RX_CH3P, GXBR4F_REFCLK3P
GXBR4F_RX_CH3N, GXBR4F_REFCLK3N
GXBR4F_TX_CH3P T1 FMCB_DP_C2M_P3
GXBR4F_TX_CH3N T2 FMCB_DP_C2M_N3

FMCB_DP_M2C_P4 U3
FMCB_DP_M2C_N4 U4
GXBR4F_RX_CH4P, GXBR4F_REFCLK4P
GXBR4F_RX_CH4N, GXBR4F_REFCLK4N
GXBR4F_TX_CH4P P1 FMCB_DP_C2M_P4
GXBR4F_TX_CH4N P2 FMCB_DP_C2M_N4

FMCB_DP_M2C_P5 T5
FMCB_DP_M2C_N5 T6
GXBR4F_RX_CH5P, GXBR4F_REFCLK5P
GXBR4F_RX_CH5N, GXBR4F_REFCLK5N
GXBR4F_TX_CH5P M1 FMCB_DP_C2M_P5
GXBR4F_TX_CH5N M2 FMCB_DP_C2M_N5

FMCB_GBTCLK_M2C_P0 W8
FMCB_GBTCLK_M2C_N0 W7
REFCLK_GXBR4F_CHTP
REFCLK_GXBR4F_CHTN

REFCLK_FMCB_P AA8
REFCLK_FMCB_N AA7
REFCLK_GXBR4F_CHBP
REFCLK_GXBR4F_CHBN

10AX115F1932C

9 REFCLK4_P
9 REFCLK4_N

FMC INTERFACE

19 FMCA_DP_M2C_P[15:0]
19 FMCA_DP_M2C_N[15:0]
19 FMCA_DP_C2M_P[15:0]
19 FMCA_DP_C2M_N[15:0]
19 FMCA_GBTCLK_M2C_P[1:0]
19 FMCA_GBTCLK_M2C_N[1:0]

20 FMCB_DP_M2C_P[15:0]
20 FMCB_DP_M2C_N[15:0]
20 FMCB_DP_C2M_P[15:0]
20 FMCB_DP_C2M_N[15:0]
20 FMCB_GBTCLK_M2C_P[1:0]
20 FMCB_GBTCLK_M2C_N[1:0]

U28M

ARRIA 10 - RIGHT TRANSCEIVER BANK-4D

FMCA_DP_M2C_P6 AN3
FMCA_DP_M2C_N6 AN4
GXBR4D_RX_CH0P, GXBR4D_REFCLK0P
GXBR4D_RX_CH0N, GXBR4D_REFCLK0N
GXBR4D_TX_CH0P AY1 FMCA_DP_C2M_P6
GXBR4D_TX_CH0N AY2 FMCA_DP_C2M_N6

FMCA_DP_M2C_P7 AM5
FMCA_DP_M2C_N7 AM6
GXBR4D_RX_CH1P, GXBR4D_REFCLK1P
GXBR4D_RX_CH1N, GXBR4D_REFCLK1N
GXBR4D_TX_CH1P AW3 FMCA_DP_C2M_P7
GXBR4D_TX_CH1N AW4 FMCA_DP_C2M_N7

FMCA_DP_M2C_P8 AL3
FMCA_DP_M2C_N8 AL4
GXBR4D_RX_CH2P, GXBR4D_REFCLK2P
GXBR4D_RX_CH2N, GXBR4D_REFCLK2N
GXBR4D_TX_CH2P AV1 FMCA_DP_C2M_P8
GXBR4D_TX_CH2N AV2 FMCA_DP_C2M_N8

FMCA_DP_M2C_P9 AK5
FMCA_DP_M2C_N9 AK6
GXBR4D_RX_CH3P, GXBR4D_REFCLK3P
GXBR4D_RX_CH3N, GXBR4D_REFCLK3N
GXBR4D_TX_CH3P AU3 FMCA_DP_C2M_P9
GXBR4D_TX_CH3N AU4 FMCA_DP_C2M_N9

FMCA_DP_M2C_P10 AJ3
FMCA_DP_M2C_N10 AJ4
GXBR4D_RX_CH4P, GXBR4D_REFCLK4P
GXBR4D_RX_CH4N, GXBR4D_REFCLK4N
GXBR4D_TX_CH4P AT1 FMCA_DP_C2M_P10
GXBR4D_TX_CH4N AT2 FMCA_DP_C2M_N10

FMCA_DP_M2C_P11 AH5
FMCA_DP_M2C_N11 AH6
GXBR4D_RX_CH5P, GXBR4D_REFCLK5P
GXBR4D_RX_CH5N, GXBR4D_REFCLK5N
GXBR4D_TX_CH5P AR3 FMCA_DP_C2M_P11
GXBR4D_TX_CH5N AR4 FMCA_DP_C2M_N11

AG8
10.0K R335 AG7
REFCLK_GXBR4D_CHTP
REFCLK_GXBR4D_CHTN

FMCA_GBTCLK_M2C_P1 AJ8
FMCA_GBTCLK_M2C_N1 AJ7
REFCLK_GXBR4D_CHBP
REFCLK_GXBR4D_CHBN

10AX115F1932C

U28P

ARRIA 10 - RIGHT TRANSCEIVER BANK-4G

FMCB_DP_M2C_P6 R3
FMCB_DP_M2C_N6 R4
GXBR4G_RX_CH0P, GXBR4G_REFCLK0P
GXBR4G_RX_CH0N, GXBR4G_REFCLK0N
GXBR4G_TX_CH0P K1 FMCB_DP_C2M_P6
GXBR4G_TX_CH0N K2 FMCB_DP_C2M_N6

FMCB_DP_M2C_P7 P5
FMCB_DP_M2C_N7 P6
GXBR4G_RX_CH1P, GXBR4G_REFCLK1P
GXBR4G_RX_CH1N, GXBR4G_REFCLK1N
GXBR4G_TX_CH1P J3 FMCB_DP_C2M_P7
GXBR4G_TX_CH1N J4 FMCB_DP_C2M_N7

FMCB_DP_M2C_P8 N3
FMCB_DP_M2C_N8 N4
GXBR4G_RX_CH2P, GXBR4G_REFCLK2P
GXBR4G_RX_CH2N, GXBR4G_REFCLK2N
GXBR4G_TX_CH2P H1 FMCB_DP_C2M_P8
GXBR4G_TX_CH2N H2 FMCB_DP_C2M_N8

FMCB_DP_M2C_P9 M5
FMCB_DP_M2C_N9 M6
GXBR4G_RX_CH3P, GXBR4G_REFCLK3P
GXBR4G_RX_CH3N, GXBR4G_REFCLK3N
GXBR4G_TX_CH3P G3 FMCB_DP_C2M_P9
GXBR4G_TX_CH3N G4 FMCB_DP_C2M_N9

FMCB_DP_M2C_P10 L3
FMCB_DP_M2C_N10 L4
GXBR4G_RX_CH4P, GXBR4G_REFCLK4P
GXBR4G_RX_CH4N, GXBR4G_REFCLK4N
GXBR4G_TX_CH4P F1 FMCB_DP_C2M_P10
GXBR4G_TX_CH4N F2 FMCB_DP_C2M_N10

FMCB_DP_M2C_P11 K5
FMCB_DP_M2C_N11 K6
GXBR4G_RX_CH5P, GXBR4G_REFCLK5P
GXBR4G_RX_CH5N, GXBR4G_REFCLK5N
GXBR4G_TX_CH5P E3 FMCB_DP_C2M_P11
GXBR4G_TX_CH5N E4 FMCB_DP_C2M_N11

R8
10.0K R350 R7
REFCLK_GXBR4G_CHTP
REFCLK_GXBR4G_CHTN

FMCB_GBTCLK_M2C_P1 U8
FMCB_GBTCLK_M2C_N1 U7
REFCLK_GXBR4G_CHBP
REFCLK_GXBR4G_CHBN

10AX115F1932C

10 REFCLK_FMCA_P
10 REFCLK_FMCA_N
10 REFCLK_FMCB_P
10 REFCLK_FMCB_N

U28N

ARRIA 10 - RIGHT TRANSCEIVER BANK-4E

FMCA_DP_M2C_P12 AG3
FMCA_DP_M2C_N12 AG4
GXBR4E_RX_CH0P, GXBR4E_REFCLK0P
GXBR4E_RX_CH0N, GXBR4E_REFCLK0N
GXBR4E_TX_CH0P AP1 FMCA_DP_C2M_P12
GXBR4E_TX_CH0N AP2 FMCA_DP_C2M_N12

FMCA_DP_M2C_P13 AF5
FMCA_DP_M2C_N13 AF6
GXBR4E_RX_CH1P, GXBR4E_REFCLK1P
GXBR4E_RX_CH1N, GXBR4E_REFCLK1N
GXBR4E_TX_CH1P AM1 FMCA_DP_C2M_P13
GXBR4E_TX_CH1N AM2 FMCA_DP_C2M_N13

FMCA_DP_M2C_P14 AE3
FMCA_DP_M2C_N14 AE4
GXBR4E_RX_CH2P, GXBR4E_REFCLK2P
GXBR4E_RX_CH2N, GXBR4E_REFCLK2N
GXBR4E_TX_CH2P AK1 FMCA_DP_C2M_P14
GXBR4E_TX_CH2N AK2 FMCA_DP_C2M_N14

FMCA_DP_M2C_P15 AD5
FMCA_DP_M2C_N15 AD6
GXBR4E_RX_CH3P, GXBR4E_REFCLK3P
GXBR4E_RX_CH3N, GXBR4E_REFCLK3N
GXBR4E_TX_CH3P AH1 FMCA_DP_C2M_P15
GXBR4E_TX_CH3N AH2 FMCA_DP_C2M_N15

AC3
AC4
GXBR4E_RX_CH4P, GXBR4E_REFCLK4P
GXBR4E_RX_CH4N, GXBR4E_REFCLK4N
GXBR4E_TX_CH4P AF1
GXBR4E_TX_CH4N AF2

AB5
AB6
GXBR4E_RX_CH5P, GXBR4E_REFCLK5P
GXBR4E_RX_CH5N, GXBR4E_REFCLK5N
GXBR4E_TX_CH5P AD1
GXBR4E_TX_CH5N AD2

REFCLK4_P AC8
REFCLK4_N AC7
REFCLK_GXBR4E_CHTP
REFCLK_GXBR4E_CHTN

AE8
10.0K R351 AE7
REFCLK_GXBR4E_CHBP
REFCLK_GXBR4E_CHBN

10AX115F1932C

U28Q

ARRIA 10 - RIGHT TRANSCEIVER BANK-4H

FMCB_DP_M2C_P12 H5
FMCB_DP_M2C_N12 H6
GXBR4H_RX_CH0P, GXBR4H_REFCLK0P
GXBR4H_RX_CH0N, GXBR4H_REFCLK0N
GXBR4H_TX_CH0P D1 FMCB_DP_C2M_P12
GXBR4H_TX_CH0N D2 FMCB_DP_C2M_N12

FMCB_DP_M2C_P13 G7
FMCB_DP_M2C_N13 G8
GXBR4H_RX_CH1P, GXBR4H_REFCLK1P
GXBR4H_RX_CH1N, GXBR4H_REFCLK1N
GXBR4H_TX_CH1P C3 FMCB_DP_C2M_P13
GXBR4H_TX_CH1N C4 FMCB_DP_C2M_N13

FMCB_DP_M2C_P14 F5
FMCB_DP_M2C_N14 F6
GXBR4H_RX_CH2P, GXBR4H_REFCLK2P
GXBR4H_RX_CH2N, GXBR4H_REFCLK2N
GXBR4H_TX_CH2P B1 FMCB_DP_C2M_P14
GXBR4H_TX_CH2N B2 FMCB_DP_C2M_N14

FMCB_DP_M2C_P15 E7
FMCB_DP_M2C_N15 E8
GXBR4H_RX_CH3P, GXBR4H_REFCLK3P
GXBR4H_RX_CH3N, GXBR4H_REFCLK3N
GXBR4H_TX_CH3P A3 FMCB_DP_C2M_P15
GXBR4H_TX_CH3N A4 FMCB_DP_C2M_N15

D5
D6
GXBR4H_RX_CH4P, GXBR4H_REFCLK4P
GXBR4H_RX_CH4N, GXBR4H_REFCLK4N
GXBR4H_TX_CH4P B5
GXBR4H_TX_CH4N B6

C7
C8
GXBR4H_RX_CH5P, GXBR4H_REFCLK5P
GXBR4H_RX_CH5N, GXBR4H_REFCLK5N
GXBR4H_TX_CH5P A7
GXBR4H_TX_CH5N A8

L8
10.0K R334 L7
REFCLK_GXBR4H_CHTP
REFCLK_GXBR4H_CHTN

N8
N7
REFCLK_GXBR4H_CHBP
REFCLK_GXBR4H_CHBN

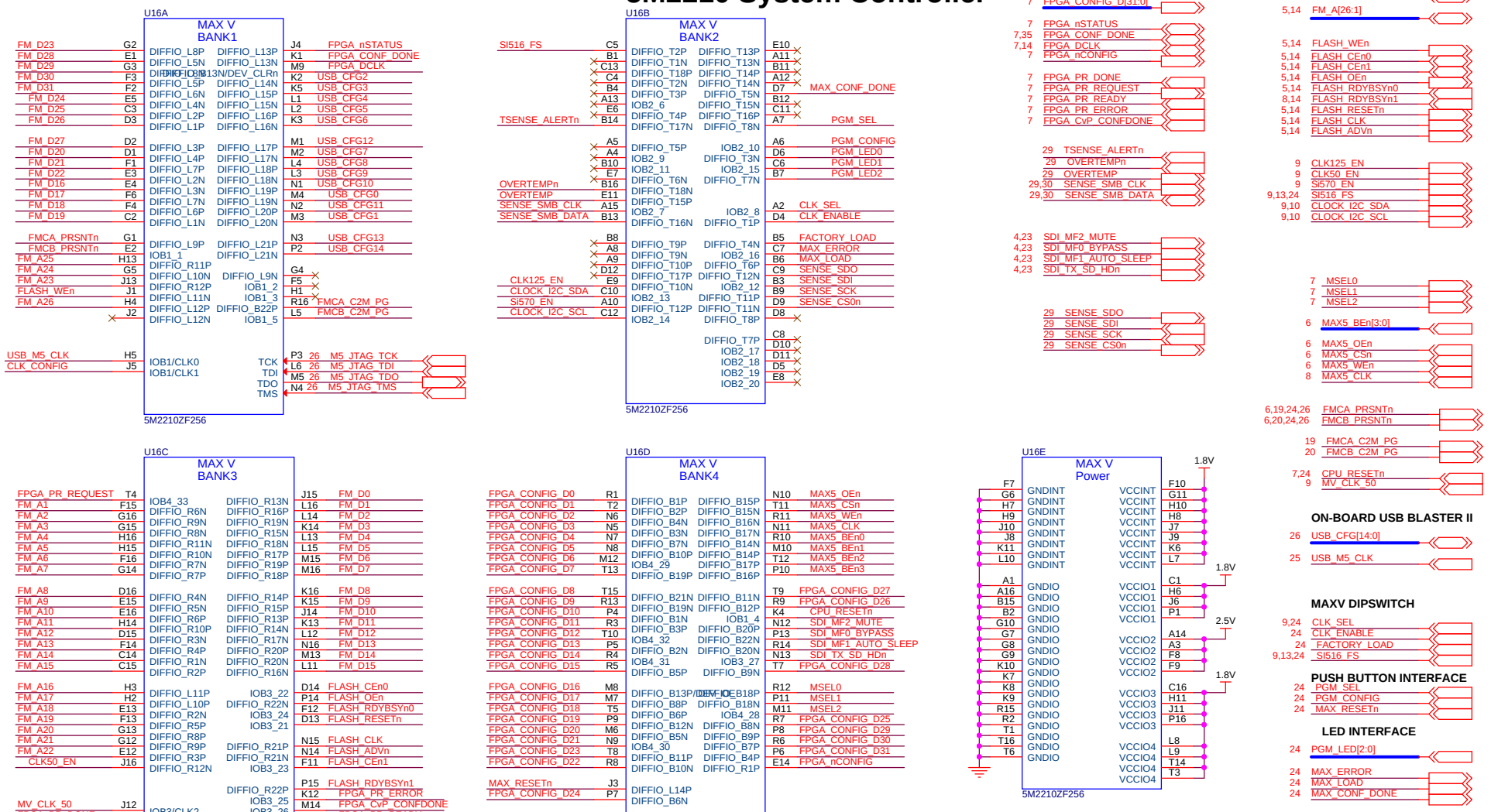
10AX115F1932C

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 12 of 49

5M2210 System Controller

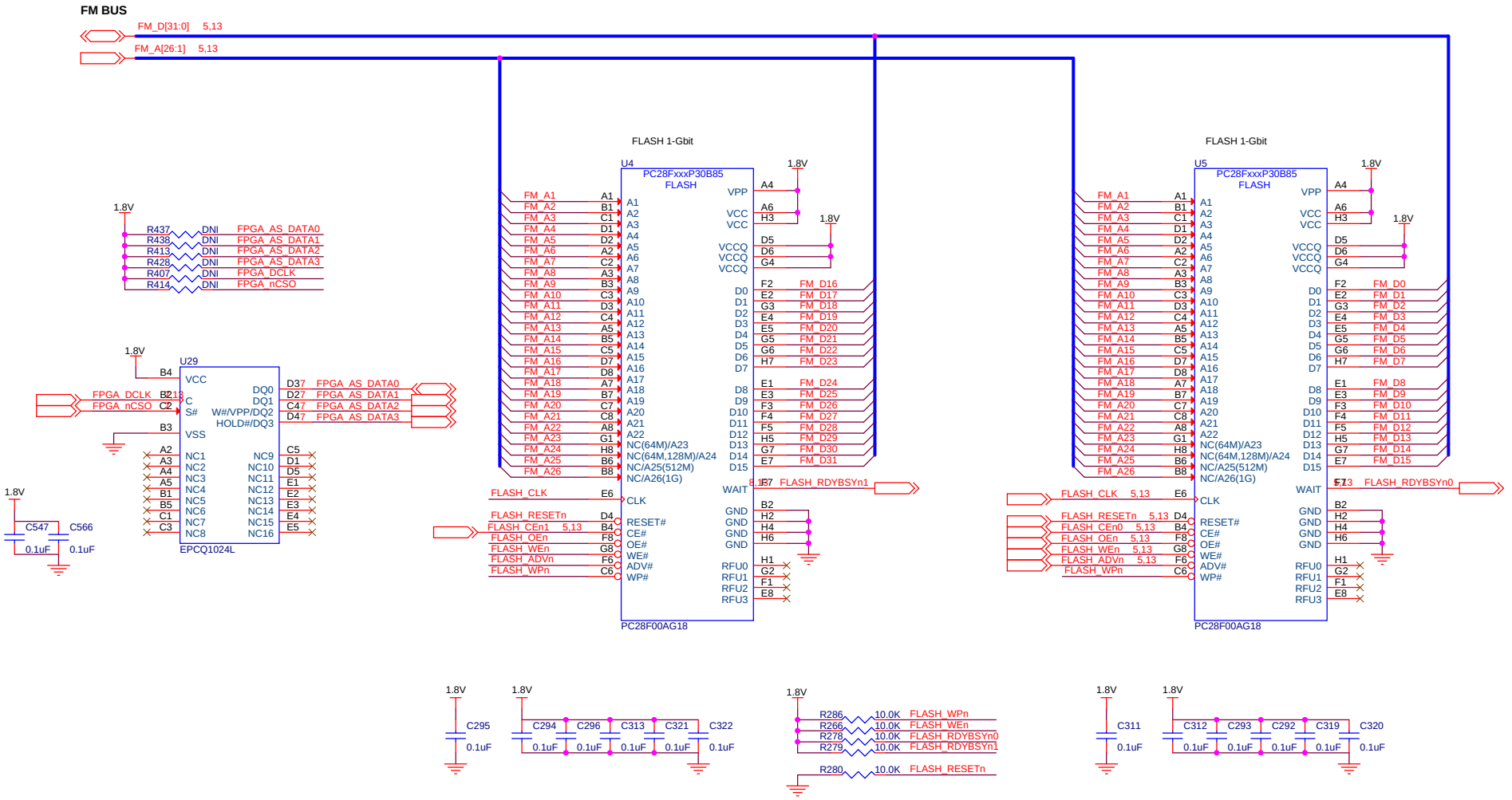


Title: **Arria 10 GX FPGA Development Kit**

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 13 of 49

FLASH



- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.
- When using dual x16 flash devices for an equivalent x32 (x16||x16) flash device a word consists of 32 data bits so addressing starts with FM_A1 mapped to address bit 2 in software.

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 14 of 49

10/100/1000 Ethernet

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autosel, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber

SGMII Mode (default)

88E1111-B2-CAA1C000 EOL
88E1111-B2-NDC2C000 Replacement

DVDD = 1.0V
DVDD = 1.2V

Place near 88E1111 PHY

ENET_DVDD = 1.0V/0.207A

Title: Arria 10 GX FPGA Development Kit

Size: B | Document Number: 150-0321301-E3 (6XX-44366R) | Rev: E3.1

Date: Wednesday, August 10, 2016 | Sheet 15 of 49

External Memory Interface Connector Map

DDR3 x72 (DQS x8	DDR4 x72 (DQS x8 Groups)	RLDRAM3 x36 (DQS x8/x9 Groups)	QDR IV x36 (DQS x18 Groups)	HiLo Pin Name	HiLo Pin Number
				CONFIG0	L6
				CONFIG1	M6
A0	A0	A0	A1	MEM_ADDR_CMD[0]	F1
A1	A1	A1	A2	MEM_ADDR_CMD[1]	H1
A10	A10	A10	A11	MEM_ADDR_CMD[10]	E4
A11	A11	A11	A12	MEM_ADDR_CMD[11]	F4
A12	A12	A12	A13	MEM_ADDR_CMD[12]	G4
A13	A13	A13	A14	MEM_ADDR_CMD[13]	H4
A14	A14	A14	A15	MEM_ADDR_CMD[14]	J4
A15	A15	A15	A16	MEM_ADDR_CMD[15]	K4
BA0	BA0	BA0	A19	MEM_ADDR_CMD[16]	M1
BA1	BA1	BA1	A20	MEM_ADDR_CMD[17]	M2
BA2	BG0	BA2	A21	MEM_ADDR_CMD[18]	N2
CASn	A17	A17	A18	MEM_ADDR_CMD[19]	L4
A2	A2	A2	A3	MEM_ADDR_CMD[2]	F2
CKE0	CKE0	A20	RWAn	MEM_ADDR_CMD[20]	P5
CKE1	CKE1	WEn	RWBn	MEM_ADDR_CMD[21]	M5
CSn0	CSn0	CSn0	LBK0n	MEM_ADDR_CMD[22]	P1
CSn1	ACTn	CSn1	LBK1n	MEM_ADDR_CMD[23]	R4
ODT0	ODT0	A18	LDAn	MEM_ADDR_CMD[24]	M4
ODT1	ODT1	A19	LDBn	MEM_ADDR_CMD[25]	R3
RASn	A16	A16	A17	MEM_ADDR_CMD[26]	L2
RESETn	RESETn	RESETn	RESETn	MEM_ADDR_CMD[27]	K1
WEn	BG1	BA3	CFGn	MEM_ADDR_CMD[28]	P2
	ALERTn	CSn3	A22	MEM_ADDR_CMD[29]	N4
A3	A3	A3	A4	MEM_ADDR_CMD[3]	G2
	CSn1	CSn2	AINV	MEM_ADDR_CMD[30]	P4
	PAR	REFn	A0	MEM_ADDR_CMD[31]	N3
A4	A4	A4	A5	MEM_ADDR_CMD[4]	H2
A5	A5	A5	A6	MEM_ADDR_CMD[5]	J2
A6	A6	A6	A7	MEM_ADDR_CMD[6]	K2
A7	A7	A7	A8	MEM_ADDR_CMD[7]	G3
A8	A8	A8	A9	MEM_ADDR_CMD[8]	J3
A9	A9	A9	A10	MEM_ADDR_CMD[9]	L3
CK_N0	CK_N0	CK_N	CK_N	MEM_CLK_N	V2
CK_P0	CK_P0	CK_P	CK_P	MEM_CLK_P	V1
DM0	LDM_n0		DINVA0	MEM_DMA[0]	B10
DM1	UDM_n0	DM1	QVLDA0	MEM_DMA[1]	C4
DM2	LDM_n1		DINVA1	MEM_DMA[2]	B17
DM3	UDM_n1		QVLDA1	MEM_DMA[3]	F17
DM4	LDM_n2	DQ18	DINVB0	MEM_DMB[0]	M16
DM5	UDM_n2		QVLDB0	MEM_DMB[1]	U16
DM6	LDM_n3	DQ0	DINVB1	MEM_DMB[2]	U11
DM7	UDM_n3		QVLDB1	MEM_DMB[3]	U6
DM8	LDM_n4			MEM_DQ_ADDR_CMD[0]	R6
DQ64	DQ64			MEM_DQ_ADDR_CMD[1]	T1
DQ65	DQ65			MEM_DQ_ADDR_CMD[2]	R2
DQ66	DQ66			MEM_DQ_ADDR_CMD[3]	T2

DDR3 x72 (DQS x8	DDR4 x72 (DQS x8 Groups)	RLDRAM3 x36 (DQS x8/x9 Groups)	QDR IV x36 (DQS x18 Groups)	HiLo Pin Name	HiLo Pin Number
DQ67	DQ67			MEM_DQ_ADDR_CMD[4]	U2
DQ68	DQ68			MEM_DQ_ADDR_CMD[5]	U3
DQ69	DQ69		AP	MEM_DQ_ADDR_CMD[6]	T4
DQ70	DQ70		A24	MEM_DQ_ADDR_CMD[7]	U4
DQ71	DQ71		A23	MEM_DQ_ADDR_CMD[8]	T5
DQ0	DQ0		DQA0	MEM_DQA[0]	A4
DQ1	DQ1		DQA1	MEM_DQA[1]	B4
DQ10	DQ10	DQ11	DQA9	MEM_DQA[10]	C2
DQ11	DQ11	DQ12	DQA10	MEM_DQA[11]	C3
DQ12	DQ12	DQ13	DQA11	MEM_DQA[12]	E3
DQ13	DQ13	DQ14	DQA12	MEM_DQA[13]	D4
DQ14	DQ14	DQ15	DQA13	MEM_DQA[14]	D1
DQ15	DQ15	DQ16	DQA14	MEM_DQA[15]	D2
DQ16	DQ16	QVLD1	DQA18	MEM_DQA[16]	A12
DQ17	DQ17		DQA19	MEM_DQA[17]	B12
DQ18	DQ18		DQA20	MEM_DQA[18]	B13
DQ19	DQ19		DQA21	MEM_DQA[19]	B14
DQ2	DQ2		DQA2	MEM_DQA[2]	B5
DQ20	DQ20		DQA22	MEM_DQA[20]	C15
DQ21	DQ21		DQA23	MEM_DQA[21]	A16
DQ22	DQ22		DQA24	MEM_DQA[22]	B16
DQ23	DQ23		QKA_N1	MEM_DQA[23]	A18
DQ24	DQ24	DQ27	DQA25	MEM_DQA[24]	C16
DQ25	DQ25	DQ28	DQA26	MEM_DQA[25]	D16
DQ26	DQ26	DQ29	DQA27	MEM_DQA[26]	E16
DQ27	DQ27	DQ30	DQA28	MEM_DQA[27]	F16
DQ28	DQ28	DQ31	DQA29	MEM_DQA[28]	D17
DQ29	DQ29	DQ32	DQA30	MEM_DQA[29]	C18
DQ3	DQ3		DQA3	MEM_DQA[3]	B6
DQ30	DQ30	DQ33	DQA31	MEM_DQA[30]	D18
DQ31	DQ31	DQ34	DQA32	MEM_DQA[31]	E18
		DQ17	DQA15	MEM_DQA[32]	E2
		DQ35	DQA33	MEM_DQA[33]	G16
DQ4	DQ4		DQA4	MEM_DQA[4]	A8
DQ5	DQ5		DQA5	MEM_DQA[5]	B8
DQ6	DQ6		DQA6	MEM_DQA[6]	B9
DQ7	DQ7		QKA_N0	MEM_DQA[7]	A10
DQ8	DQ8	DQ9	DQA7	MEM_DQA[8]	B1
DQ9	DQ9	DQ10	DQA8	MEM_DQA[9]	B2
DQ32	DQ32	DQ19	DQB0	MEM_DQB[0]	H16
DQ33	DQ33	DQ20	DQB1	MEM_DQB[1]	J16
DQ42	DQ42		DQB9	MEM_DQB[10]	P17
DQ43	DQ43		DQB10	MEM_DQB[11]	P18
DQ44	DQ44		DQB11	MEM_DQB[12]	R18
DQ45	DQ45		DQB12	MEM_DQB[13]	T16
DQ46	DQ46		DQB13	MEM_DQB[14]	T17
DQ47	DQ47		DQB14	MEM_DQB[15]	T18
DQ48	DQ48	DQ1	DQB18	MEM_DQB[16]	U15

DDR3 x72 (DQS x8	DDR4 x72 (DQS x8 Groups)	RLDRAM3 x36 (DQS x8/x9 Groups)	QDR IV x36 (DQS x18 Groups)	HiLo Pin Name	HiLo Pin Number
DQ49	DQ49	DQ2	DQB19	MEM_DQB[17]	T14
DQ50	DQ50	DQ3	DQB20	MEM_DQB[18]	U14
DQ51	DQ51	DQ4	DQB21	MEM_DQB[19]	V14
DQ34	DQ34	DQ21	DQB2	MEM_DQB[2]	K16
DQ52	DQ52	DQ5	DQB22	MEM_DQB[20]	T13
DQ53	DQ53	DQ6	DQB23	MEM_DQB[21]	T12
DQ54	DQ54	DQ7	DQB24	MEM_DQB[22]	U12
DQ55	DQ55	DQ8	QKB_N1	MEM_DQB[23]	V12
DQ56	DQ56		DQB25	MEM_DQB[24]	T10
DQ57	DQ57		DQB26	MEM_DQB[25]	U10
DQ58	DQ58		DQB27	MEM_DQB[26]	V10
DQ59	DQ59		DQB28	MEM_DQB[27]	T9
DQ60	DQ60		DQB29	MEM_DQB[28]	T8
DQ61	DQ61		DQB30	MEM_DQB[29]	U8
DQ35	DQ35	DQ22	DQB3	MEM_DQB[3]	L16
DQ62	DQ62		DQB31	MEM_DQB[30]	U7
DQ63	DQ63		DQB32	MEM_DQB[31]	V6
			DQB15	MEM_DQB[32]	R16
			DQB33	MEM_DQB[33]	T6
DQ36	DQ36	DQ23	DQB4	MEM_DQB[4]	H17
DQ37	DQ37	DQ24	DQB5	MEM_DQB[5]	K17
DQ38	DQ38	DQ25	DQB6	MEM_DQB[6]	K18
DQ39	DQ39	DQ26	QKB_N0	MEM_DQB[7]	L18
DQ40	DQ40	QVLD0	DQB7	MEM_DQB[8]	M17
DQ41	DQ41		DQB8	MEM_DQB[9]	N18
DQS_N8	DQSL_N4			MEM_DQS_ADDR_CMD_N	V5
DQS_P8	DQSL_P4		PEn	MEM_DQS_ADDR_CMD_P	V4
DQS_N0	DQSL_N0		DQA17	MEM_DQSA_N[0]	A7
DQS_N1	DQSU_N0	QK1#	DKA_N0	MEM_DQSA_N[1]	A3
DQS_N2	DQSL_N1	DK1#	DQA35	MEM_DQSA_N[2]	A15
DQS_N3	DQSU_N1	QK3#	DKA_N1	MEM_DQSA_N[3]	G18
DQS_P0	DQSL_P0		DQA16	MEM_DQSA_P[0]	A6
DQS_P1	DQSU_P0	QK1	DKA_P0	MEM_DQSA_P[1]	A2
DQS_P2	DQSL_P1	DK1	DQA34	MEM_DQSA_P[2]	A14
DQS_P3	DQSU_P1	QK3	DKA_P1	MEM_DQSA_P[3]	F18
DQS_N4	DQSL_N2	QK2#	DQB17	MEM_DQSB_N[0]	J18
DQS_N5	DQSU_N2	DK0#	DKB_N0	MEM_DQSB_N[1]	V18
DQS_N6	DQSL_N3	QK0#	DQB35	MEM_DQSB_N[2]	V17
DQS_N7	DQSU_N3		DKB_N1	MEM_DQSB_N[3]	V9
DQS_P4	DQSL_P2	QK2	DQB16	MEM_DQSB_P[0]	H18
DQS_P5	DQSU_P2	DK0	DKB_P0	MEM_DQSB_P[1]	U18
DQS_P6	DQSL_P3	QK0	DQB34	MEM_DQSB_P[2]	V16
DQS_P7	DQSU_P3		DKB_P1	MEM_DQSB_P[3]	V8
			QKA_P0	MEM_QKA_P[0]	A11
			QKA_P1	MEM_QKA_P[1]	B18
			QKB_P0	MEM_QKB_P[0]	M18
		DM0	QKB_P1	MEM_QKB_P[1]	V13

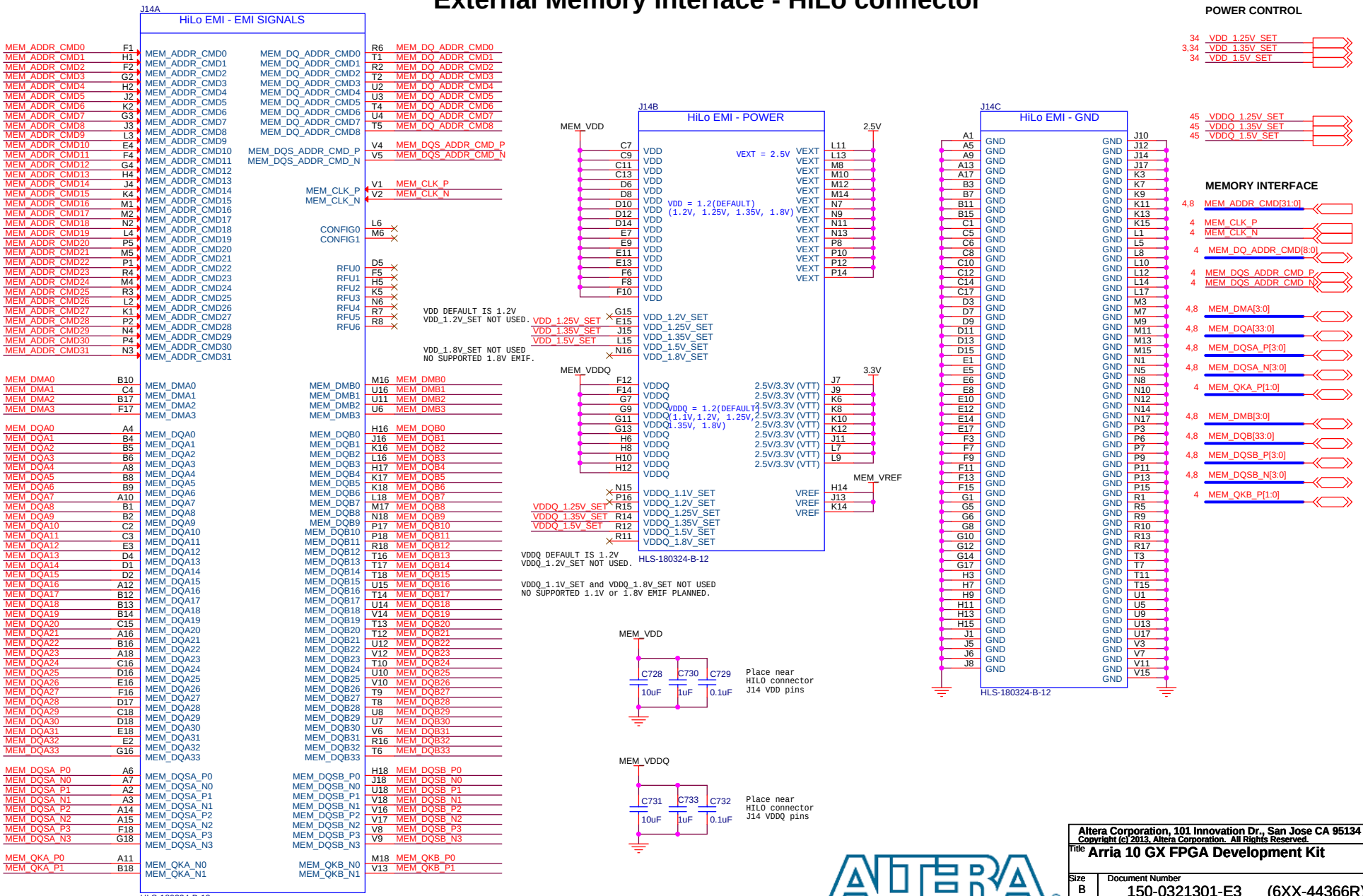
Altera Corporation, 101 Innovation Dr., San Jose CA 95134

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 16 of 49

External Memory Interface - HiLo connector

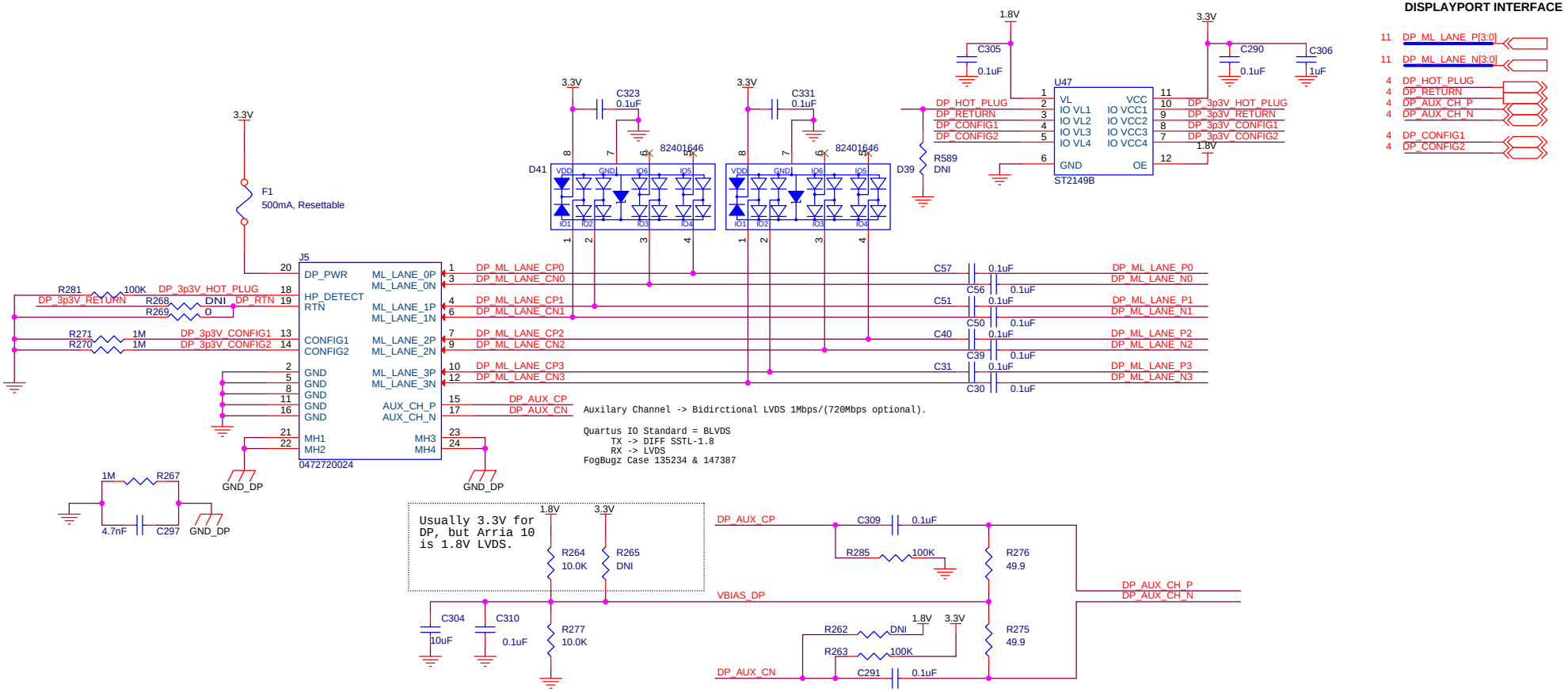


Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 17 of 49

Display Port (x4)



1) TX uses diff sstl18 configuration, which is able to meet peak-to-peak differential voltage and common mode voltage spec for DP.
2) RX uses LVDS input, but user need to ensure pin voltage at NF receiver end is <1.9v.
   a. If the channel is AC couple, then user need to choose the correct Vbias_RX so that Vpin < 1.9v. The spec is 0 – 2v, which is quite wide. Selecting Vbias_Rx at 2v region will cause NF device to have reliability issue.
   b. If the channel is DC couple, user need to make sure TX common mode voltage + ground reference differences between Tx and Rx will not cause Vpin for NF to be higher than 1.9v.

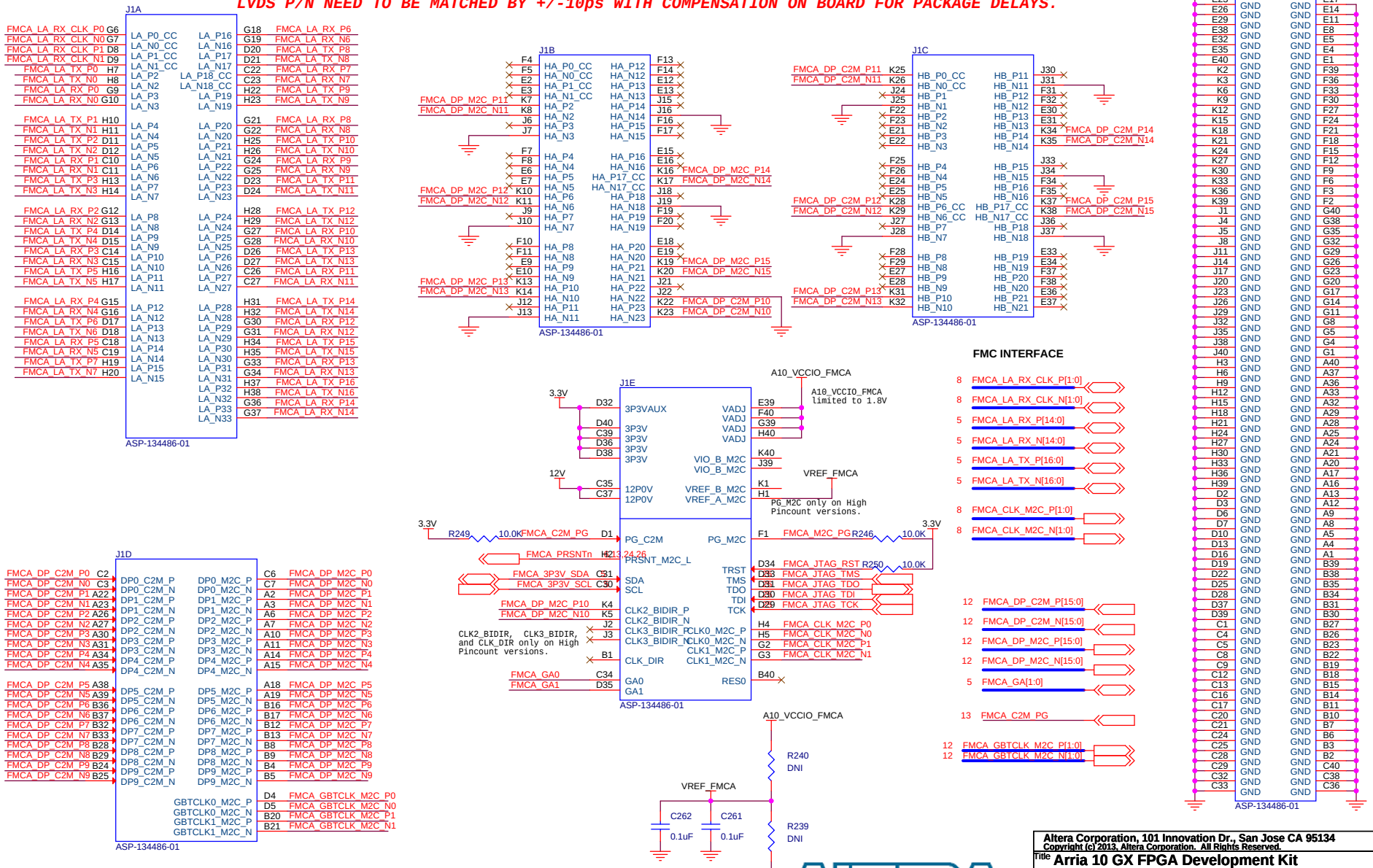
Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 18 of 49

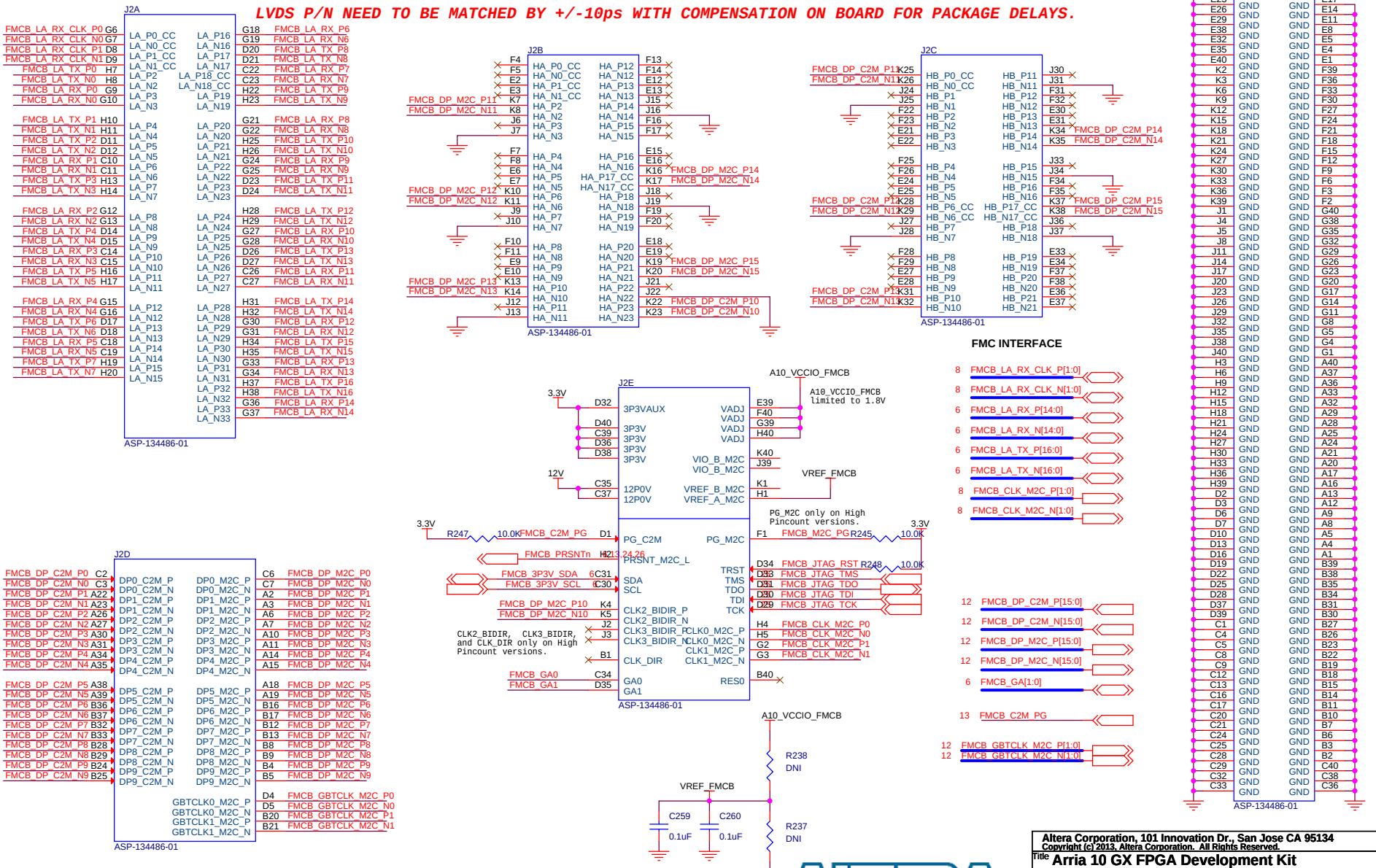
FMC Port A

LVDS P/N NEED TO BE MATCHED BY +/-10ps WITH COMPENSATION ON BOARD FOR PACKAGE DELAYS.



FMC Port B

LVDS P/N NEED TO BE MATCHED BY +/-10ps WITH COMPENSATION ON BOARD FOR PACKAGE DELAYS.



Altera Corporation, 101 Innovation Dr., San Jose CA 95134

Title	Arria 10 GX FPGA Development Kit		
Size B	Document Number 150-0321301-E3 (6XX-44366R)		Rev E3.1
Date: Wednesday, August 10, 2016	Sheet 20 of 49		

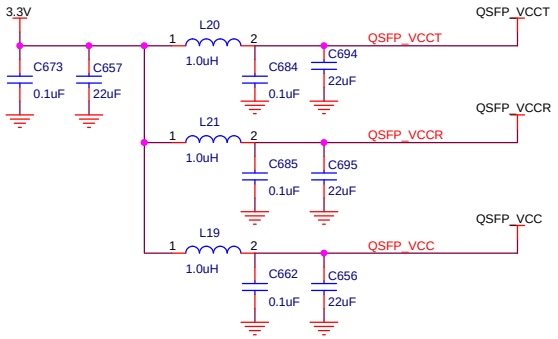
Quad Small Form-factor Pluggable (QSFP) Interface

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

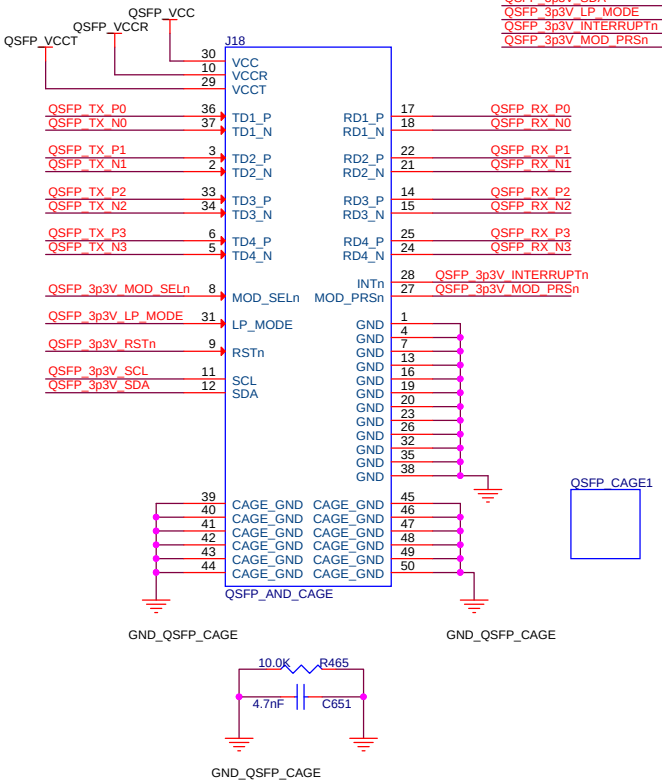
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

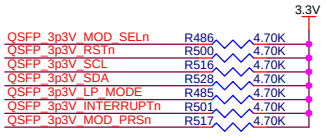
NOTE 3: DC blocking capacitors are in the module for RX and TX.

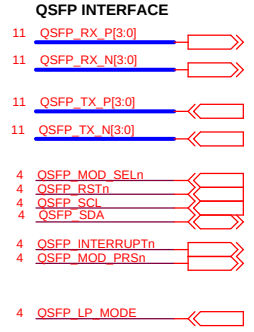
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.

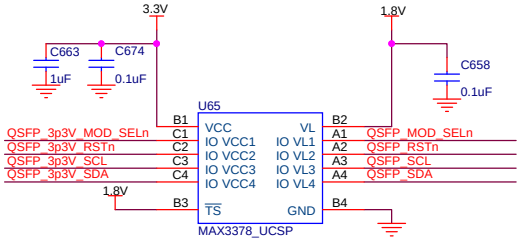


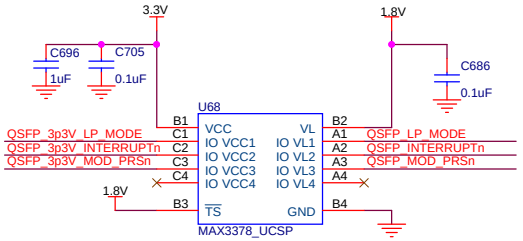
Maximum power is <= 3.5W (1.06 A)
Maximum inrush current = 1.3A











Altera Corporation, 101 Innovation Dr., San Jose CA 95134

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

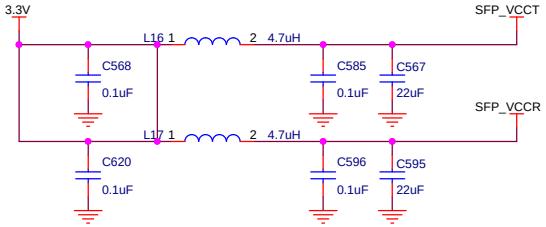
Date: Wednesday, August 10, 2016 Sheet 21 of 49

Small Form Factor Pluggable Plus (SFP+) Connector

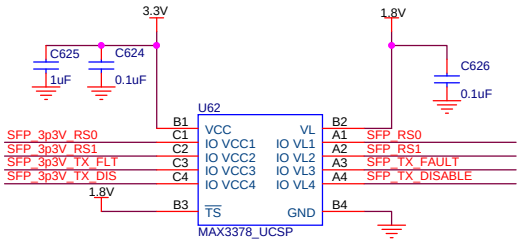
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

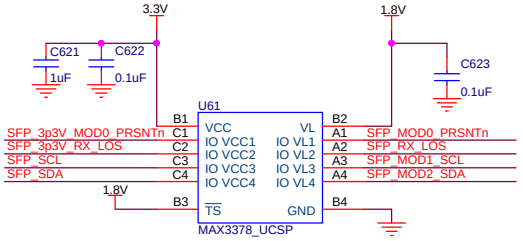
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

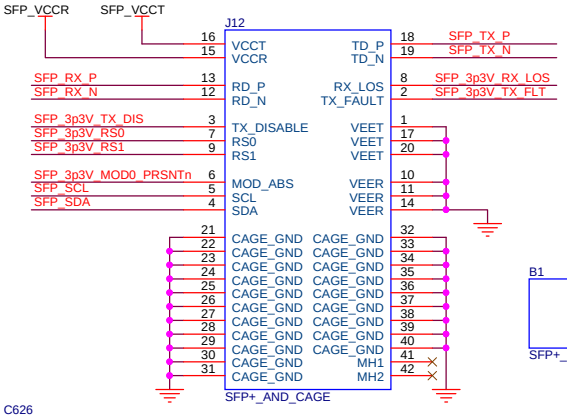
NOTE 3: DC blocking capacitors are in the module for RX and TX.



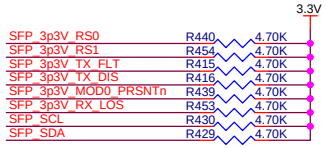
Level I power is < 1W (0.3 A)
Level II power is < 1.5W (0.45 A)
Level II Instantaneous peak current per rail 600mA





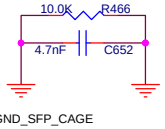


Optical (SFP+) Transceiver Cage & Connector

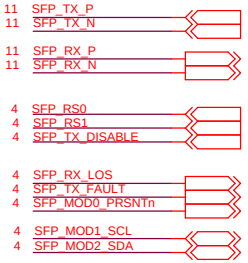


SFP modules have RS1 connected to GND.
If using SFP+ Rate Select pin are defined as:
RS1=0 -> TX datarates <= 4.25GB/s
RS1=1 -> TX datarates > 4.25GB/s

RS0=0 -> RX datarates <= 4.25GB/s
RS0=1 -> RX datarates > 4.25GB/s



SFP+ INTERFACE

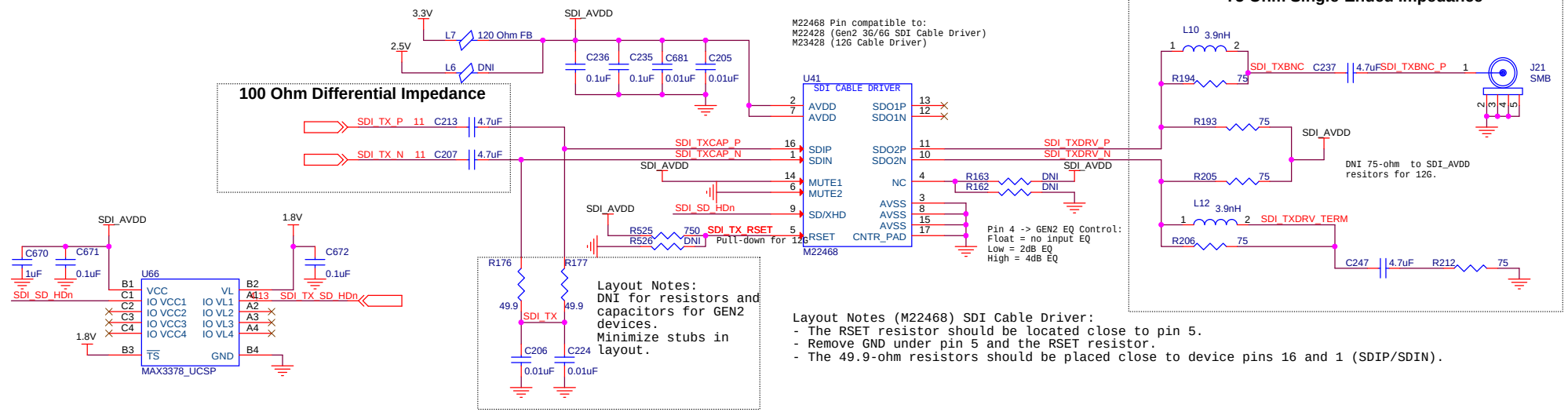


Title: **Arria 10 GX FPGA Development Kit**

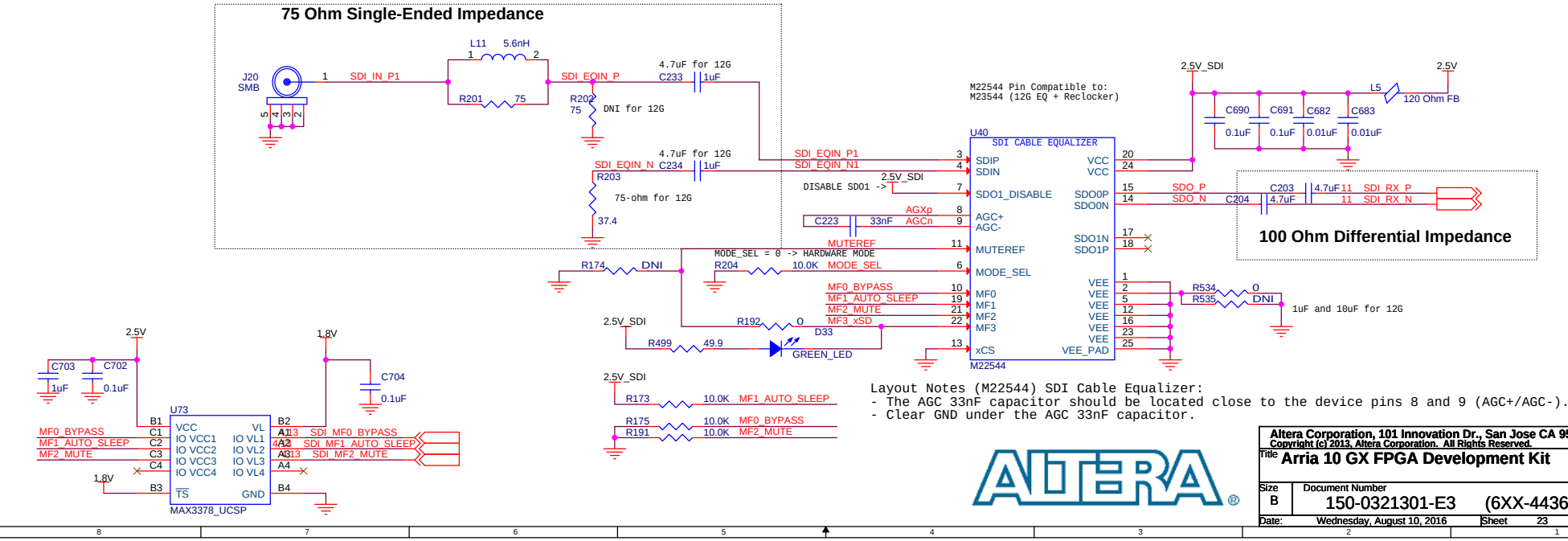
Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 22 of 49

SDI Cable Driver, Equalizer, and SMB



Layout Notes (M22468) SDI Cable Driver:
- The RSET resistor should be located close to pin 5.
- Remove GND under pin 5 and the RSET resistor.
- The 49.9-ohm resistors should be placed close to device pins 16 and 1 (SDIP/SDIN).



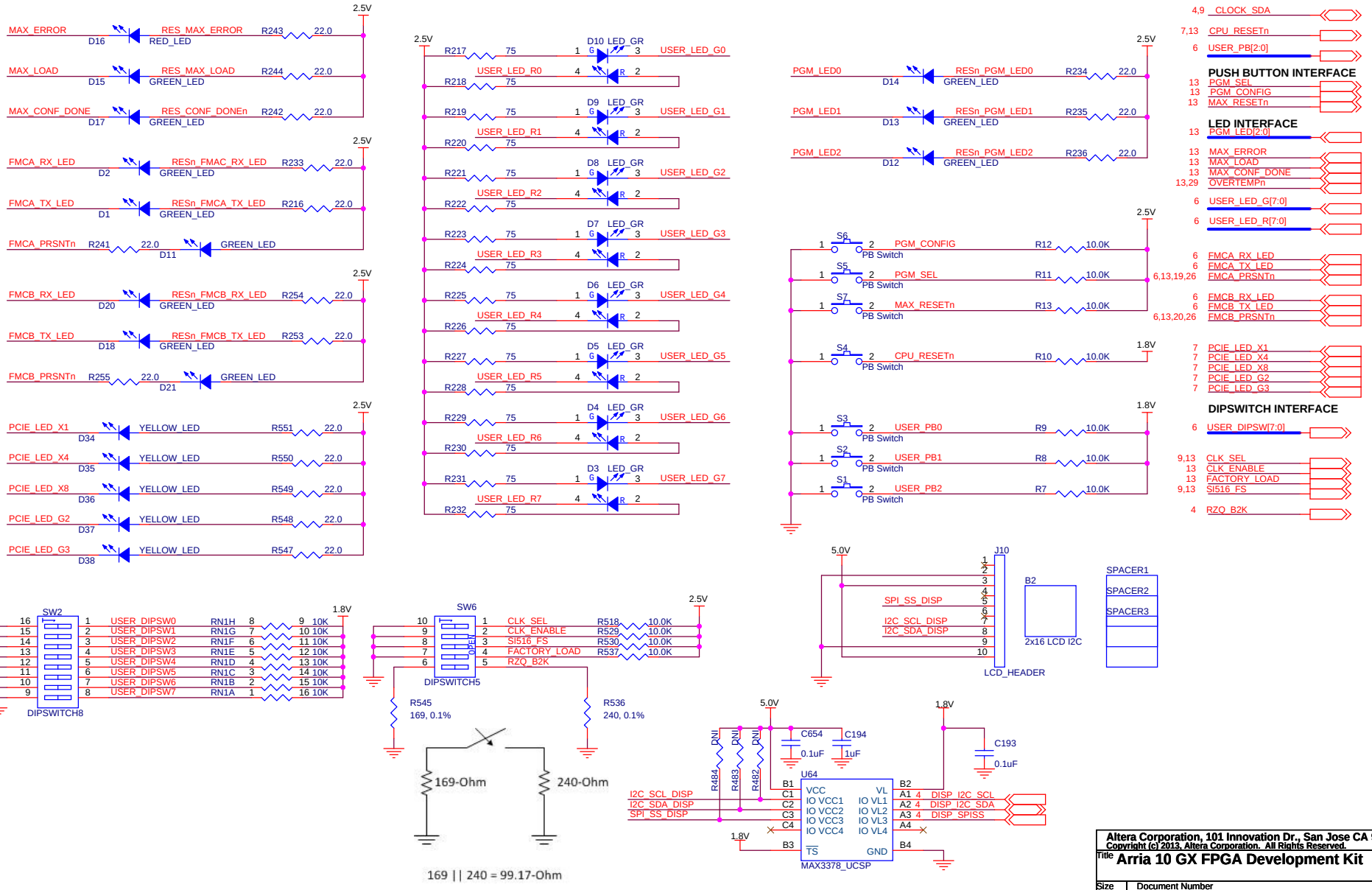
Layout Notes (M22544) SDI Cable Equalizer:
- The AGC 33nF capacitor should be located close to the device pins 8 and 9 (AGC+/AGC-).
- Clear GND under the AGC 33nF capacitor.

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 23 of 49

User I/O

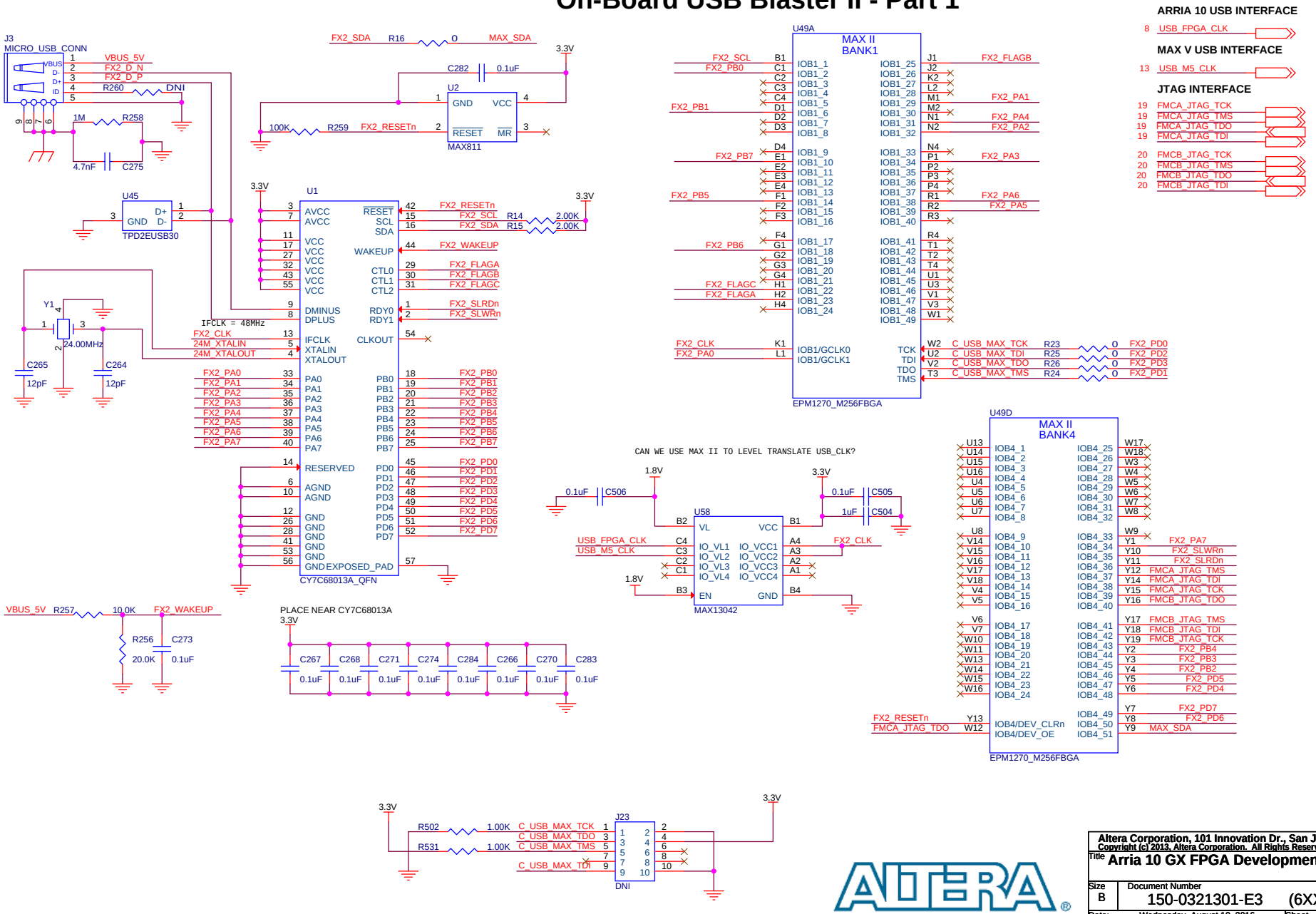


Title: **Arria 10 GX FPGA Development Kit**

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 24 of 49

On-Board USB Blaster II - Part 1



Altera Corporation, 101 Innovation Dr., San Jose CA 95134

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 25 of 49

On-Board USB Blaster II - Part 2

SW4 DIPSWITCH4
A10_JTAG_BYPASSn R473 10.0K
M5_JTAG_BYPASSn R474 10.0K
FMCA_JTAG_BYPASSn R487 10.0K
FMCB_JTAG_BYPASSn R488 10.0K
1.8V

Logic 0 = Device JTAG Bypass
Logic 1 = Device JTAG Enable

U49B MAX II BANK2 EPM1270_M256FBGA
JTAG_RX A1
USB_CFG14 A10
USB_CFG11 A11
USB_CFG10 A12
USB_CFG13 A13
USB_CFG12 A14
USB_CFG5 A15
USB_CFG9 A16
USB_CFG2 A17
USB_CFG6 A18
USB_CFG3 A19
SC_RX A2
USB_DATA3 A20
C_JTAG_TDO A3
SC_TX A4
FMCA_PRSNTn A5
M5_JTAG_TDI A6
M5_JTAG_TDO A7
M5_JTAG_TMS A8
M5_JTAG_TCK A9
B10 B11 B12 B13
IOB2_1 IOB2_2 IOB2_3 IOB2_4 IOB2_5 IOB2_6 IOB2_7 IOB2_8 IOB2_9 IOB2_10 IOB2_11 IOB2_12 IOB2_13 IOB2_14 IOB2_15 IOB2_16 IOB2_17 IOB2_18 IOB2_19 IOB2_20 IOB2_21 IOB2_22 IOB2_23 IOB2_24
IOB2_25 IOB2_26 IOB2_27 IOB2_28 IOB2_29 IOB2_30 IOB2_31 IOB2_32 IOB2_33 IOB2_34 IOB2_35 IOB2_36 IOB2_37 IOB2_38 IOB2_39 IOB2_40 IOB2_41 IOB2_42 IOB2_43 IOB2_44 IOB2_45 IOB2_46 IOB2_47 IOB2_48 IOB2_49 IOB2_50 IOB2_51 IOB2_52 IOB2_53
B14 USB_CFG7
B15 USB_CFG1
B16 USB_CFG4
B17 USB_CFG8
B18 USB_CFG0
B19 FMCB_PRSNTn
B2 JTAG_TX
B3 FMCB_JTAG_BYPASSn
B4 B5 B6 B7 B8 B9 C14 C15 C16
C17 A10_JTAG_BYPASSn
C5 C6 C7 D13 D14 D15 FMCB_JTAG_MASTERn
D16 D5 FMCA_JTAG_MASTERn D6 D7 D8 FMCA_JTAG_BYPASSn

1.8V
R43 10.0K M5_JTAG_TDI
R44 10.0K M5_JTAG_TMS
R45 1.00K M5_JTAG_TCK

U49C MAX II BANK3 EPM1270_M256FBGA
USB_DATA2 B20
M5_JTAG_BYPASSn C18
C19
USB_EMPTY C20
D17 D18 D19
USB_ADDR0 D20
E17 E18
C_JTAG_TMS E19
USB_FULL E20
F17 F18 F19
USB_ADDR1 F20
G17 G18 G19
C_JTAG_TDI G19
USB_OEn G20
H17 H19 H20
USB_DATA1 H20
USB_DISABLEn J19
USB_DATA6 M20
USB_DATA4 L20
IOB3_1 IOB3_2 IOB3_3 IOB3_4 IOB3_5 IOB3_6 IOB3_7 IOB3_8 IOB3_9 IOB3_10 IOB3_11 IOB3_12 IOB3_13 IOB3_14 IOB3_15 IOB3_16 IOB3_17 IOB3_18 IOB3_19 IOB3_20 IOB3_21 IOB3_22 IOB3_23 IOB3_24 IOB3_49 IOB3_50 IOB3_51 IOB3/GCLK2 IOB3/GCLK3
IOB3_25 IOB3_26 IOB3_27 IOB3_28 IOB3_29 IOB3_30 IOB3_31 IOB3_32 IOB3_33 IOB3_34 IOB3_35 IOB3_36 IOB3_37 IOB3_38 IOB3_39 IOB3_40 IOB3_41 IOB3_42 IOB3_43 IOB3_44 IOB3_45 IOB3_46 IOB3_47 IOB3_48 IOB3_52 IOB3_53
J20 USB_DATA0
K19
K20 USB_RDn
L19 C_JTAG_TCK
M19 USB_DATA5
N17
N19
N20 USB_DATA7
P17 P18 P19
P20 A10_JTAG_TDI
R17 R18 R19
R20 A10_JTAG_TCK
T17 T18
T19 USB_WRn
T20 USB_SCL
U17 U18 U19
U20 USB_RESETn
V19
V20 USB_SDA
W19
W20 A10_JTAG_TMS
Y20 A10_JTAG_TDO
1.8V
P20 A10_JTAG_TDI 10.0K R30
R20 A10_JTAG_TCK 1.00K R32
W20 A10_JTAG_TMS 10.0K R31

ARRIA 10 USB INTERFACE
5 USB_DATA[7:0]
5 USB_ADDR[1:0]
8 USB_FULL
8 USB_EMPTY
8 USB_SCL
8 USB_SDA
5 USB_RESETn
5 USB_OEn
5 USB_RDn
5 USB_WRn

MAX V USB INTERFACE
13 USB_CFG[14:0]

JTAG INTERFACE
7 A10_JTAG_TCK
7 A10_JTAG_TMS
7 A10_JTAG_TDO
7 A10_JTAG_TDI
13 M5_JTAG_TCK
13 M5_JTAG_TMS
13 M5_JTAG_TDO
13 M5_JTAG_TDI
6,13,19,24 FMCA_PRSNTn
6,13,20,24 FMCB_PRSNTn

1.8V
R33 1.00k USB_SCL
R27 1.00k USB_SDA
R39 1.00k USB_FULL
R40 1.00k USB_EMPTY
R42 DNI FMCA_JTAG_MASTERn
R46 DNI FMCB_JTAG_MASTERn

USB Blaster Programming Header
(uses JTAG mode only)
J17 2X5_100mil
2.5V R504 1.00k USB_DISABLEn
J17_JTAG_TCK R491 DNI C664 DNI
R503 1.00k
J17_JTAG_TCK
J17_JTAG_TDO
J17_JTAG_TMS
J17_JTAG_TDI
R477 1.00k
R467 1.00k

U49E MAX II Power EPM1270_M256FBGA
GNDINT J4 U12 M17 D12
GNDIO H3 J3 M4 N3 U9 V8 V9 V13 H18 J17 N18 C8 D9 C12 C13 M18
VCCINT K4 U11 L17 D11
VCCIO1 K3 L3 L4 M3
VCCIO2 C9 C10 D10 C11
VCCIO3 J18 K17 K18 L18
VCCIO4 U10 V10 V11 V12
2.5V 3.3V 1.8V

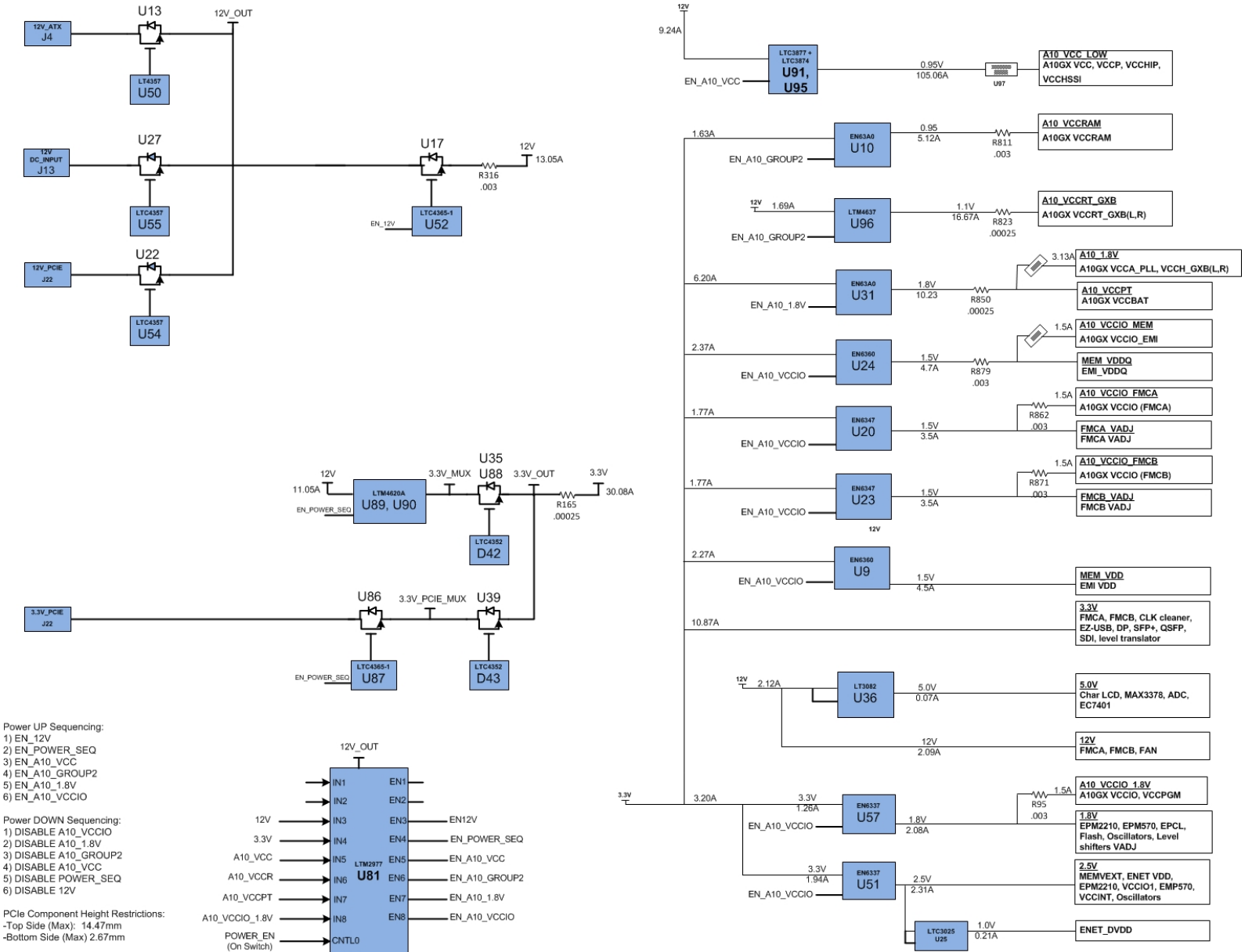
PLACE NEAR MAX II (U25)
C18 C43 C19 C17 C32 C33 C42 C41 C34 C35 0.1uF

U76 MAX13042
0.1uF C741
0.1uF C742
1uF C740
VL VCC EN GND
IO_VL1 IO_VL2 IO_VL3 IO_VL4 IO_VCC1 IO_VCC2 IO_VCC3 IO_VCC4
C_JTAG_TCK C_JTAG_TDO C_JTAG_TMS C_JTAG_TDI
J17_JTAG_TCK J17_JTAG_TDO J17_JTAG_TMS J17_JTAG_TDI

JTAG_RX D22 RESn_JTAG_RX R314 22.0
JTAG_TX D23 RESn_JTAG_TX R313 22.0
SC_RX D24 RESn_SC_RX R312 22.0
SC_TX D25 RESn_SC_TX R311 22.0
GREEN_LED

Title: Arria 10 GX FPGA Development Kit
Size: B
Document Number: 150-0321301-E3 (6XX-44366R)
Rev: E3.1
Date: Wednesday, August 10, 2016
Sheet 26 of 49

Power Tree



Power UP Sequencing:
1) EN_12V
2) EN_POWER_SEQ
3) EN_A10_VCC
4) EN_A10_GROUP2
5) EN_A10_1.8V
6) EN_A10_VCCIO

Power DOWN Sequencing:
1) DISABLE A10_VCCIO
2) DISABLE A10_1.8V
3) DISABLE A10_GROUP2
4) DISABLE A10_VCC
5) DISABLE POWER_SEQ
6) DISABLE 12V

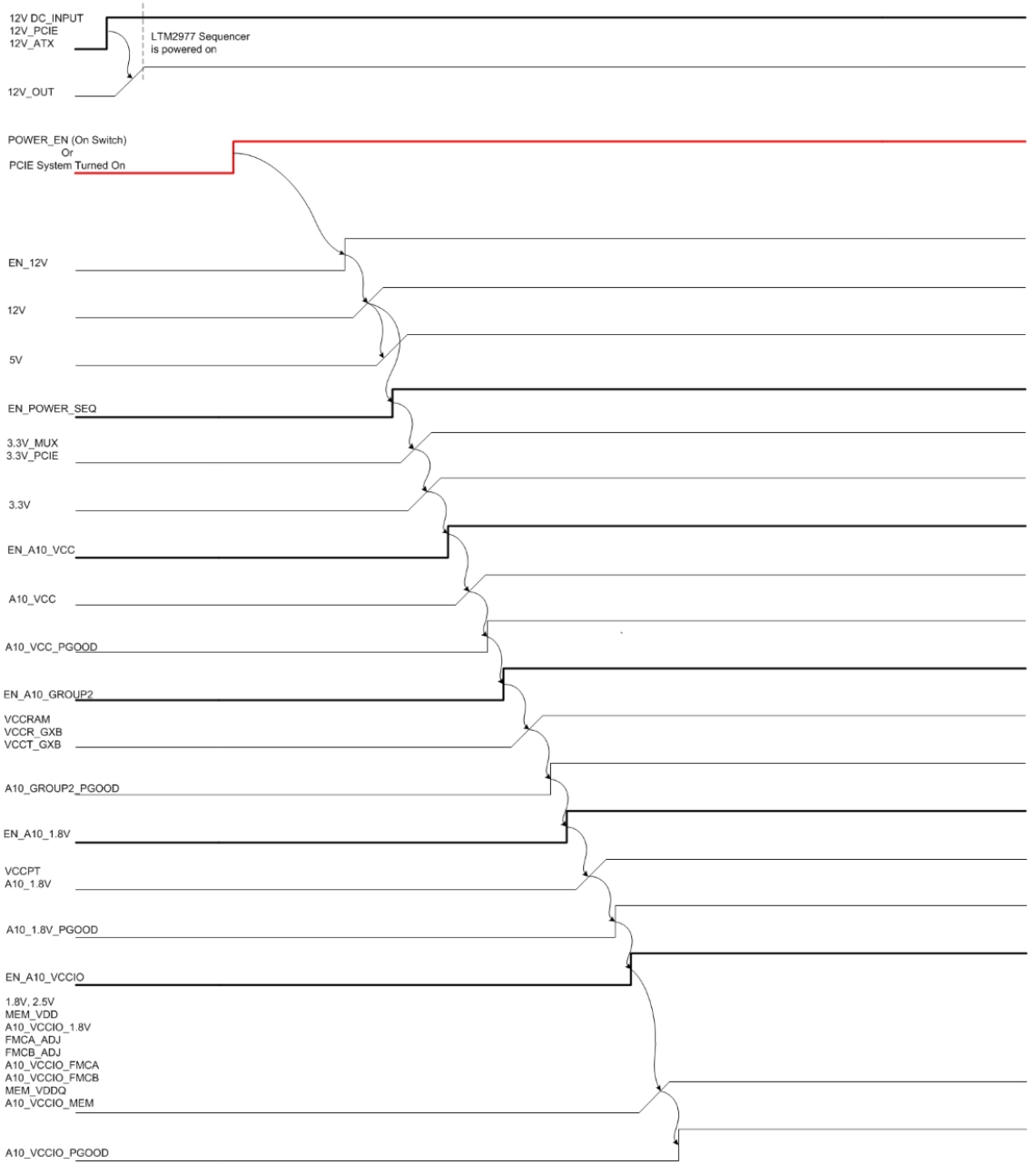
PCIe Component Height Restrictions:
-Top Side (Max): 14.47mm
-Bottom Side (Max) 2.67mm

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
C	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 27 of 49

Power-On Sequencing
(Power-Off is reverse of Power-On)

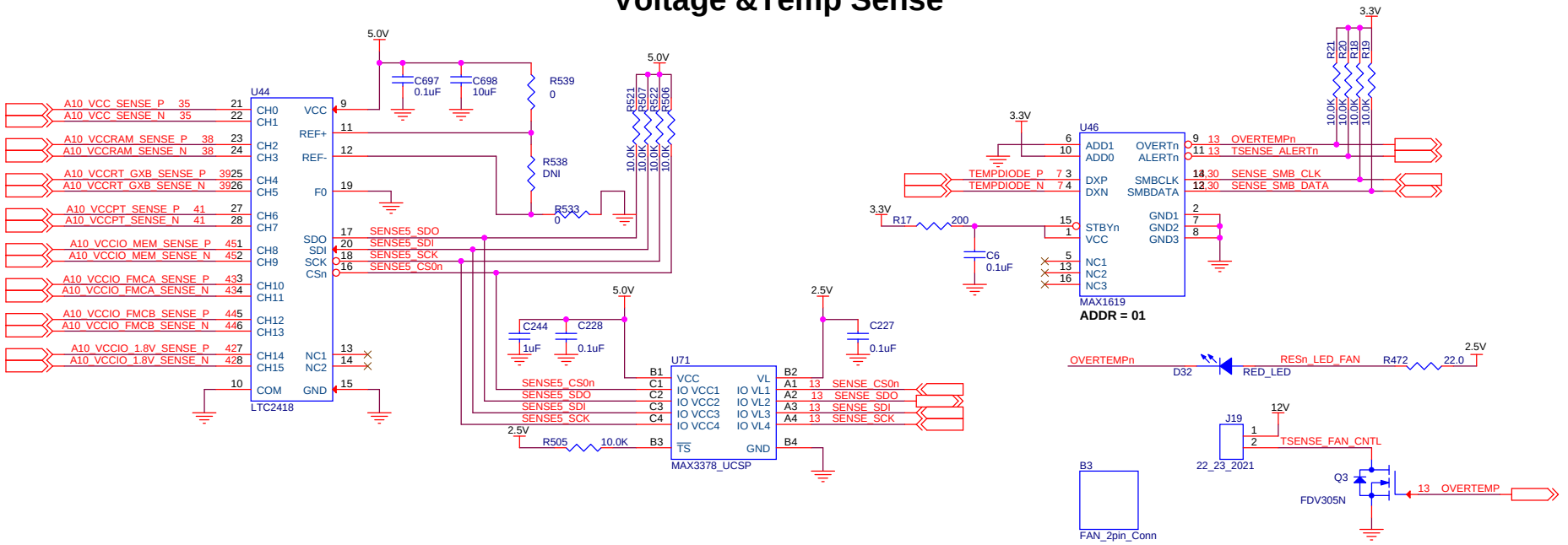


Title: **Arria 10 GX FPGA Development Kit**

Size	Document Number	Rev
C	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 28 of 49

Voltage &Temp Sense

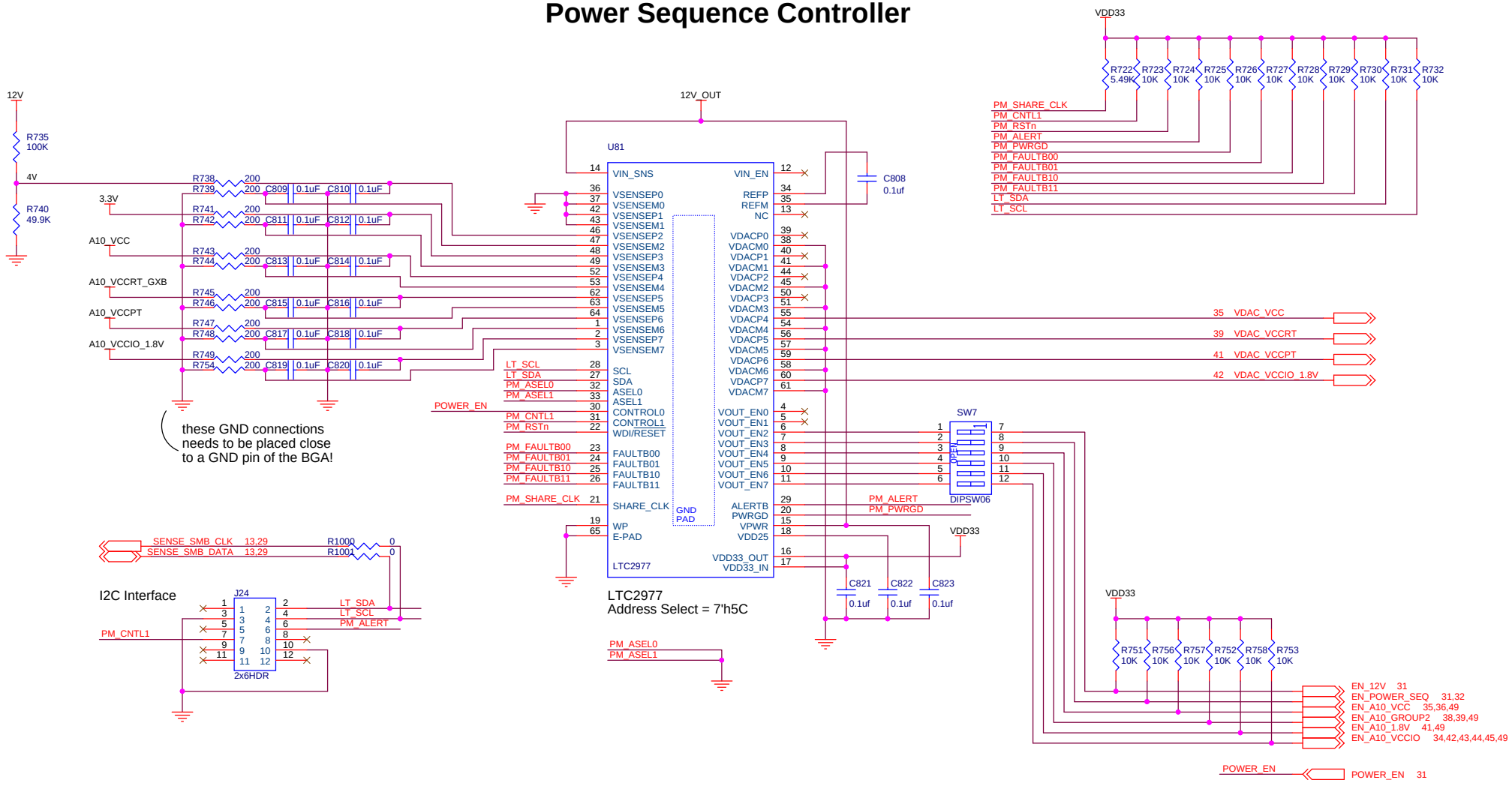


Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 29 of 49

Power Sequence Controller



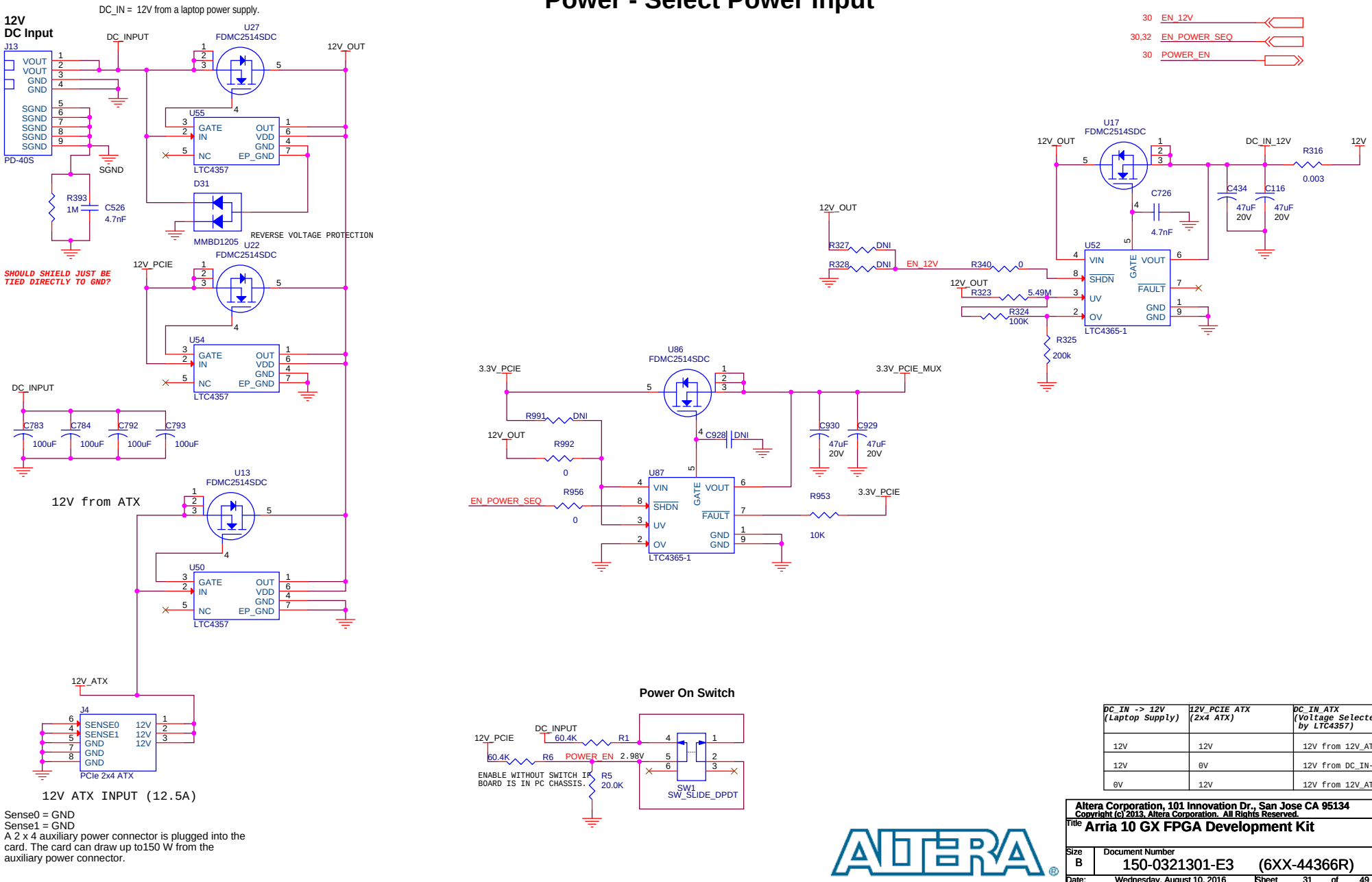
Altera Corporation, 101 Innovation Dr., San Jose CA 95134

Title: **Arria 10 GX FPGA Development Kit**

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 30 of 49

Power - Select Power Input



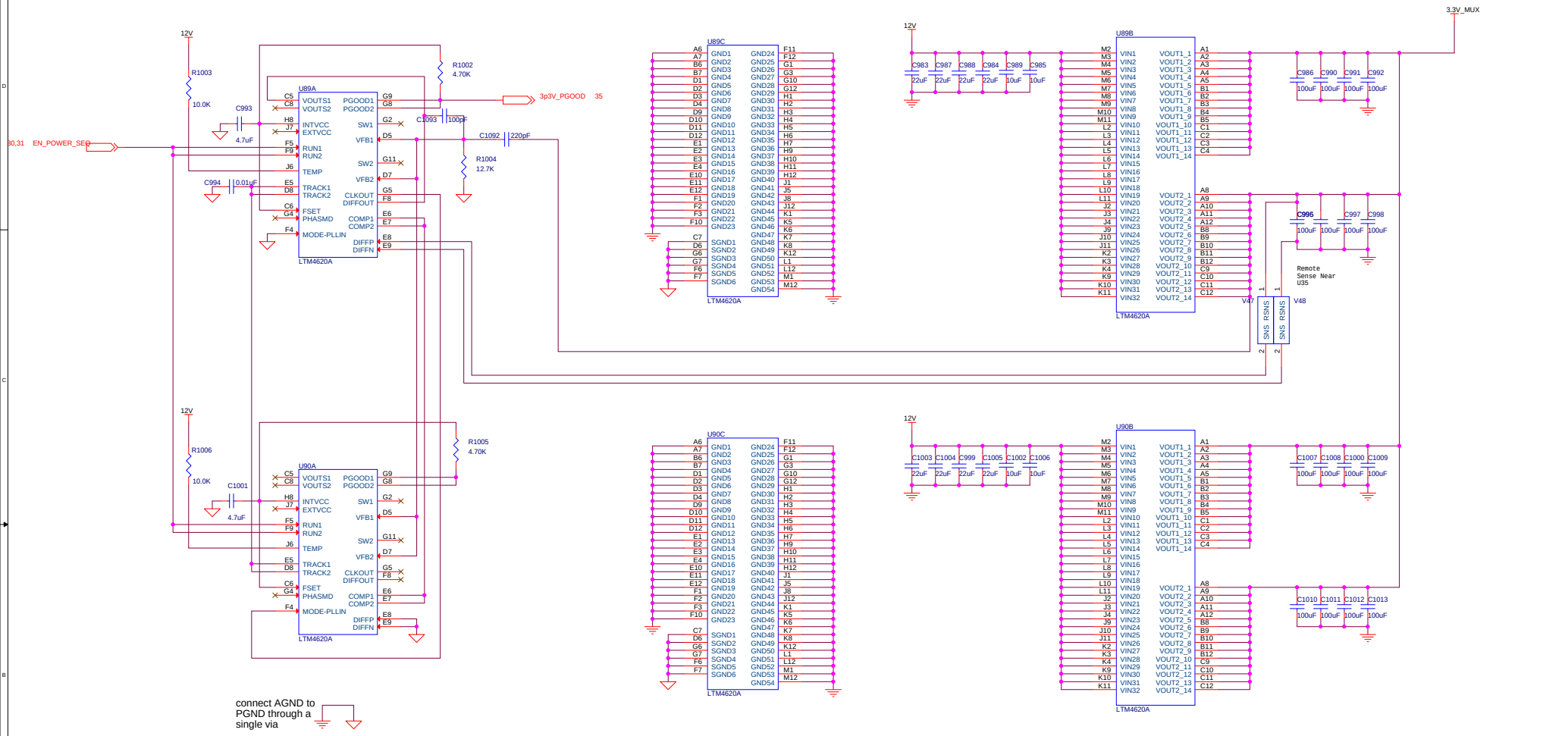
DC_IN -> 12V (Laptop Supply)	12V_PCIE ATX (2x4 ATX)	DC_IN_ATX (Voltage Selected by LTC4357)
12V	12V	12V from 12V_ATX_IN
12V	0V	12V from DC_IN->12V
0V	12V	12V from 12V_ATX_IN

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

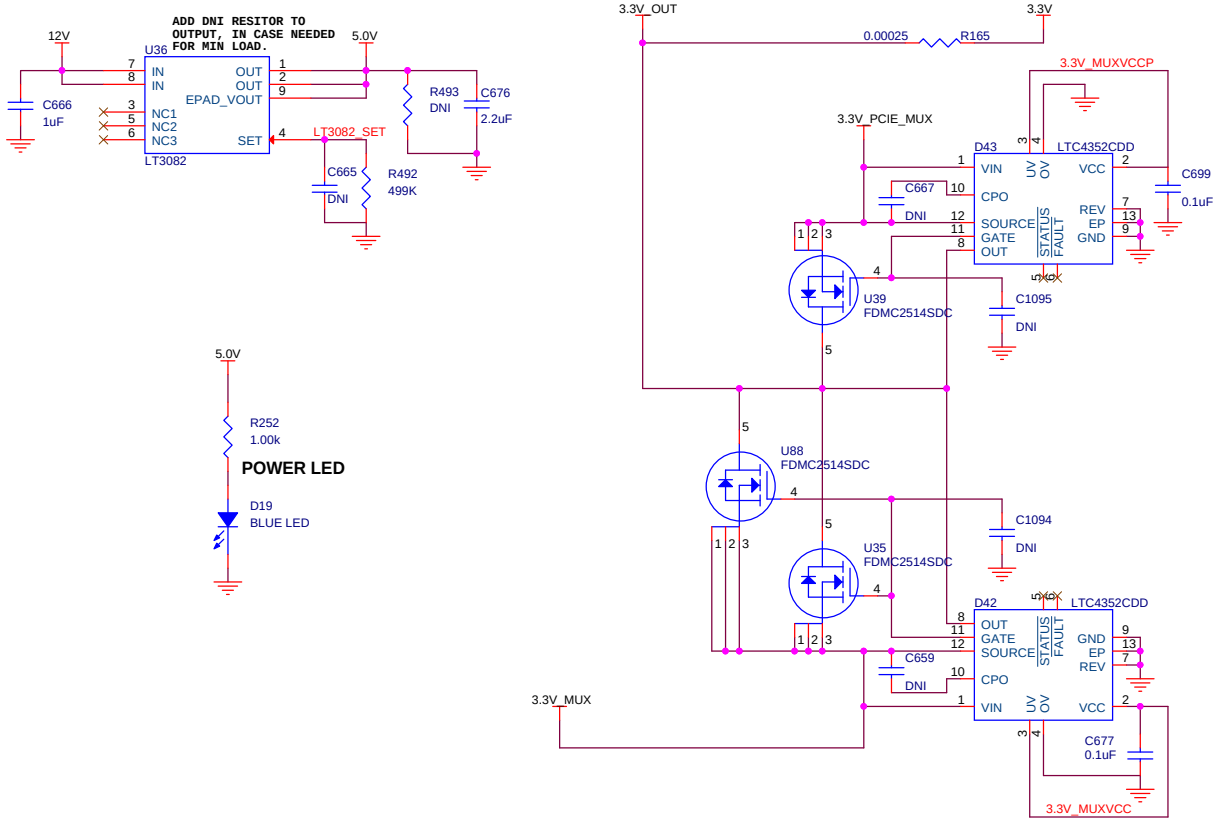
Date: Wednesday, August 10, 2016 Sheet 31 of 49

Power - 12V to 3.3V



Title	Arria 10 GX FPGA Development Kit	
Size C	Document Number 150-0321301-E3 (6XX-44366R)	Rev E3.1
Date: Wednesday, August 10, 2016	Sheet 32 of 49	

Power 1 - DC Input to 3.3V Output

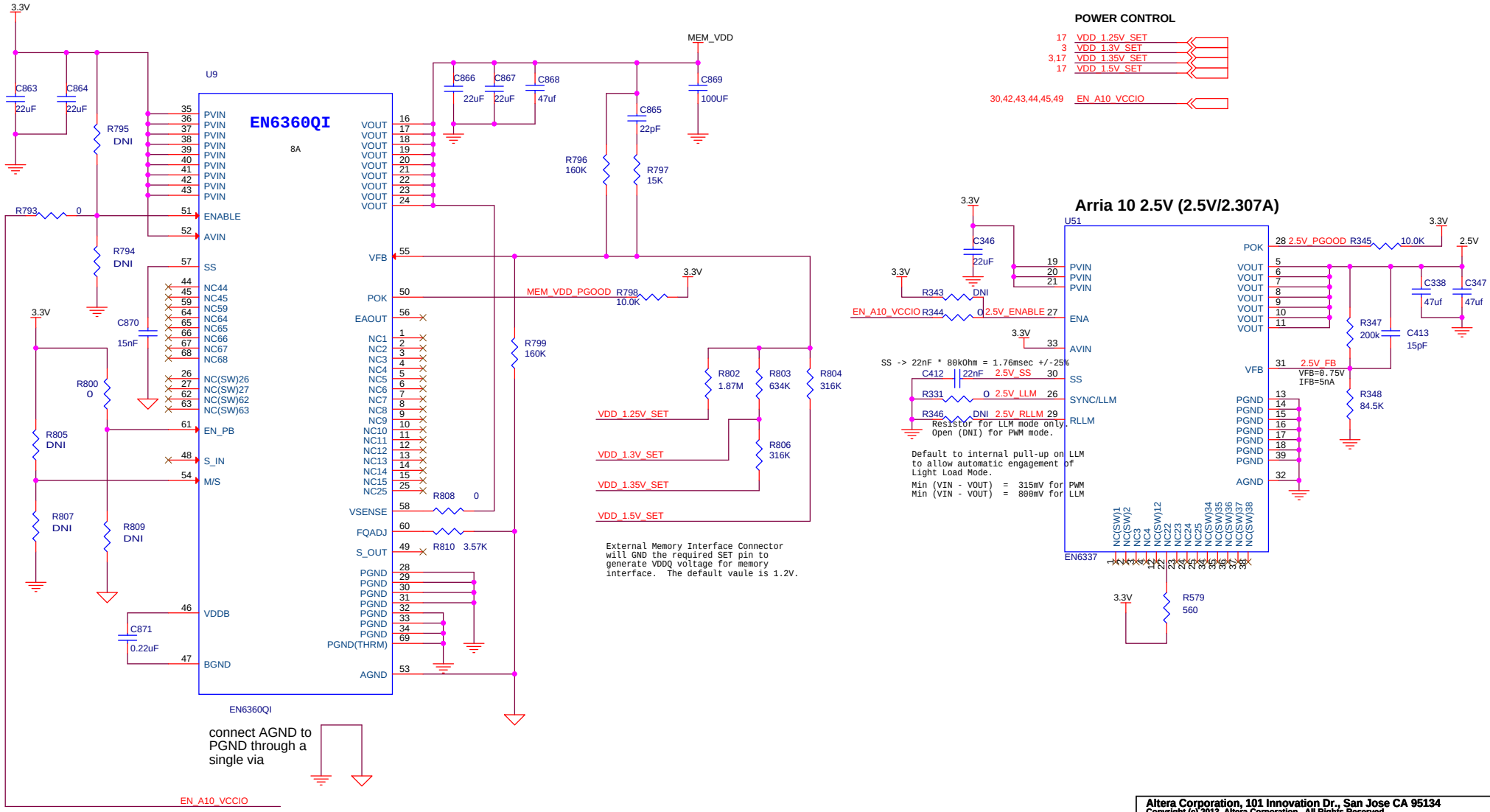


Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 33 of 49

Power - MEM_VDD, 2.5V

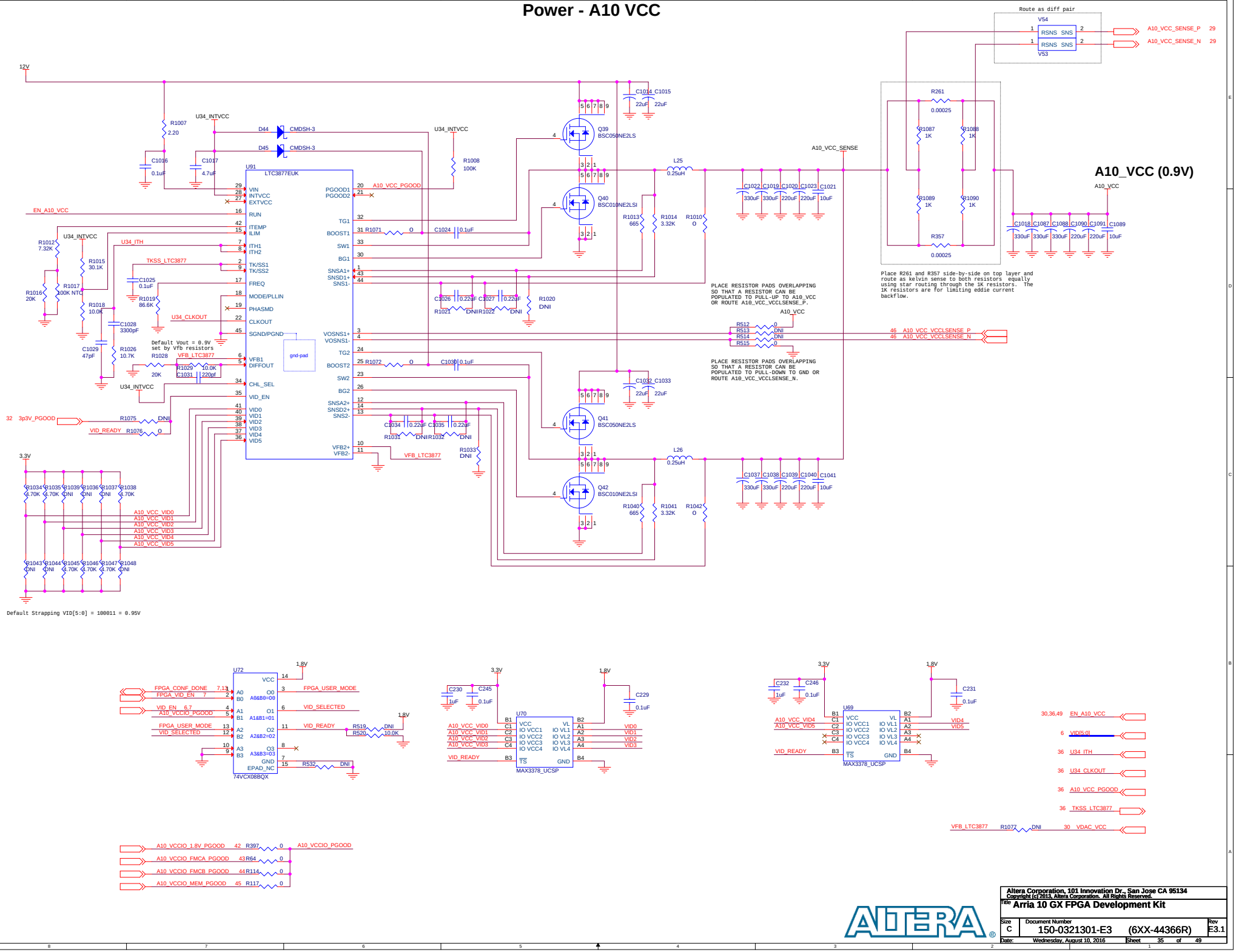


Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 34 of 49

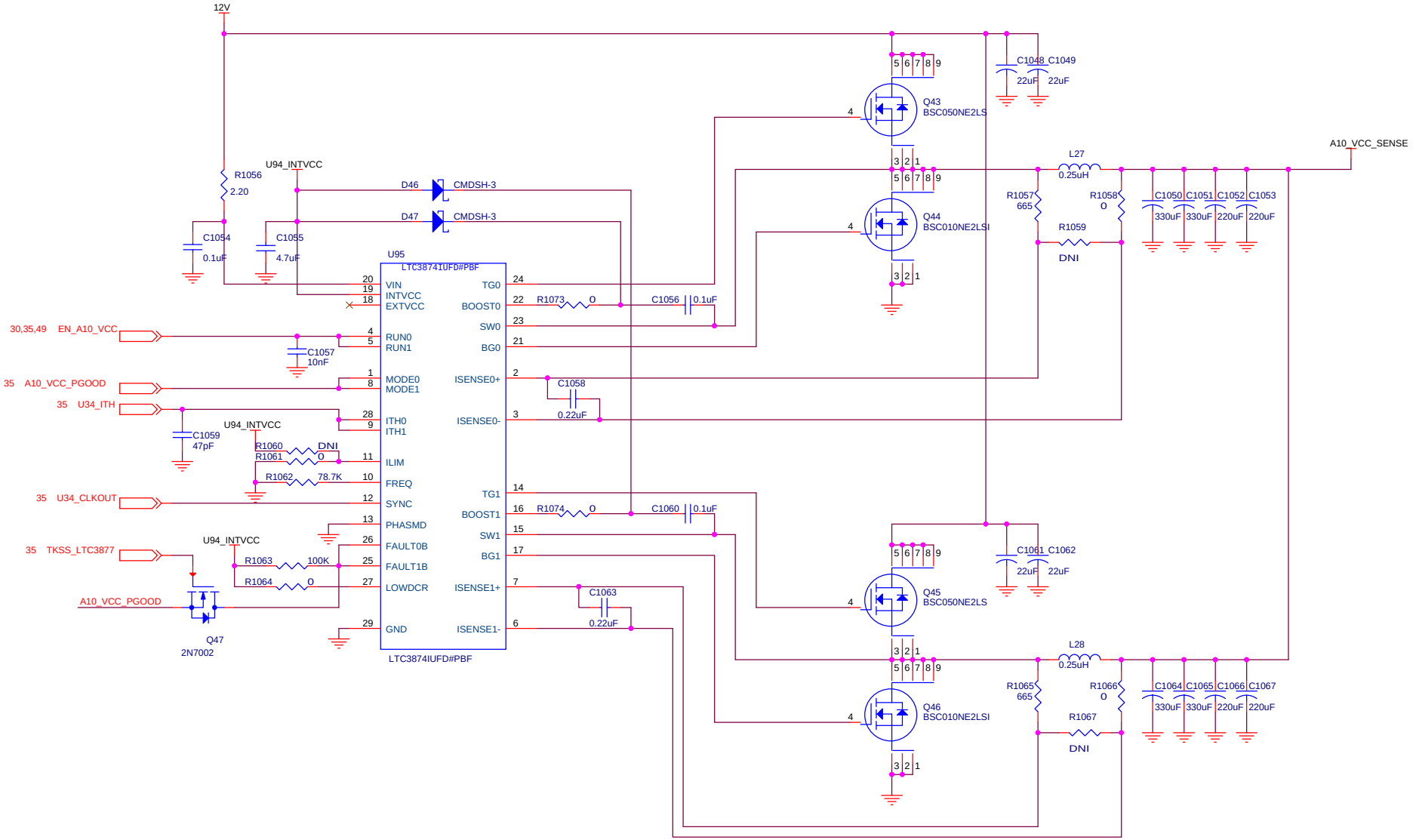
Power - A10 VCC



Altera Corporation, 101 Innovation Dr., San Jose CA 95134

Title	Arria 10 GX FPGA Development Kit	
Size C	Document Number 150-0321301-E3 (6XX-44366R)	Rev E3.1
Date: Wednesday, August 10, 2016	Sheet 35 of 49	

Power - A10 VCC



Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 36 of 49

This page intentionally left blank

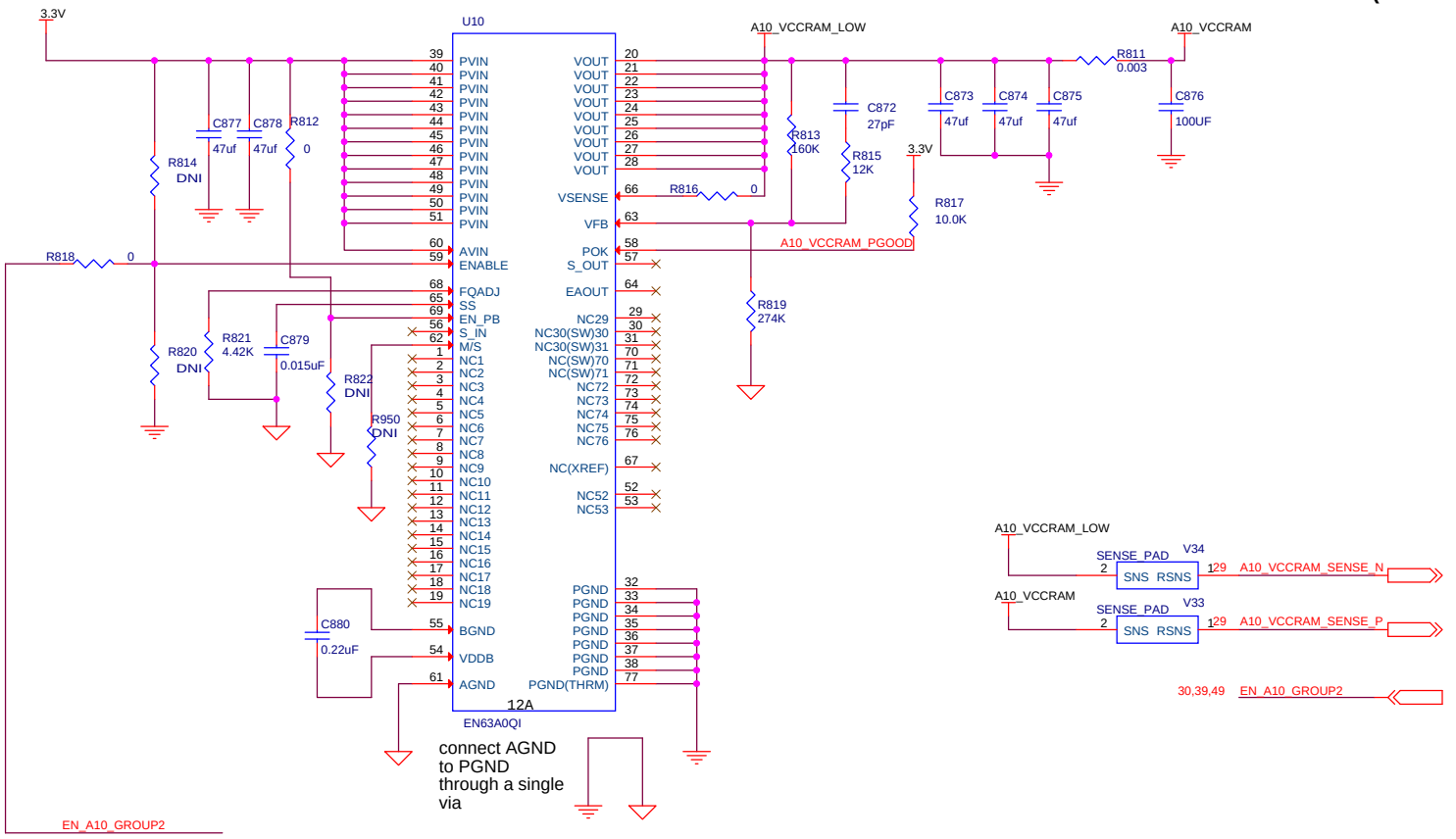
Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 37 of 49

Power - A10 VCCRAM

Arria 10 - VCCRAM (0.95V/5.117A)



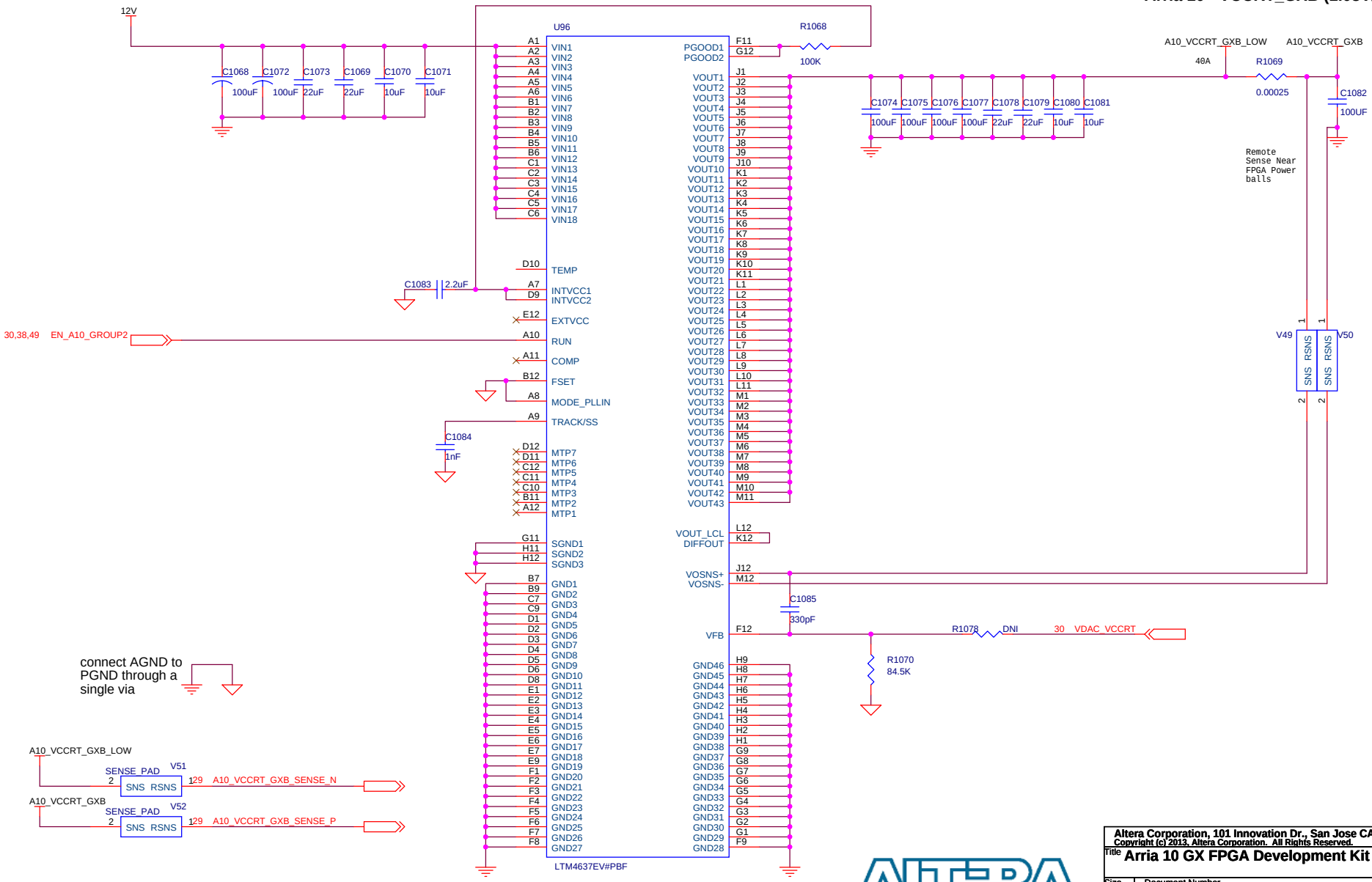
Title: **Arria 10 GX FPGA Development Kit**

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 38 of 49

Power - A10 VCCRT GXB

Arria 10 - VCCRT_GXB (1.03V/17A)



Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 39 of 49

This page intentionally left blank

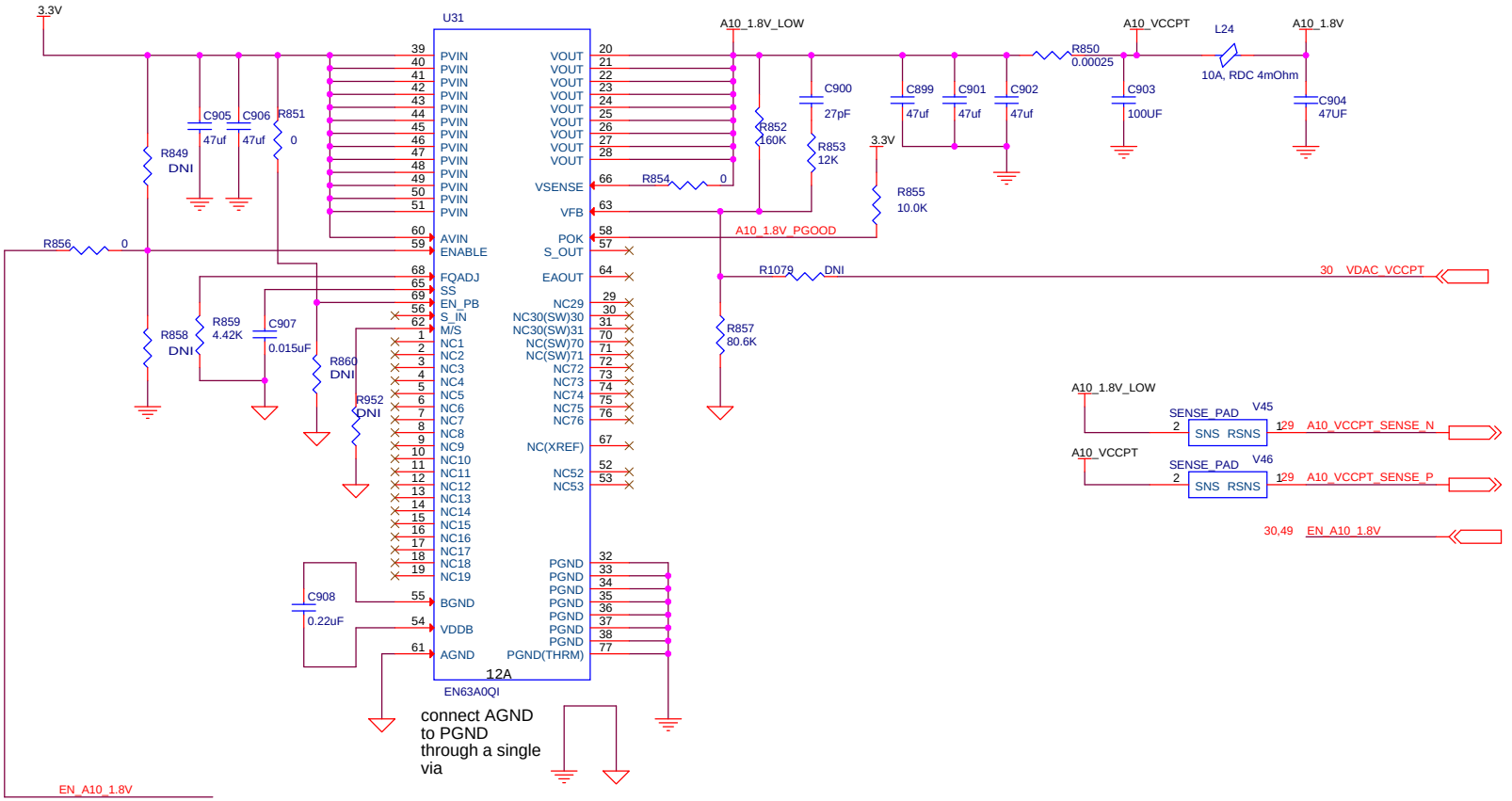
Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 40 of 49

Power - A10 VCCPT & 1.8V

Arria 10
VCCA_PLL, VCCH_GXB, VCCPT
(1.8V/10.229A)

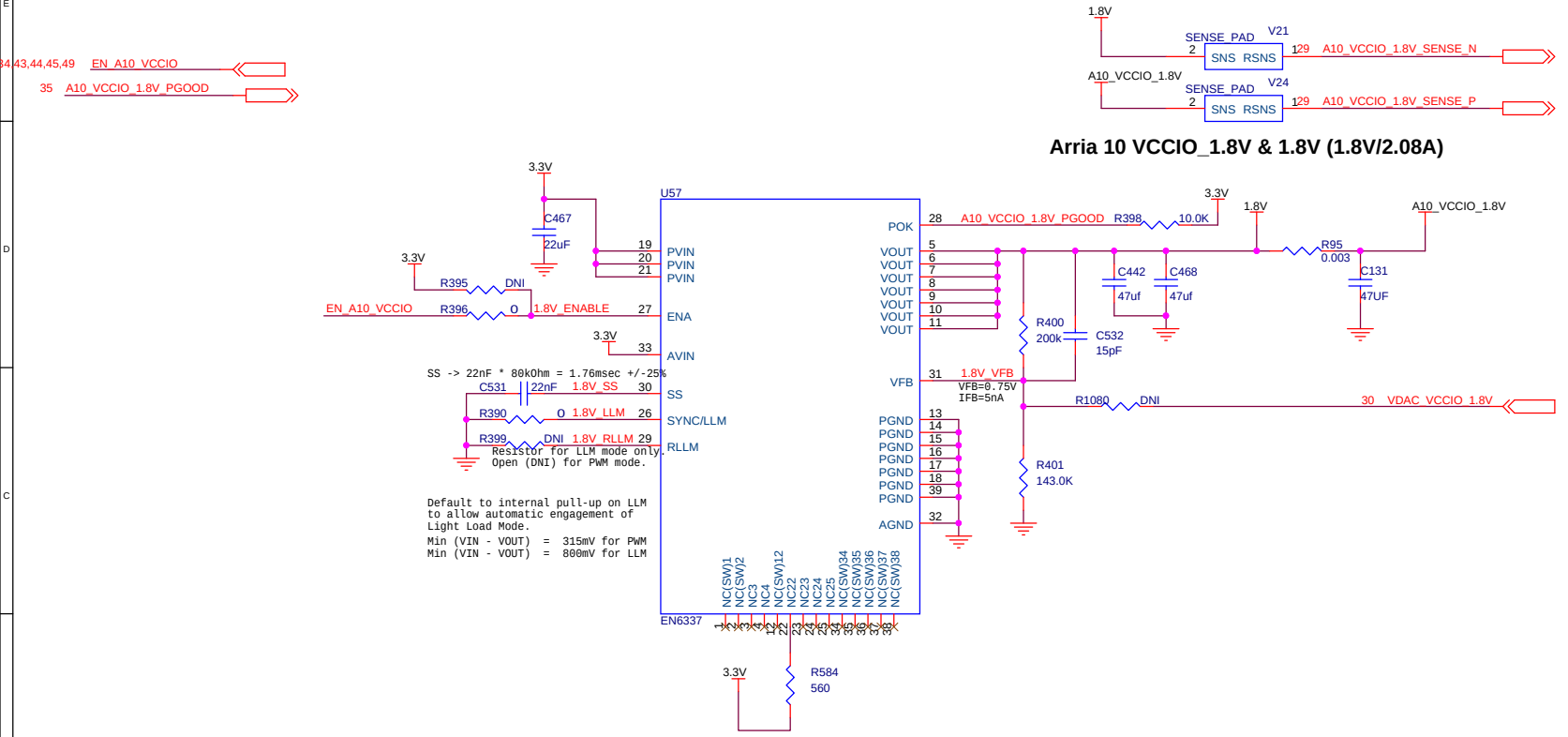


Title: **Arria 10 GX FPGA Development Kit**

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 41 of 49

Power - A10 VCCIO 1.8V



Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 42 of 49

Power - A10 VCCIO FMCA

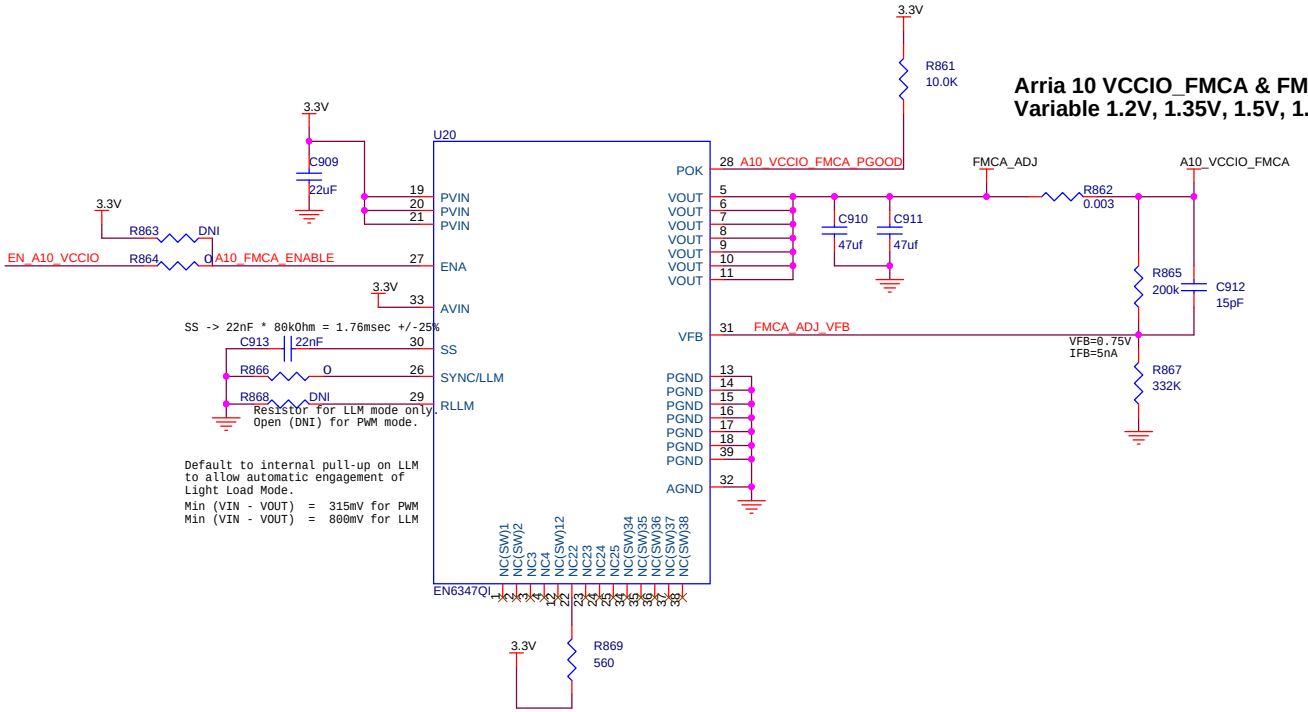
34,42,44,45,49 EN_A10_VCCIO

35 A10_VCCIO_FMCA_PGOOD

FMCA_ADJ — SENSE_PAD V37 (2) SNS RSNS (129) A10_VCCIO_FMCA_SENSE_N

A10_VCCIO_FMCA — SENSE_PAD V38 (2) SNS RSNS (129) A10_VCCIO_FMCA_SENSE_P

Arria 10 VCCIO_FMCA & FMCA_VADJ (1.2V/3.5A)
Variable 1.2V, 1.35V, 1.5V, 1.8V



Install only one

FMCA_ADJ_VFB
R1084 DNI R389 1M
R1085 DNI R394 499K
R1086 0 R409 249K

FMCA Voltage

Installed	VCCIO FMCA SELECT
NONE	1.2V
R1084	1.35V
R1085	1.5V
R1086 (Default)	1.8V

Title: Arria 10 GX FPGA Development Kit

Size: B | Document Number: 150-0321301-E3 (6XX-44366R) | Rev: E3.1

Date: Wednesday, August 10, 2016 | Sheet 43 of 49

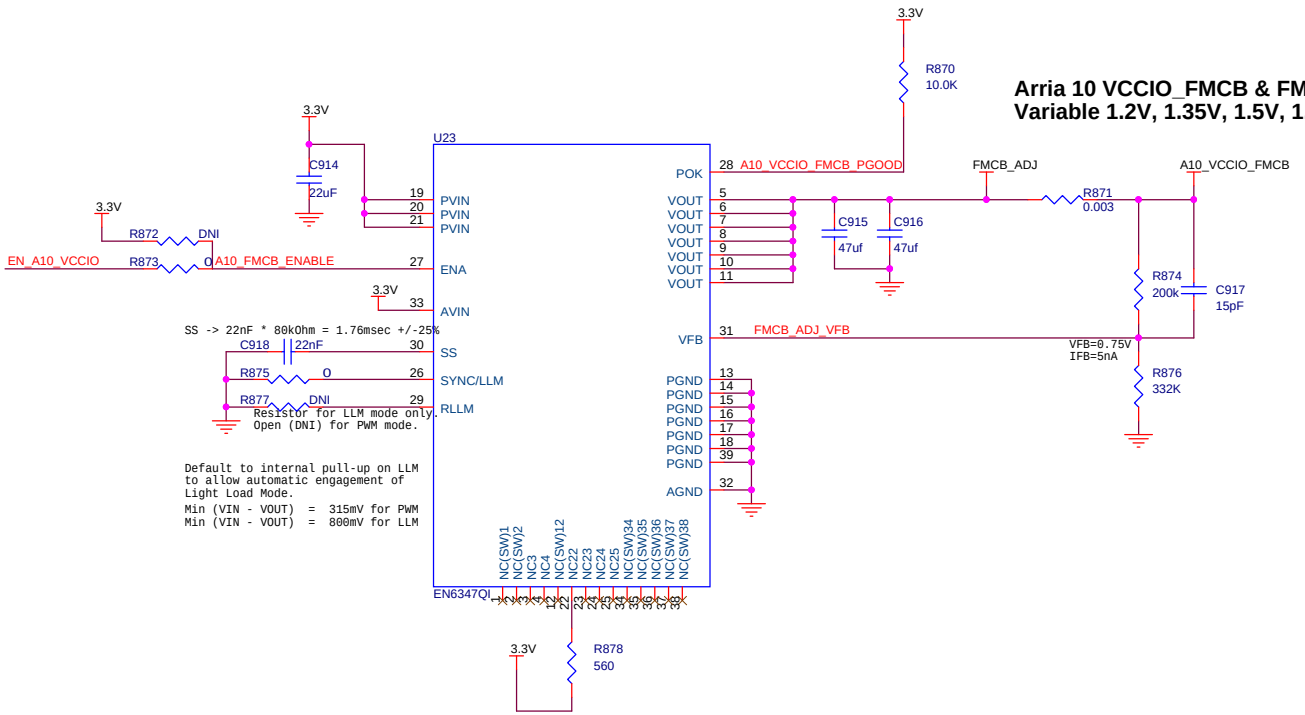
Power - A10 VCCIO FMCB

3,45,49 EN_A10_VCCIO

35 A10_VCCIO_FMCB_PGOOD

FMCB_ADJ — SENSE_PAD V42 — 2 SNS RSNS 1 — 29 A10_VCCIO_FMCB_SENSE_N

A10_VCCIO_FMCB — SENSE_PAD V41 — 2 SNS RSNS 1 — 29 A10_VCCIO_FMCB_SENSE_P



FMCA Voltage

Installed	VCCIO FMCB SELECT
NONE	1.2V
R1083	1.35V
R1082	1.5V
R1081 (default)	1.8V

Altera Corporation, 101 Innovation Dr., San Jose CA 95134

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 44 of 49

Power - A10 VCCIO MEM

POWER CONTROL

17 VDDQ_1.25V_SET
17 VDDQ_1.35V_SET
17 VDDQ_1.5V_SET
49 EN_A10_VCCIO
39 A10_VCCIO_MEM_PGOOD

MEM_VDDQ — SENSE_PAD 2 — V40 SNS RSNS 129 — A10_VCCIO_MEM_SENSE_N
A10_VCCIO_MEM — SENSE_PAD 2 — V39 SNS RSNS 129 — A10_VCCIO_MEM_SENSE_P

Arria 10 VCCIO_MEM & MEM_VDDQ (1.2V/4.7A)
Variable 1.2V, 1.25V, 1.35V, 1.5V

3.3V
C923 22uF
C924 22uF
R880 DNI
R883 0
R884 DNI
C926 15nF
R887 0
R888 DNI
R893 DNI
R894 DNI
C927 0.22uF

U24
EN6360QI
8A

35 PVIN
36 PVIN
37 PVIN
38 PVIN
39 PVIN
40 PVIN
41 PVIN
42 PVIN
43 PVIN
51 ENABLE
52 AVIN
57 SS
44 NC44
45 NC45
59 NC59
64 NC64
65 NC65
66 NC66
67 NC67
68 NC68
26 NC(SW)26
27 NC(SW)27
62 NC(SW)62
63 NC(SW)63
61 EN_PB
48 S_IN
54 M/S
46 VDDB
47 BGND

MEM_VDDQ
C919 22uF
C920 22uF
C921 47uf
R879 0.003
16 VOUT
17 VOUT
18 VOUT
19 VOUT
20 VOUT
21 VOUT
22 VOUT
23 VOUT
24 VOUT
55 VFB
50 POK
56 EAOUT
1 NC1
2 NC2
3 NC3
4 NC4
5 NC5
6 NC6
7 NC6
8 NC7
9 NC8
10 NC9
11 NC10
12 NC11
13 NC12
14 NC13
15 NC14
25 NC15
NC25
58 VSENSE
60 FQADJ
49 S_OUT
28 PGND
29 PGND
30 PGND
31 PGND
32 PGND
33 PGND
34 PGND
69 PGND(THRM)
53 AGND

A10_VCCIO_MEM
C922 100UF
C925 22pF
R881 160K
R882 15K
A10_VCCIO_MEM_PGOOD
R885 10.0K
R886 160K
R892 0
R895 3.57K
3.3V
R889 1.87M
R890 634K
R891 316K
VDDQ_1.25V_SET
VDDQ_1.35V_SET
VDDQ_1.5V_SET

External Memory Interface Connector will GND the required SET pin to generate VDDQ voltage for memory interface. The default vaule is 1.2V.

EN6360QI

connect AGND to PGND through a single via

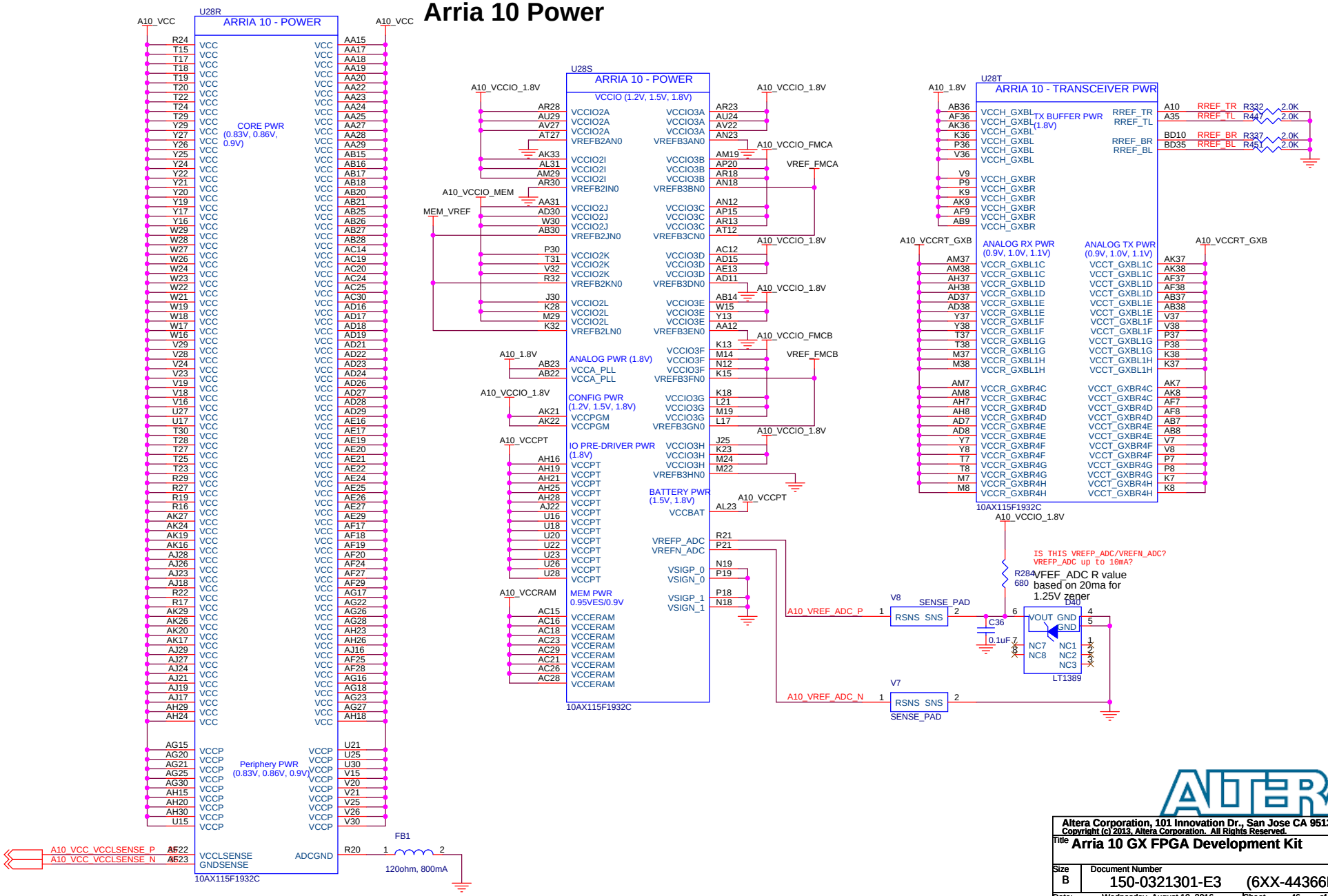
EN_A10_VCCIO

Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 45 of 49

Arria 10 Power

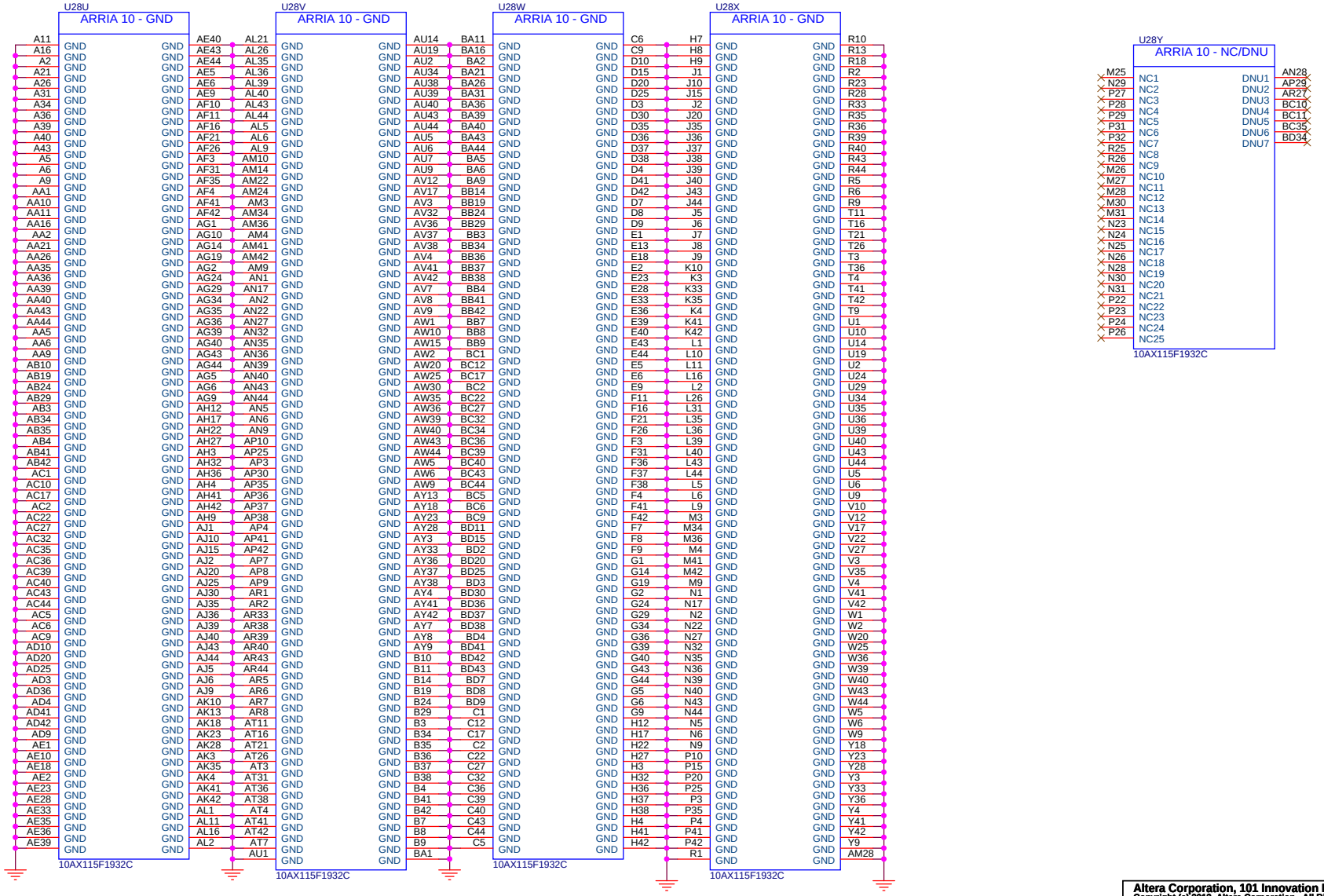


Title: **Arria 10 GX FPGA Development Kit**

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 46 of 49

Arria 10 Ground



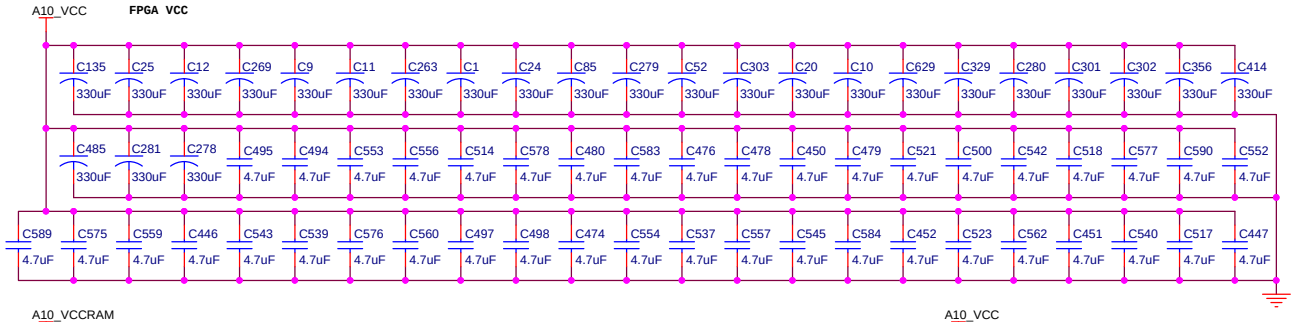
Title: **Arria 10 GX FPGA Development Kit**

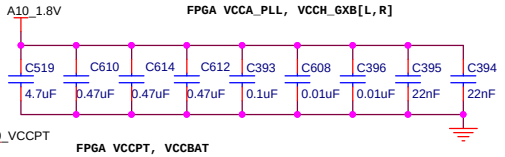
Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

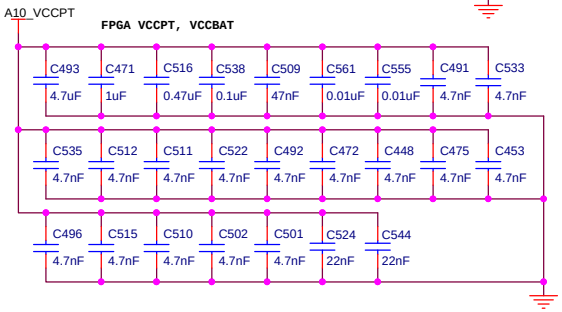
Date: Wednesday, August 10, 2016 Sheet 47 of 49

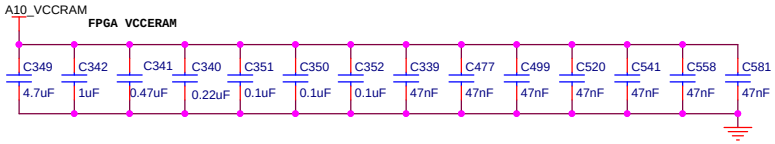
Decoupling

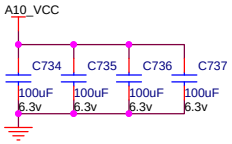
Do Not Copy. Decoupling requirements is design specific. Please use the Early Power Estimator and PDN Tool available on Altera.com to determine your specific decoupling requirements.

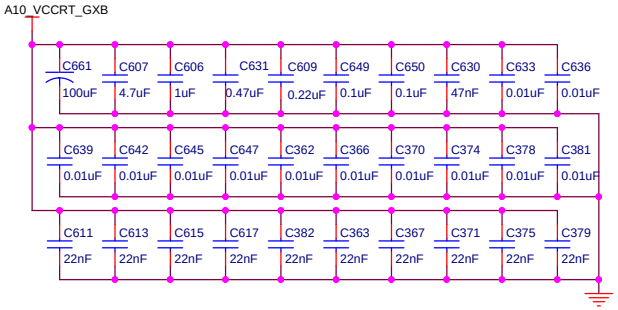


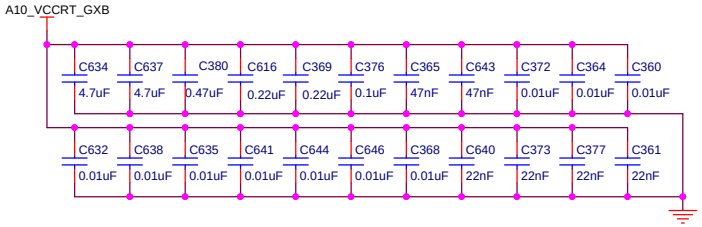


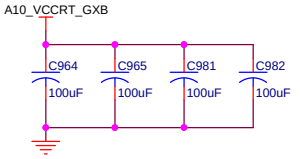


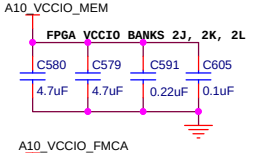


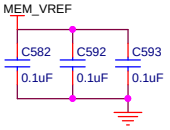


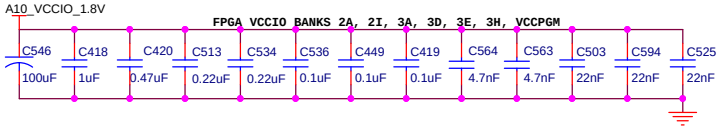


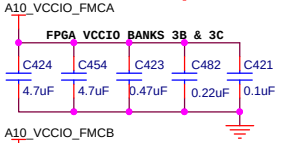


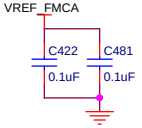


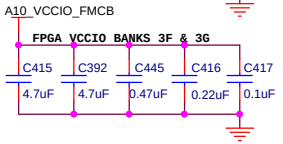


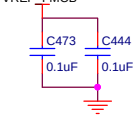


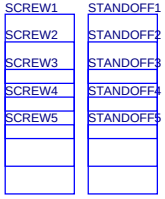












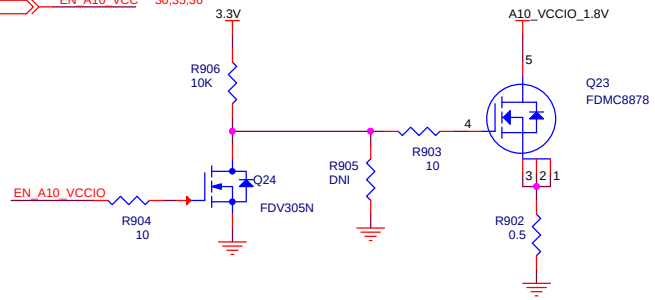
Title: Arria 10 GX FPGA Development Kit

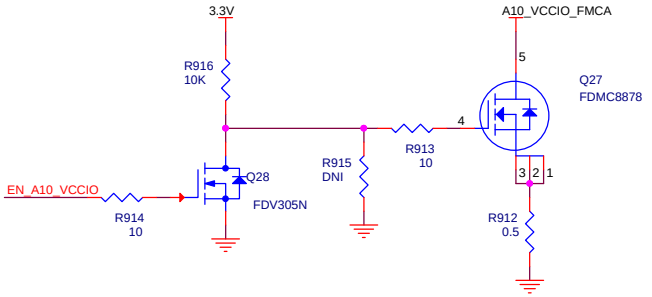
Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

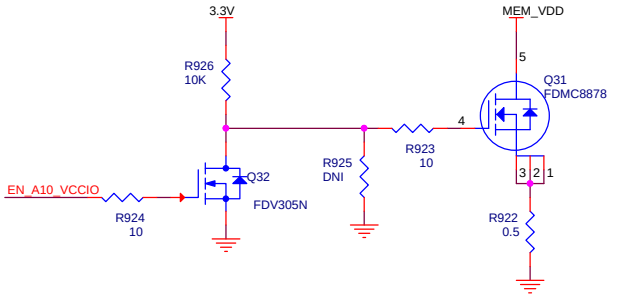
Date: Wednesday, August 10, 2016 Sheet 48 of 49

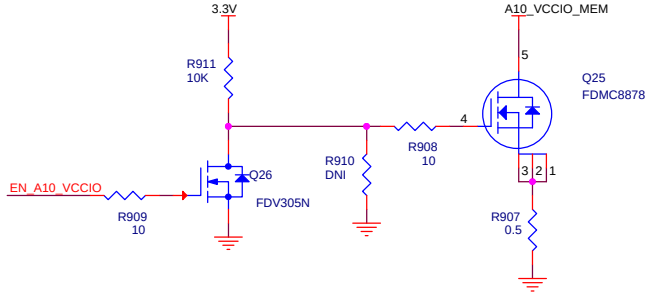
Power-down Fast Discharge

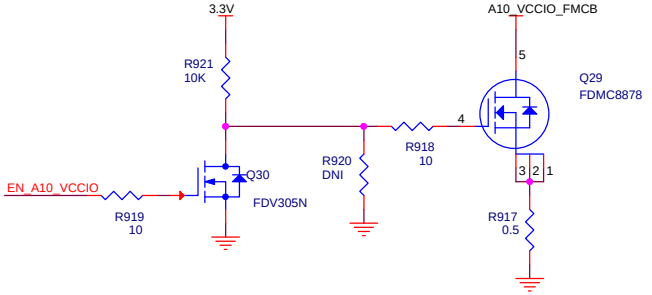
EN_A10_VCCIO 30,34,42,43,44,45
EN_A10_1.8V 30,41
EN_A10_GROUP2 30,38,39
EN_A10_VCC 30,35,36

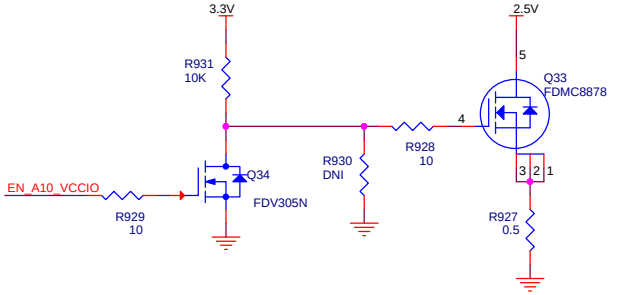


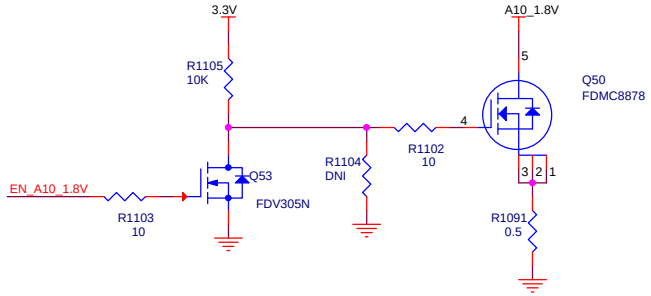


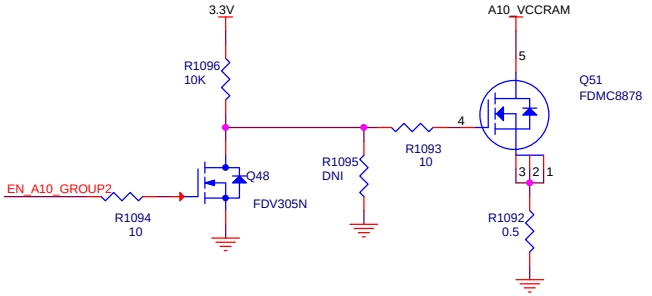


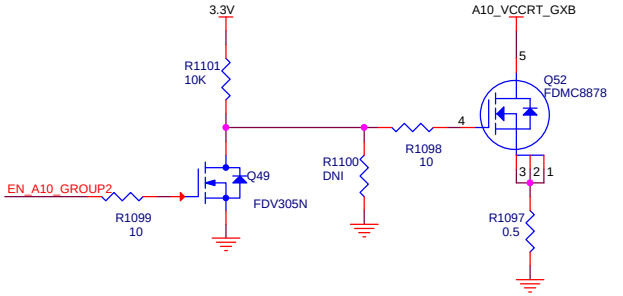


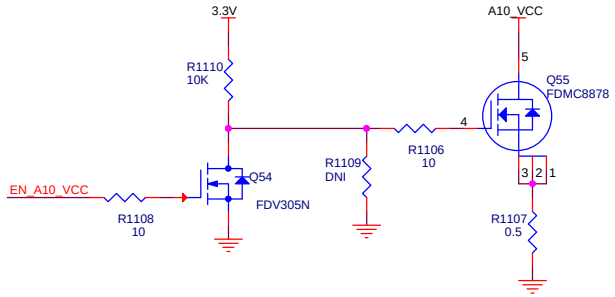












Title: Arria 10 GX FPGA Development Kit

Size	Document Number	Rev
B	150-0321301-E3 (6XX-44366R)	E3.1

Date: Wednesday, August 10, 2016 Sheet 49 of 49