AUTOMOTIVE
Paving the way to productivity

CONNECTIVITY
FUNCTIONAL SAFETY
MOTOR CONTROL
SENSOR FUSION
EMBEDDED VISION

FPGAs
SoCs

DESIGN TOOLS
AUTOSAR

IP
POWER MANAGEMENT

Q1 2017
For more than twelve years, Altera has been delivering AEC-Q100 qualified programmable logic devices (PLD), including MAX® CPLDs, Cyclone®, and MAX 10 family of FPGAs and SoCs, to our valued automotive OEM and Tier 1 customers. We understand the rigorous quality, reliability, and supply-chain requirements of our automotive customers and have implemented several programs to address these requirements, such as zero defect philosophy, continuous improvement, and product lifecycles of more than 15 years.

Why FPGA?

Market research indicates FPGAs and PLDs in automotive will grow at double digit compound annual growth rates (CAGR) over the next several years. Altera’s key automotive focus areas include some of the fastest growing segments in the industry, such as Infotainment and Driver Information, Advanced Driver Assistance System (ADAS), and E-Vehicle and Powertrain. Each of these application areas are undergoing a metamorphosis sparked by the proliferation of electronic content in vehicles and the associated megatrends driving them. Why the need for programmable logic in automotive? Three reasons: Scalability, flexibility, and raw performance. FPGAs are the only solution that are able to truly scale architectures from entry-level to luxury model vehicles by offering a wide range of logic densities, optional embedded ARM® cores and peripherals, and a single software development flow. This helps engineering managers and system designers get their products to market faster, more efficiently, and at a lower total cost of ownership, while maintaining the ability to make last minute tweaks prior to production launch.

Safety First

Functional safety has long been a key strategic imperative for us, and Altera was the first FPGA supplier to achieve IEC 61508 functional safety certification1 for the industrial market. That early commitment and investment has put us in a leading position to execute on our ISO 26262 functional safety plan for automotive applications. The Cyclone V SoC safety manual (automotive functional safety data pack) and device level FMEDA are available now, and the full qualification to ISO 26262 is expected by mid-2015. Altera is an active member of the ISO 26262 working group and our functional safety manager co-chairs the ISO 19451 PLD sub-group, which helps to drive PLD requirements into the 2nd edition of the ISO 26262 standard.

Get to Market Faster

Altera's total solution offering helps our customers go from proof-of-concept to production in the shortest possible time. How? By complementing our silicon with best-in-class development tools to help software and hardware engineers port their designs to FPGA or create new ones from the ground up. We've got you covered whether it’s industry standards like Open Computing Language (OpenCL™), AUTOSAR, Altera's own Quartus® II development tool, or complementary solutions such as DSP Builder that bridge between Quartus II software and MATLAB/Simulink. Many of our design tools and methodologies have been certified by TÜV Rheinland to ensure the highest level of quality, integrity, and safety. Lastly, every programmable logic device requires power management and Altera is the only FPGA supplier to offer optimized power management solutions. Altera's Enpirion® power management products deliver the industry’s first family of PowerSoC DC-DC converters featuring integrated inductors. They provide an industry-leading combination of high-efficiency, small-footprint, and low-noise performance in an integrated product. Unlike discrete power products, these turnkey solutions give designers complete power systems that are fully simulated, characterized, and production qualified. With our new AEC-Q100 qualified Enpirion PowerSoCs, automotive system designers can now leverage both power management and programmable logic from a single trusted supplier. Altera is here to help you deliver a total proven solution on time.

1 Certified by TÜV Rheinland
Advanced Driver Assistance Systems

Our FPGAs can help you keep pace with the rapid advancements in driver assistance technology and address the key challenges you face, including:

- Running multiple ADAS algorithms in parallel in a single low-cost SoC
- Delivering a scalable, low-cost solution tailored to address the requirements of different vehicle models
- Leveraging your intellectual property (IP) investments across multiple products
- Operating within the power and thermal limits of small camera modules without active cooling
- Incorporating new features to differentiate your products in the market

Our FPGAs provide an ideal platform for developing high-performance, low-power, low-cost ADAS systems with the optimal level of integration and flexibility. You can incorporate changes late in the design cycle and deploy in-field upgrades that let you differentiate your products and keep pace with your customers’ expectations.

Benefits of Altera FPGAs in ADAS Applications

- Parallel-processing architecture to run multiple ADAS algorithms simultaneously
- Scalability and differentiation, which allows you to include the latest features that can be deployed into all vehicle platforms
- Increased productivity using software-based design methodologies with open standards like OpenCL and model-based design using MATLAB and DSP Builder
- Simplified software development with an AUTOSAR-compliant MCAL layer developed using an ASIL-B methodology supported in our Cyclone V SoCs
- Ability to deliver the highest performance/watt vs. CPU, graphics processing unit (GPU), and ASSP devices
- Flexibility to be used as either the main processing device or a companion FPGA to offload high-performance processing tasks and incorporate new features

FPGA Applications

- Forward, surround-view cameras
- 77-79 GHz digital radar
- V2X communications
- Radar and video sensor fusion

Cyclone V SoC Development Resources

- OpenCL-based design flow
- MATLAB to DSP Builder model-based design
- AUTOSAR v4.0.3 MCAL
- ISO 26262 functional safety data package

Forward Camera Sensor Fusion

Cyclone V SoC

HD Cameras

Parallel or Serial

LVDS

77GHz Radar

Image Sensor Pipeline

Sensor Fusion

Analytics & Decision Making

Radar Sensor Processing

ARM Cortex-A9 CPU x 2

Vehicle Network

CAN Controller

DDR Memory

x32 with ECC

Hard IP

Soft IP

Vehicle Network
INFOTAINMENT

Automotive infotainment systems are an integral part of modern vehicle design and greatly influence global vehicle sales. You need to continually create compelling new technology that both rivals and complements the latest consumer devices while keeping up with the pace of product obsolescence common in consumer electronics.

It is important to select the right main system processor to differentiate the system’s user interface with the latest graphics. Should you choose a high-performance SoC with a GPU or a CPU with applications that can be upgraded with software? With multiple models to support, you may need to select several different SoCs due to system variations and emerging interfacing technologies. This is neither cost effective nor efficient usage of engineering resources.

By using our FPGAs as an I/O companion, you can support any combination of I/O interfaces. You may also leverage the FPGA as an efficient coprocessor to offload functions from your host main processor such as video scaling and graphics acceleration. With an FPGA, your system becomes easily scalable, enabling you to upgrade firmware on the fly to support multiple manufacturers, regions, and models with minimum changes to the hardware.

BENEFITS OF ALTERA FPGAS IN INFOTAINMENT APPLICATIONS

- Support multiple camera inputs in any bit rate or resolution via video select and front-end processing
- Support multiple display interfaces and offloads GPU
- Optimize system performance by integrating 2D/3D graphic accelerator, scalar, image enhancer, and interface protocol bridge
- Reduce cost by integrating radio digital signal processing (DSP) into FPGA with software-based radio IP
- Accelerate time to market by supporting the latest generation of interface standards in programmable logic
- Minimize PCB spins and future-proof your system with in-field upgrades to the FPGA

Pre and Post Video Processing Video Companion Application

* Embedded Display Port
ELECTRIC VEHICLES AND POWERTRAIN

The introduction of hybrid-electric vehicles (HEV) and electric vehicles (EV) have enabled breakthrough innovations and greater efficiency in electric motor controls, power conversion, and battery management systems.

The algorithms driving these systems require continuous upgrades and design changes to optimize performance. ASIC development cycles are too long to meet these market demands and microcontroller units (MCUs) are unable to keep up with performance requirements. Our FPGAs deliver hardware failsafe logic for insulated gate bipolar transistor (IGBT) bridge protection, efficient motor control with our model-based DSP Builder design flow, and hardware acceleration with faster control loops to improve energy efficiency, reduce noise, and improve reliability of electrical motors.

You can use FPGAs or CPLDs anywhere DSP is needed to improve system performance, such as the AC/DC converters, DC/DC converters, battery management systems, and motor inverter systems.

To accelerate your time to market and increase productivity, Altera and its partner network offer a variety of IP and tools. Our motor control IP includes pulse-width modulation (PWM), analog-to-digital (ADC) and digital encoder interfaces, and integrated customizable field-oriented control (FOC) reference designs.

** BENEFITS OF ALTERA FPGAS IN HEV/EV APPLICATIONS **

- Improve system performance by using hardware co-processor to accelerate your motor control algorithm
- Shorten design cycles with model-based design tools, safety methodology, and pre-qualified devices
- Designed for functional safety with IEC 61508-certified design tools, IP, and products (ISO 26262 certification expected mid 2015 for Cyclone V SoC)
- Low latency and fast response in FPGA logic for motor control loops

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**HEV/EV System**

![HEV/EV System Diagram]

- **Charger**
- **AC/DC Converter**
- **Battery Management Unit**
- **Cell Monitoring Unit**
- **Battery Cell Module**
- **CAN, LIN, FlexRay, etc**

**FPGA application**
As automotive digital content and control systems move to high definition, wireless communication, and multi-gigabit bandwidths, automakers and system OEMs will continue to demand top-notch quality semiconductor devices. With tens of millions of programmable logic devices shipped to automotive customers worldwide since 2003, we are well positioned for high-volume automotive production.

As an active member of the Automotive Electronics Council (AEC), Altera has chaired two AEC subcommittees and qualifies all of its automotive or “A” grade products to the AEC-Q100 standard. Our production part approval process (PPAP) includes the AEC-Q100 qualification results in the document package we provide to qualify your products. The PPAP provides the baseline product details including die, package, wafer fabrication process, package assembly process, and constituent materials.

We have a zero-defect philosophy, with rigorous procedures at each phase of development to ensure the highest quality and lowest defective parts per million (DPPM). Our wafer fabs, package, assembly, test, and programming facilities are TS-16949 certified for a quality management system that provides for continual improvement, emphasizes defect prevention, and reduces variation and waste in the supply chain.

We take business continuity planning (BCP) seriously and employ several initiatives to ensure you have a continuous supply of product, including use of six fabs across four locations, dual fab strategy by Fabmatch methodology, multiple assembly site sourcing, and sub-material sourcing control.

We understand that you need to support your products and vehicles for a minimum of 10 years after release. Our average product cycle is 15 years, with many of our products having lifetimes in excess of 20 years, so you can design in our products with confidence. When change is absolutely mandatory, we take exceptional care to provide special product change notifications so you can manage the delicate rollout of changes to your customers—the automakers—in a coordinated and well-orchestrated manner.
OpenCL enables FPGAs to be programmed in a C-like language instead of the traditional register transfer level (RTL) programming language. This enables FPGAs to be more accessible to software engineers who traditionally do not use RTL and are more familiar with C-based languages. Using this methodology, software engineers can now target FPGAs to increase performance and flexibility over CPU or GPU-based systems while using significantly less power. This combination of increased performance, flexibility and reduced power is ideal for automotive designs that require semiconductor devices to process huge volumes of data in an energy-efficient fashion. OpenCL design is supported today in Altera’s automotive qualified Cyclone V SoC family.

SAFETY FIRST! ALTERA’S LEADERSHIP IN FUNCTIONAL SAFETY EXPANDS TO ISO 26262

The automotive industry is adding multiple active safety systems to reduce the risk of injury and harm. Adapted from the IEC 61508 functional safety standard, the ISO 26262 automotive electronic system safety standard helps you avoid systematic faults and also detect, control, and mitigate any random hardware faults that may cause a malfunction of the system.

To simplify and speed up your certification process, we are working with TÜV Rheinland, an independent third-party assessor specializing in functional safety testing and certification, to receive qualification to ISO 26262. Altera is the first FPGA supplier whose FPGA devices, diagnostics IP, development tools, and FPGA design flow are all certified for the IEC 61508 functional safety standard. Our Functional Safety Data Pack (FSDP) typically saves customers 12-18 man months in certifying their safety applications.

Altera’s Cyclone V SoC family will be the first family qualified for ISO 26262 with our Automotive Functional Safety Data Pack (AFSDP). A detailed safety manual and general FMEDA application note are available now to start your design along with a suite of diagnostics IP. Additionally, we are developing a...
detailed FMEDA calculator tool to support required hardware architectural metric calculations. Audit and certification are scheduled for mid-2015.

Altera's functional safety approach is a holistic one, which provides guidance in methodology, backed up with qualified tools that increase your tool confidence and may eliminate the use of redundant tool chains. Next, we offer a safety-ready suite of diagnostics IP and expert technical support along with our certified PLDs. Functional safety documentation, reliability reports, and our TÜV certificate will assist you in the certification of your systems. Safety first!

For additional details on our ISO 26262 functional safety program, please visit:

COMON AUTOMOTIVE IP – ALTERA AND PARTNER

Altera and its partners offer a broad portfolio of off-the-shelf, configurable IP cores for our devices. This pre-validated IP can help you further accelerate your design flow. Examples include:

INTERFACE IP

<table>
<thead>
<tr>
<th>Connectivity</th>
<th>Provider(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAN</td>
<td>Bosch, CAST, IFI</td>
</tr>
<tr>
<td>LIN</td>
<td>Bosch, CAST</td>
</tr>
<tr>
<td>FlexRay</td>
<td>Bosch</td>
</tr>
<tr>
<td>DisplayPort / eDP</td>
<td>Altea / Bitec</td>
</tr>
<tr>
<td>PCI Express® (PCIe®)</td>
<td>Altea - MegaCore® function</td>
</tr>
<tr>
<td>OpenLDI</td>
<td>Altea - megafunctiion</td>
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</table>

GRAPHICS IP

<table>
<thead>
<tr>
<th>Function</th>
<th>Provider(s)</th>
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</thead>
<tbody>
<tr>
<td>Video and Image Processing suite: scaler, converters, Alpha Blender, and more</td>
<td>Altea</td>
</tr>
<tr>
<td>2D/3D Graphics, HMI, Video I/O</td>
<td>TES</td>
</tr>
<tr>
<td>Video and graphics</td>
<td>Imagem Technology</td>
</tr>
<tr>
<td>DisplayPort / eDP</td>
<td>Altea / Bitec</td>
</tr>
<tr>
<td>Video codec</td>
<td>CAST</td>
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</table>

<table>
<thead>
<tr>
<th>FAMILY / DENSITY</th>
<th>PART NUMBER</th>
<th>IMAGE</th>
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<tbody>
<tr>
<td>Cyclone V SX SoC</td>
<td>DK-DEV-5CSXC6N/ES</td>
<td></td>
</tr>
<tr>
<td>Dual-core ARM Cortex®-A9 processor, 110K LE, 3 Gbps Transceiver</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cyclone V GT</td>
<td>DK-DEV-5CGTD9N</td>
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</tr>
<tr>
<td>301K LE, 5 Gbps Transceiver</td>
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<td></td>
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<tr>
<td>Cyclone V E</td>
<td>DK-DEV-5CEA7N</td>
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<tr>
<td>149K LE</td>
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<td></td>
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<tr>
<td>Cyclone IV GX</td>
<td>DK-DEV-4CGX150N</td>
<td></td>
</tr>
<tr>
<td>149.8K LE, 3 Gbps Transceiver</td>
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<tr>
<td>Cyclone IV GX Starter</td>
<td>DK-START-4CGX15N</td>
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<tr>
<td>14.4K LE, 2.5 Gbps Transceiver</td>
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<tr>
<td>MAX 10</td>
<td>DK-DEV-10M50-A</td>
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<tr>
<td>50K LE, ADC</td>
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<td></td>
</tr>
<tr>
<td>MAX 10</td>
<td>EK-10M08E144ES</td>
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<tr>
<td>8K LE, ADC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MAX V</td>
<td>DK-DEV-5M570ZN</td>
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</tr>
<tr>
<td>570 LE</td>
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</tr>
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</table>
Automotive-Grade Products

Our automotive-grade devices feature junction temperature support from -40°C to +125°C (or higher on selected devices). These devices meet or exceed ISO 9001:2001 and AEC-Q100 standards. All our automotive-grade devices are manufactured at fully TS-16949-registered/certified sites using some of programmable logic industry’s smallest, highest reliability, and mainstream semiconductor fabrication processes. Our automotive-grade portfolio spans CPLDs to FPGA and also includes SoCs as well as power management PowerSoCs.

Introducing the Cyclone V SoC

The Cyclone V SoC integrates an ARM-based hard processor system (HPS) with our FPGA fabric. These user-customizable SoCs increase system performance, lower power consumption, and reduce board space requirements, all designed to help you lower your overall system cost.

Cyclone V SoC key features:
- AEC-Q100 automotive-grade options
- Dual-core ARM Cortex - A9 processors, 700MHz
- Vertical and horizontal migration
- 3 Gbps and 5 Gbps transceiver options
- Hard IP: Dual CAN, Dual EMAC, Dual PCIe
- Safety ready - Error correction code (ECC) support

**Cyclone V SoC Package / Maximum User I/O Matrix**

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

<table>
<thead>
<tr>
<th>FAMILY</th>
<th>PRODUCT LINE</th>
<th>LOGIC DENSITY (K LES)</th>
<th>PLL FPGA/HPS (COUNT)</th>
<th>PACKAGE TYPE/PIN COUNT</th>
<th>BALL SPACING (MM)</th>
<th>DIMENSIONS (MM)</th>
<th>FPGA I/O / PROCESSOR I/O / LVDS I/O / TRANSCEIVERS (XCVR COUNT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclone V SE SoC</td>
<td>SCSE-A2</td>
<td>25</td>
<td>5 / 3</td>
<td>66 151 15 18</td>
<td>UBGa-484 (U19)</td>
<td>0.8</td>
<td>19 x 19</td>
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<tr>
<td></td>
<td>SCSE-A4</td>
<td>40</td>
<td>5 / 3</td>
<td>66 151 15 18</td>
<td>UBGa-672 (U23)</td>
<td>0.8</td>
<td>23 x 23</td>
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<tr>
<td></td>
<td>SCSE-A5</td>
<td>85</td>
<td>6 / 3</td>
<td>66 151 15 18</td>
<td>FBGA-896 (F31)</td>
<td>1.0</td>
<td>31 x 31</td>
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<tr>
<td></td>
<td>SCSE-A6</td>
<td>110</td>
<td>6 / 3</td>
<td>66 151 15 18</td>
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<td></td>
<td></td>
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<tr>
<td>Cyclone V SX SoC (3 Gbps)</td>
<td>SCSX-C2</td>
<td>25</td>
<td>5 / 3</td>
<td>66 151 15 18</td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td>SCSX-C4</td>
<td>40</td>
<td>5 / 3</td>
<td>66 151 15 18</td>
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<tr>
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<td>6 / 3</td>
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<tr>
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<td>SCSX-C6</td>
<td>110</td>
<td>6 / 3</td>
<td>66 151 15 18</td>
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<td></td>
<td></td>
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<tr>
<td>Cyclone V ST SoC (5 Gbps)</td>
<td>SCST-D5</td>
<td>85</td>
<td>6 / 3</td>
<td>66 151 15 18</td>
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<td></td>
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<tr>
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<td>SCST-D6</td>
<td>110</td>
<td>6 / 3</td>
<td>66 151 15 18</td>
<td></td>
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</tr>
</tbody>
</table>

AEC-Q100 Package options available with automotive-grade variants.
Altera's Cyclone V FPGAs provide the industry's lowest system cost and power, along with performance levels that make the device family ideally suited for differentiating your high-volume applications.

**Cyclone V FPGA key features:**
- Up to 40% power savings over prior generation
- Vertical migration across logic densities
- 3 Gbps and 5 Gbps transceiver options
- PCIe interface (hard IP)
- Memory controller (hard IP)
- Variable-precision DSP blocks
- 4 to 8 Phase-locked loop (PLL)

### CYCLONE V PACKAGE / MAXIMUM USER I/O MATRIX

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

<table>
<thead>
<tr>
<th>FAMILY</th>
<th>PRODUCT LINE</th>
<th>LOGIC DENSITY (K LEs)</th>
<th>PLL (COUNT)</th>
<th>BALL SPACING (MM)</th>
<th>DIMENSIONS (MM)</th>
<th>I/OS / LVDS / TRANSCEIVERS (COUNT)</th>
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<tr>
<td>CYCLONE V</td>
<td>5CE-A2</td>
<td>25</td>
<td>4</td>
<td>–</td>
<td>223/50*</td>
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<tr>
<td></td>
<td>5CE-A4</td>
<td>49</td>
<td>4</td>
<td>–</td>
<td>223/50*</td>
<td>0.5</td>
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<tr>
<td></td>
<td>5CE-A5</td>
<td>77</td>
<td>6</td>
<td>–</td>
<td>175/38*</td>
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<td>5CE-A7</td>
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<td>5CE-A9</td>
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<td>6</td>
<td>–</td>
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<tr>
<td>CYCLONE V</td>
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<td>50</td>
<td>6</td>
<td>–</td>
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<td>77</td>
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<td>7</td>
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<td>–</td>
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<tr>
<td>CYCLONE V</td>
<td>5CGT-D5</td>
<td>77</td>
<td>6</td>
<td>–</td>
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<td></td>
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<td>7</td>
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<td>301</td>
<td>8</td>
<td>–</td>
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</tr>
</tbody>
</table>

**AEC-Q100** Package options available with automotive-grade variants. True LVDS I/O count only. Does not include eTX. *Additional RX available.
## CYCLONE IV E PACKAGE / MAXIMUM USER I/O MATRIX

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

<table>
<thead>
<tr>
<th>FAMILY</th>
<th>PRODUCT LINE</th>
<th>LOGIC DENSITY (K LES)</th>
<th>PLL (COUNT)</th>
<th>PACKAGE TYPE/ PIN COUNT</th>
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</thead>
<tbody>
<tr>
<td>Cyclone IV E</td>
<td>EP4CE6</td>
<td>6.3</td>
<td>2</td>
<td>EQFP-144 (E144)</td>
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<td>EP4CE10</td>
<td>10.3</td>
<td>2</td>
<td>MBGA-164 (M164)</td>
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<td>EP4CE15</td>
<td>15.4</td>
<td>4</td>
<td>UBGa-256 (U256)</td>
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<td>EP4CE22</td>
<td>22.3</td>
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<td>EP4CE115</td>
<td>114.5</td>
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### PLL (COUNT)
- 0.5
- 1.0
- 1.0
- 1.0
- 1.0
- 1.0
- 1.0
- 1.0

### BALL SPACING (MM)
- 0.5
- 0.5
- 0.8
- 1.0
- 0.8
- 1.0
- 1.0
- 1.0

### DIMENSIONS (MM)
- 22 x 22
- 8 x 8
- 14 x 14
- 17 x 17
- 19 x 19
- 19 x 19
- 23 x 23
- 29 x 29

### I/O / LVDS I/O (COUNT)
- 91 / 21
- 91 / 21
- 81 / 18
- 79 / 17
- 79 / 17
- 81 / 18
- 79 / 17
- 81 / 18

### BALL SPACING (MM)
- 0.5
- 0.5
- 0.8
- 1.0
- 0.8
- 1.0
- 1.0
- 1.0

### DIMENSIONS (MM)
- 11 x 11
- 14 x 14
- 19 x 19
- 23 x 23
- 27 x 27
- 31 x 31

### I/O / LVDS / TRANSCEIVERS (COUNT)
- 3
- 2
- 2
- 2
- 2
- 2
- 2
- 2

---

**AEC-Q100** Package options available with automotive-grade variants.

LVDS count includes dedicated and emulated LVDS pairs, see Cyclone IV Device Handbook.

---

## CYCLONE IV GX PACKAGE / MAXIMUM USER I/O MATRIX

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

<table>
<thead>
<tr>
<th>FAMILY</th>
<th>PRODUCT LINE</th>
<th>LOGIC DENSITY (K LES)</th>
<th>PLL (COUNT)</th>
<th>PACKAGE TYPE/ PIN COUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclone IV GX</td>
<td>EP4CGX15</td>
<td>14.4</td>
<td>3</td>
<td>QFN-148 (N148)</td>
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<td>EP4CGX22</td>
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<td>FBGA-169 (F169)</td>
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<td>EP4CGX30</td>
<td>29.4</td>
<td>4 / 6</td>
<td>FBGA-324 (F324)</td>
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<td>EP4CGX50</td>
<td>49.9</td>
<td>8</td>
<td>FBGA-484 (F484)</td>
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<td>EP4CGX75</td>
<td>73.9</td>
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<td>FBGA-672 (F672)</td>
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<td>EP4CGX110</td>
<td>109.4</td>
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<td>FBGA-896 (F896)</td>
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<td>EP4CGX150</td>
<td>149.8</td>
<td>8</td>
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</table>

### PLL (COUNT)
- 0.5
- 1.0
- 1.0
- 1.0
- 1.0
- 1.0
- 1.0
- 1.0

### BALL SPACING (MM)
- 22 x 22
- 8 x 8
- 14 x 14
- 17 x 17
- 19 x 19
- 19 x 19
- 23 x 23
- 29 x 29

### DIMENSIONS (MM)
- 11 x 11
- 14 x 14
- 19 x 19
- 23 x 23
- 27 x 27
- 31 x 31

### I/O / LVDS / TRANSCEIVERS (COUNT)
- 72
- 72
- 72
- 72
- 72
- 72
- 72
- 72

### BALL SPACING (MM)
- 0.5
- 1.0
- 1.0
- 1.0
- 1.0
- 1.0
- 1.0
- 1.0

### DIMENSIONS (MM)
- 11 x 11
- 14 x 14
- 19 x 19
- 23 x 23
- 27 x 27
- 31 x 31

### I/O / LVDS / TRANSCEIVERS (COUNT)
- 72
- 72
- 72
- 72
- 72
- 72
- 72
- 72

---

**AEC-Q100** Package options available with automotive-grade variants.
# Introducing the MAX10 FPGA (2.5V, 1.2V Core)

Altera's new MAX® 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, instant-on, small form factor programmable logic device.

## MAX 10 FPGA Key Features:
- 2 to 50k LE logic density
- Dual-image configuration
- Instant-on configuration
- Dual or single core rail options
- Optional ADC converter(s)
- Variable-precision DSP blocks

## MAX 10 FPGA Dual (Core) Supply Device Package / Maximum User I/O Matrix

<table>
<thead>
<tr>
<th>FAMILY PRODUCT LINE</th>
<th>LOGIC DENSITY (K LES)</th>
<th>PLL COUNT</th>
<th>PACKAGE TYPE/ PIN COUNT</th>
<th>PAD / BALL SPACING (MM)</th>
<th>DIMENSIONS (MM)</th>
<th>MAXIMUM IOS - TRUE RX / TRUE TX / EMULATED TX (COUNT)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td>36-WLCSP (V36)*</td>
<td>0.4</td>
<td>3 x 3</td>
<td>Ios - RX / TX / eTX</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>81-WLCSP (V81)*</td>
<td>0.4</td>
<td>4 x 4</td>
<td>Ios - RX / TX / eTX</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>256-FBGA (F256)</td>
<td>1.0</td>
<td>17 x 17</td>
<td>Ios - RX / TX / eTX</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>324-UBGA (U324)</td>
<td>0.8</td>
<td>15 x 15</td>
<td>Ios - RX / TX / eTX</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>484-FBGA (F484)</td>
<td>1.0</td>
<td>23 x 23</td>
<td>Ios - RX / TX / eTX</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>672-FBGA (F672)</td>
<td>1.0</td>
<td>27 x 27</td>
<td>Ios - RX / TX / eTX</td>
</tr>
</tbody>
</table>

### Feature Set Options:
- C = Base
- F = Dual Configuration CFM
- A = Dual Configuration CFM + Analog Features

### Note:
- RX = True LVDS RX, TX = True LVDS TX, eTX = emulated LVDS TX, additional LOW SPEED eTX/RX I/O provided.
- "_6" denotes special FAST speed grade supported, A6G suffix. Contact Factory on availability.

### AEC-Q100
- Package options available in Quartus II with automotive-grade variants.
- Planned package option - available upon request / approval. A-Grade production 2H2015-1H2016 - device dependent. See Website for updated information.
## MAX 10 FPGA SINGLE (CORE) SUPPLY DEVICE PACKAGE / MAXIMUM USER I/O MATRIX (3.0V OR 3.3V CORE)

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

<table>
<thead>
<tr>
<th>FAMILY</th>
<th>PRODUCT LINE</th>
<th>LOGIC DENSITY (K LES)</th>
<th>PLL (COUNT)</th>
<th>PACKAGE TYPE/ PIN COUNT</th>
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<td>MAX 10</td>
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<tr>
<td>FPGA &quot;S&quot;</td>
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</tr>
</tbody>
</table>

### Package Details

- **MBGA-64** (E64)
- **EQFP-64** (E144)
- **MBGA-68** (M68)
- **MBGA-100** (M100)
- **TQFP-100** (T100)
- **TQFP-144** (T144)
- **FBGA-256** (F256)
- **FBGA-324** (F324)

### Ball Spacing (MM)

- 0.5
- 0.4
- 0.5
- 0.5
- 0.5
- 1.0

### Dimensions (MM)

- 4.5 x 4.5
- 9 x 9
- 5 x 5
- 16 x 16
- 6 x 6
- 22 x 22
- 17 x 17
- 19 x 19

### I/Os (COUNT)

- 101 - 27/10/27
- 122 - 29/9/29
- 110 - 28/10/28

### Notes:

1. For a specific list of part numbers for automotive-grade devices, consult the Automotive-Grade Device Handbook at altera.com.
2. For details on additional product line features (i.e., hard IP blocks, on-chip memory, and so on), consult the online device handbook at altera.com.
3. Other automotive-grade options might be available upon request. Consult your Altera sales representative to submit your request.
4. For full specifications, features, and I/O count for GPIO, HPS, LVDS, emulated LVDS, and transceivers, refer to Quartus II software documentation/handbooks.

### AEC-Q100

Package options available in Quartus II with automotive-grade variants.

### AEC-Q100

Planned package option - available upon request / approval. A-Grade production 2H2015-1H2016 - device dependent. See Website for updated information.

## MAX V (CPLD) DEVICE PACKAGE / MAXIMUM USER I/O MATRIX

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

<table>
<thead>
<tr>
<th>FAMILY</th>
<th>PRODUCT LINE</th>
<th>LOGIC DENSITY (LES)</th>
<th>PACKAGE TYPE/ PIN COUNT</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MAX V</td>
<td></td>
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</tr>
</tbody>
</table>

### Package Details

- **MBGA-64** (M64)
- **EQFP-64** (E64)
- **MBGA-68** (M68)
- **MBGA-100** (M100)
- **TQFP-100** (T100)
- **TQFP-144** (T144)
- **FBGA-256** (F256)
- **FBGA-324** (F324)

### Ball Spacing (MM)

- 0.5
- 0.4
- 0.5
- 0.5
- 0.5
- 1.0
- 1.0

### Dimensions (MM)

- 4.5 x 4.5
- 9 x 9
- 5 x 5
- 16 x 16
- 6 x 6
- 22 x 22
- 17 x 17
- 19 x 19

### I/Os (COUNT)

- 101 - 27/10/27
- 122 - 29/9/29
- 110 - 28/10/28

### Notes:

1. For a specific list of part numbers for automotive-grade devices, consult the Automotive-Grade Device Handbook at altera.com.
2. For details on additional product line features (i.e., hard IP blocks, on-chip memory, and so on), consult the online device handbook at altera.com.
3. Other automotive-grade options might be available upon request. Consult your Altera sales representative to submit your request.
4. For full specifications, features, and I/O count for GPIO, HPS, LVDS, emulated LVDS, and transceivers, refer to Quartus II software documentation/handbooks.

### AEC-Q100

Package options available with automotive-grade variants.
POWERING YOUR INNOVATION: AUTOMOTIVE- GRADE ENPIRION POWERSOCs

Altera’s automotive-grade Enpirion PowerSoC power management products are ideally suited for powering automotive-grade programmable logic devices and other automotive sub-system circuits. These highly integrated devices combine high efficiency and a tiny footprint to maximize power density while minimizing heat. With a 45,000 years mean time between failures (MTBF), Enpirion PowerSoCs are built to meet automotive reliability requirements.

**Enpirion PowerSoC key features:**
- AEC-Q100 qualified
- 45,000 years MTBF
- Integrated MOSFETs, inductor, and capacitors enable tiny footprint
- High efficiency reduces power loss and heat
- Easy to use with minimal external components, comprehensive FPGA power tools, and fully validated designs

### ENPIRION AUTOMOTIVE-GRADE POWERSOC MATRIX

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

<table>
<thead>
<tr>
<th>PRODUCTS</th>
<th>$I_{\text{out}}$ (A)</th>
<th>$V_{\text{IN}}$ RANGE (V)</th>
<th>$V_{\text{OUT}}$ RANGE (V)</th>
<th>PACKAGE</th>
<th>APPROX. TOTAL SOLUTION SIZE (MM²)</th>
<th>ENABLE</th>
<th>OVERCURRENT PROTECTION (OCP)</th>
<th>OVER-TEMPERATURE PROTECTION (OTP)</th>
<th>UNDER VOLTAGE LOCK-OUT (UVLO)</th>
<th>VID $V_{\text{OUT}}$ SET</th>
<th>EXTERNAL VOLTAGE DIVIDER $V_{\text{OUT}}$ SET</th>
<th>POWER GOOD (POK)</th>
<th>PROGRAMMABLE SOFT-START</th>
<th>FREQUENCY SYNCHRONIZATION</th>
<th>PARALLEL OPERATION</th>
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<td>EP53xx 5V PowerSoCs</td>
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<td>EP5358LUA</td>
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<td>2.4 – 5.5</td>
<td>1.8 – 3.3</td>
<td>QFN16</td>
<td>21</td>
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<td>QFN60</td>
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<td>EN6390QA</td>
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</tr>
</tbody>
</table>

Note: OCP = Overcurrent protection, OTP = Over-Temperature protection
See device datasheet for more information
WANT TO DIG DEEPER?

To learn more about Altera's automotive-grade products, contact your local FAE or sales representative. You can download automotive handbooks, white papers, and application notes at www.altera.com/automotive.


Visit our website for information on legacy automotive-grade devices:
- Cyclone III FPGAs
- Cyclone II FPGAs
- Cyclone FPGAs
- MAX II CPLDs
- MAX 7000A CPLDs