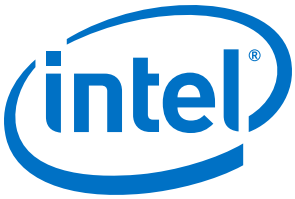

Quartus Prime Design Suite Update Release Notes

RN-01080-17.0.1.0
2017.06.16

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Contents

1 Quartus Prime Design Suite® Version 17.0 Update Release Notes

The *Quartus® Prime Design Suite Update Release Notes* describe the contents of Intel® Quartus Prime Design Suite Version 17.0 software update 1.

Quartus Prime Design Suite software updates require Version 17.0 of one of the following software packages:

- Quartus Prime Pro Edition
- Quartus Prime Standard Edition
- Quartus Prime Lite Edition

You must have one of these editions of Intel Quartus Prime software installed before you can install the software updates.

If you are using Quartus Prime Lite Edition software, apply the Quartus Prime Standard Edition software update. The Quartus Prime Standard Edition software issues addressed in this update also apply to the device families that are supported Quartus Prime Lite Edition software.

Related Links

- Quartus Prime Standard Edition Software and Device Support Release Notes Version 17.0
- Quartus Prime Pro Edition Software and Device Support Release Notes Version 17.0

1.1 Issues Addressed in Update 1

1.1.1 Quartus Prime Standard Edition Software

1.1.1.1 Quartus Prime Software GUI

- Corrected an issue where the Tasks panel sometimes incorrectly displayed all processes in a compilation with a question mark next to them, despite the processes running successfully.

1.1.1.2 Quartus Prime Device Support

- For Arria 10 devices, enabled missing timing arcs for the HPS NAND interface to the FPGA.
- For Arria 10 devices, updated timing models for Arria 10 devices that support 125 degree operation.

1.1.1.3 Quartus Prime Compilation and Design Flows

- Fixed an issue in Chip Planner where performing location assignment to a node with a name that contains "\" did not produce a correct location assignment because the "\" was omitted and the node could not be identified.
- Fixed an internal error that occurred when trying to assign a differential I/O standard to a node or bus signal that has a name shorter than 2 characters.
- Updated the RTL simulation for specific INI protected use case where LVDS Rx DPA is dynamically reconfigured for specific data bit rates that are lower than PLL minimum frequency.

1.1.1.4 Fitter

- Fixed an internal error during the fitter when fPLL `c_counter` settings are legal (between 1 and 3) but the fitter still errored out.
- For Arria 10 devices, the RX bonded check was enhanced so that RX-only PCS-bonded designs pass the fitter checks.
- For MAX 10 devices, fixed an issue where selecting a combination of I/O standard and strength for a MAX 10 device causes an error.

1.1.2 Quartus Prime Pro Edition Software

1.1.2.1 Quartus Prime Software GUI

- Fixed a bug in the Qsys GUI where if you change your focus to a subsystem and generate the system, the parent system is skipped.

1.1.2.2 Quartus Prime Device Support

- Updated packages for the following Cyclone 10 device models to go from 4 HSSI channels to 6 HSSI channels so that the PCIe Hard IP Core is accessible:
  - 10CX105 (U484 package)
  - 10CX085 (U484, F672 package)

1.1.2.3 Quartus Prime Compilation and Design Flows

- Improved run time on Windows platforms.
- Fixed the following error that can be caused when Synopsys Design Constraint (.sdc) files in a project include `.` or `..` in an otherwise absolute file path (for example, `/home/me/designs/./project_files/../timing/test.sdc`)

```
Internal Error: Sub-system: QHD, File:
/quartus/comp/qhd/qhd_sdc_database_model.cpp, Line: 143
is_normalized_path(abs_path, m_is_windows)
```

  This fix allows the affected style of path name to be used for SDC files.
- For Arria 10 devices, added a fix to automatically legalize a transceiver setting in a design. The update is applied during the design database import flow. This updated flow enables you to keep your fitter result from a previously compiled design. You must regenerate your bit-streams using the Quartus Prime assembler.
- Fixed an issue in Chip Planner where performing location assignment to a node with a name that contains "\" did not produce a correct location assignment because the "\" was omitted and the node could not be identified.
- Fixed an issue with the handling of entity-bound Synopsy design constraint (`.sdc`) files and Windows junction point type file system links.
- Fixed an `undefined entity` error that occured when preserving periphery logic in a `root_partition.qdb` if the original project includes HSSI IP in a default `auto_fab_0` partition. This fix improves the stability of importing periphery logic with a `root_partition.qdb`.

1.1.2.4 Fitter

- For Arria 10 devices, fixed an issue where the fitter would read the constraints database for Cyclone 10 GX devices instead, causing unforeseen issues such as incorrect bit settings due to different rules-based configuration (RBC) rules between the two device families.
- Fixed an issue that could cause the following Internal Error, when arithmetic output crosses partition boundary:

```
Internal Error: Sub-system: U2B2_CDB, File:
/quartus/db/u2b2/u2b2_cdb_nf_lab_ibr_module.cpp, Line: 342
```

- For Arria 10 devices, removed an unnecessary timing constraint on some clock nets. This change restored the behavior to that seen in Quartus Prime Version 16.1 and earlier. This change is strictly a timing improvement over Quartus Prime Version 17.0.
- For Arria 10 devices, the RX bonded check was enhanced so that RX-only PCS-bonded designs pass the fitter checks.
- Fixed an internal error during the fitter when fPLL `c_counter` settings are legal (between 1 and 3) but the fitter still errored out.

1.1.3 IP and IP Cores

Attention: Unless stated otherwise, the following IP issues apply to both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

DisplayPort IP Core

- Refined DisplayPort TX PMA settings based on compliance testing to enable optimized transceiver performance.
- Fixed inaccurate transmission of MVID value at certain boundary values. This issue caused the pixel clock generation on the corresponding DisplayPort sink to be potentially wrong.
- Enhanced the DisplayPort RX API to handle the scenario where the GPU produces a one-time burst of bit errors after link training completes.

Low Latency (LL) Ethernet 10GbE MAC IP Core

- For Quartus Prime Pro Edition software running on Windows platforms, fixed the Arria 10 example design generation errors.

External Memory Interface IP Core

- Removed a default timing constraint that was applied to the `altera_reserved_tck` clock, which is used for ISSPs and SLD tools. You must add the proper timing constraint for this design based on your JTAG topology in `jtag_example.sdc`.

Fractional Phase-Locked Loop (fPLL) IP Core

- For Arria 10 devices, restricted the use of the 25 Mhz reference clock for fPLL to the HDMI protocol. This restriction also returns the minimum reference clock for fPLL in core mode to 27MHz.

HDMI IP Core

- Resolved possible HDMI design example IP generation issue in Windows systems caused by the Java script character limit being exceeded.
- Updated the HDMI RX IP core to fix timing violation that occurred when you connected each input `ls_clk` to independent clocks. This violation caused the channel data paths to be asynchronous after lane deskewing and alignment.
- Updated design example to work around interoperability issues with certain HDMI sources. Switching between different color space using certain HDMI source might cause no display or image distortion on the HDMI sink. This problems is caused by the following issues that have been corrected:
  - Read requests from the auxiliary bypass FIFO have a problem that caused missing end-of-packets in the last auxiliary packet.
  - Because the HDMI reconfiguration state machine performs a reconfiguration when the CD[3:2] from General Control Packet is `2'b01`. According to HDMI 1.4b specification, video with 24 bit per pixel can be indicated as CD[3:0] is `4'b0100`. However, certain source considers 24 bits per pixel as non-deep color ("Color Depth not indicated") and then transmits CD[3:0] as `4'b0000`. This transmission affects existing reconfiguration logic which monitors where CD[3:2] to trigger reconfiguration required for deep color.

I/O Phase-Locked Loop (IOPLL) IP Core

- For Cyclone 10 GX devices, addressed an issue where IOPLL IP cores did not generate correctly.

JESD204B IP Core

- For Arria 10 devices, fixed the following issues related to the transceiver dynamic reconfiguration interface:
  - The reconfig_* ports are unconnected in ED for L=1.
  - VHDL reconfig_* port type mismatch (std_logic, std_logic_vector).
  - Unconstraint reconfig_clk in standalone IP.
  - Unconnected reconfig_* ports in IP simulation.

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core

PCIe Hard IP Core

- For Arria 10 devices, made the following updates
  - Enabled a hardware cap value of 10.
  - Fixed a bug in Quartus Prime for mapping a hard IP atom parameter.
  - Updated the PCIe hard IP to use a consistent value for the HIP parameter across all revisions.
- For V-Series Avalon-MM DMA Interface, the ByteEnable signal is now visible in 128-bit mode.
- For Arria 10 devices, resolved the ModelsSim VHDL compile error.

RapidIO IP Core

- Fixed an issue where the next expected acknowledge packet ackID does not increment when triggering the bit-23 PORT_DIS of Port 0 Control CSR.
- Fixed an issue where spurious packets are sent after link partner re-initializes from reset.
- Fixed an issue where the outbound/transmitted packet ackID is out of sync after link partner re-initializes from reset.
- Fixed an issue where Port OK does not assert occasionally when resetting the link partner.

Serial Data Interface (SDI) IP Core

- Fixed a VHDL compilation issue in the NCSim simulator.

SerialLite III Streaming IP Core

- Fixed the SerialLite III VHDL example design which fails in the `ncsim` command due to an NC Sim version update.

Transceiver PHY IP Core

- Added a fix to handle the incorrect behavior of CDR controller and signal detect block for Electrical Idle entry in Gen2 and Gen3 in PCIe bonded designs.
- For Arria 10 devices, removed the following warning:

```
The value of parameter hssi_common_pcs_pma_interface_bypass_pma_sw_done"
cannot be automatically resolved.
Valid values are: true false.
```

Video and Image Processing Suite IP Cores

- Enabled OpenCore Plus evaluation for the configurable guard bands IP core.
- Fixed Video IP simulation models compilation issues in VCS/NCSIM.
- Fixed a bug where the Deinterlacer II IP core does not function correctly when configured in motion adaptive mode high quality mode but without video-over-film cadence correction.

1.1.4 Intel FPGA SDK for OpenCL

Attention: Unless stated otherwise, the following Intel FPGA SDK for OpenCL™ issues are associated with both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

- Updated fast-compile settings to remove LU decomposition limit and static timing analysis (STA) calls.
- For Arria 10 SX devices, connected HPS IP reset ports to fix base and flat compile.
- Updated the `cl_ext.h` with modified define values to avoid conflicts with the emulator.
- Fixed the problem with using `vstore_halfn` and `vstore_half` compiled for the emulator.
- Fixed bug in handling of constant arrays.
- Fixed a bug which causes problems in the `aoc` compiler when you specify absolute paths for the project directory.
- Fixed an issue that caused the following assertion:

```
acl_thread.h:47:acl_sig_started: Assertion '!acl_inside_sig' failed
```

- Fixed a situation where the compiler deletes a project directory even when it was not originally created by the compiler. The first time that you compile a project with the updated version of the compile, you might need to delete the old project directory manually.
- On Windows systems, the compiler now exposes Quartus Prime errors to `stdout` and warns you that missing file errors might be caused by file name length limits.
- For Arria 10 GX devices, added support for the Ubuntu Version 16.04 operating system.
- This fix correctly sets up the path to the required Qsys tools for the Intel FPGA SDK for OpenCL Offline Compiler targeting Arria 10 based board support packages. Without this fix, the compiler fails in the ip-generate stage and outputs a `sh: qsys-archive: command not found` message to the log file.

1.2 Software Issues Resolved

Table 1. Customer Service Requests Resolved in the Quartus Prime Design Suite Version 17.0 Update 1

Customer Service Request Numbers Resolved					
11266103	11276040	11280782	11281478	11293397	11302641
11302641	11306504	11307454	11311366	11314093	11317825

1.3 Software Patches Included in Update Releases

Table 2. Software Patches included in the Quartus Prime Design Suite Version 17.0 Update 1

Software Version	Patch	Customer Service Request Number
Quartus Prime 17.0	0.07	11314093
Quartus Prime 17.0	0.03	-
Quartus Prime 16.1.2	2.17	11298413
Quartus II 15.0.2	2.25	11266103

1.4 Known Issues and Workarounds

For information about known software issues, please visit the Intel FPGA Knowledge Base.

Related Links

- Intel FPGA Knowledge Database
- Intel FPGA Documentation: Release Notes
- Quartus Prime and Quartus II Software Support

1.5 Document Revision History

Date	Document Version	Changes
June 2017	2017.06.16	• Initial release with Quartus Prime Design Suite version 17.0 update 1 information.