

Implementing Digital IF & Digital Predistortion Linearizer Functions with Programmable Logic

Introduction

Mobile communication is quickly becoming the primary mode of communication for most of the developed world. Based on 2.5G technologies, most countries now have data services available that will bring about significant changes in the way people exchange business and personal information.

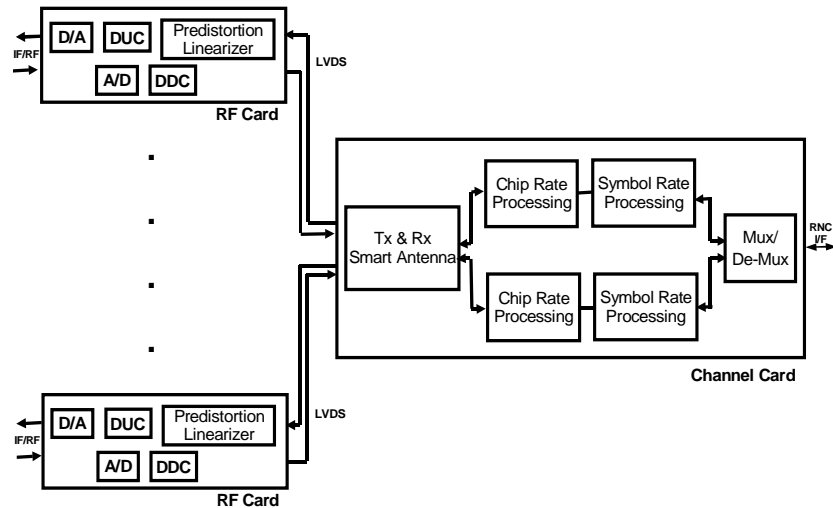
With the increasing popularity of data services, greater amounts of bandwidth are required. One of the key ways to increase the bandwidth is to use diversity techniques, which have been incorporated in most of the 3G (base station modem) standards specifications. However, with each additional antenna an additional transceiver is required, which can significantly increase the system cost and deter the operators from leveraging this technology. On the other hand, Digital IF, which leverages advancement in data converter and hardware programmable technology, reduces component and manufacturing costs. Another method that is gaining popularity is the digital predistortion linearizer (DPL) technique. The DPL technique relaxes the linearity requirements of power amplifiers (PAs), enabling the use of non-linear PAs that are significantly cheaper, thereby reducing the cost of the overall system.

Designers may wonder what is the best platform to implement the cost-effective Digital IF and DPL techniques. This white paper discusses the many advantages of implementing Digital IF and DPL functions with programmable logic, as opposed to ASSPs. First, the field programmability feature significantly lowers the risk of introducing new technologies such as DPL, while also offering scalability for use with different types of systems (e.g., macro, micro, and pico BTS, etc.). Second, programmable logic enables a highly integrated solution, which can include a digital upconverter, DPL, digital downconverter, resampler, data reformatter, and LVDS I/O transceivers in a single chip. Finally, with programmable logic, a designer can implement a custom design optimized for his or her application (i.e., filter skirts, decimation factor, word length, etc.) resulting in superior performance compared with a generic ASSP solution.

Mobile Base Station Signal Processing Data Path

Figure 1 shows the digital signal processing data path of a mobile base station. On the transmit side, time-division multiplexed (TDM) data from the RNC I/F card is de-muxed and fed to different symbol-rate processing units on the channel card. After encoding, interleaving, and rate matching, data is spread using channelization and scrambling codes. The output from the chip-rate processing unit is fed to the smart antenna unit which implements transmit-diversity based on either closed-loop or space-time diversity techniques as specified in 3GPP. Output from the smart antenna unit is sent over the backplane or cable/fiber to the RF card. The RF card combines the signals it receives from multiple channel cards, performs digital upconversion from baseband to IF (as well as DPL) before converting the signals into an analog waveform using a digital-to-analog converter (DAC).

Figure 1. Signal Processing Data Path of a Mobile Base Station



On the receive side, IF data is sampled using the undersampling techniques. The band of interest is downconverted to baseband and filtered within the digital downconverter (DDC). The downconverted data from the different antennas is fed into the smart antenna unit, which can be based on either beamforming or antenna diversity. Next, chip- and symbol-rate processing is performed to extract the user's data, which is then muxed and forwarded to RNC by the RNC interface card.

- For more information, refer to: A. Hottinen, O. Tirkkonen and R. Wichman, *Closed-loop Transmit Diversity Technique for Multi-Element Transceivers*, IEEE VTC 2000.

Using DPL & Digital IF Techniques with W-CDMA Transmitters

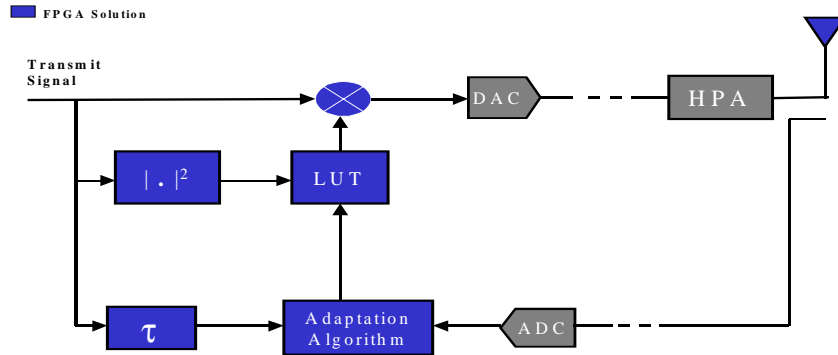
DPL Technique

To achieve the overall system specification, the system PAs need to meet rigorous performance requirements. With wideband-code division multiple access (W-CDMA), the challenge becomes even greater as the PAs need to maintain linearity over a wider bandwidth, while also supporting a higher peak-to-average ratio of 3 to 12 dB.

Traditionally, the approach has been to use linear amplifiers, such as class A amplifiers, and operate them in the linear mode by backing off from the saturation range, thereby reducing the efficiency of the system. This approach results in excessive power consumption as well as increased equipment cost, which in some cases can run up to one-third the overall base-station cost.

An attractive alternative to low-efficiency class A linear amplifiers is the class AB and class B amplifiers as they are significantly more cost-effective to build. However, the issue with the class AB and class B amplifiers is that they do not meet the linearity requirements demanded by 3G standards. To address this issue, there are a number of techniques that can be used for linearization; DPL is one such technique that can potentially meet the requirements of a W-CDMA transmitter. Figure 2 shows the functional block diagram of a DPL system.

Figure 2: Functional Block Diagram of DPL System



DPL Predistortion Algorithm

The DPL is equivalent to a nonlinear circuit with a gain expansion response that is the inverse of the PA gain compression response, and a phase response that is the negative of the PA phase response. The amplitude (ρ) and phase (θ) response for the predistorter is as follows, Equation 1:

$$A(\rho_x^2) = \begin{cases} \frac{1 - \sqrt{1 - \rho_x^2}}{\rho_x^2}, 0 \leq \rho_x^2 \leq 1 \\ \frac{1}{\sqrt{\rho_x^2}}, \rho_x^2 > 1 \end{cases} \quad \text{Equation 1}$$

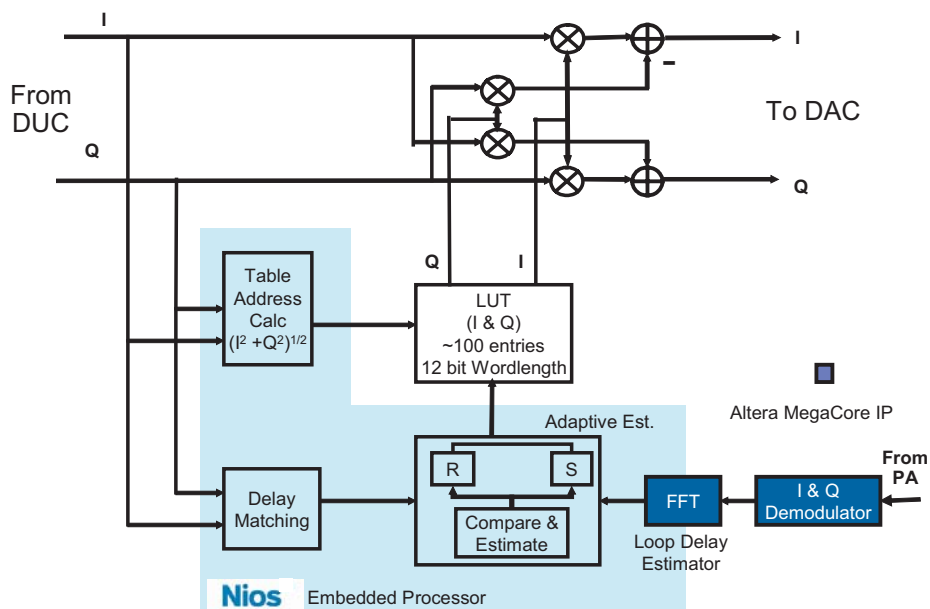
$$\theta(\rho_x^2) = A(\rho_x^2) * \theta_0, \because \theta_0 = \frac{\pi}{6}$$

where $A(\rho_x^2)$ is the output magnitude as a function of input magnitude squared and $\theta(\rho_x^2)$ is the output phase as a function of input magnitude squared.

To adapt to the change in the response of the PA (due to temperature changes or aging), the output of the PA is continuously monitored and look-up table (LUT) values are dynamically updated to compensate for variation in the PA's behavior; it calculates the mean square error between the input and output and calculates the new weights using Equation 1. A computationally efficient and robust algorithm that has been proposed is the rotate and scale (RASCAL) method. RASCAL is an iterative method, which is evaluated every time the complex modulation envelope traverses a given entry in the LUT. Given that the maximum rate of change of the complex modulation envelop is the input data rate (i.e., symbol rate or chip rate in a CDMA system), the processing speed needed to compute the new values is well within the capability of a Nios[®] embedded processor, which is capable of running at 100+ MHz in a Stratix[™] device. Figure 3 shows the Altera[®] Stratix device implementation of a DPL function.

- For more information on the RASCAL method, refer to: Wright and Duller, *Experimental Performance of an Adaptive Digital Linearized Power Amplifier*, IEEE Trans. on Vehicular Tech., Vol. 41, No. 4, Nov. 1992.

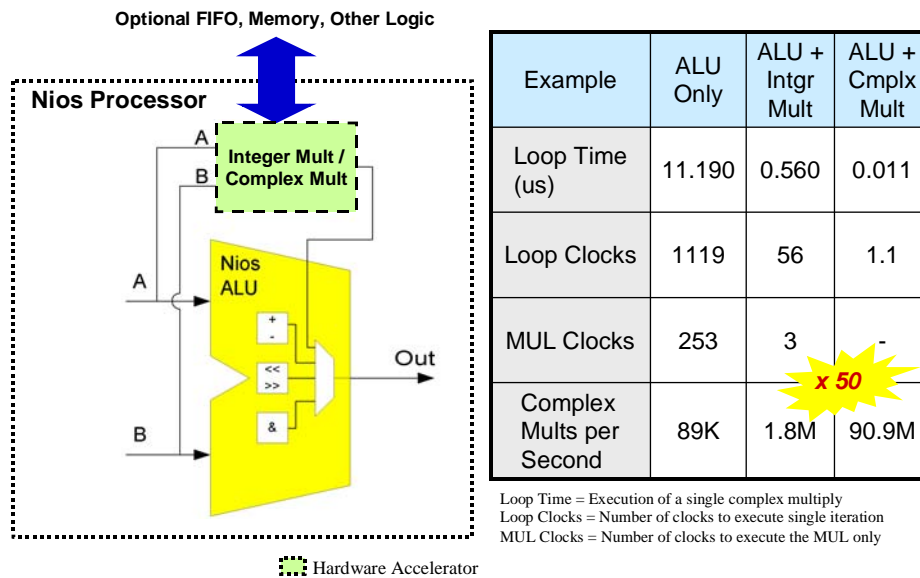
Figure 3: Implementing a DPL Function Using the Nios Embedded Processor & Stratix Device



Stratix devices, with their embedded multipliers and RAM blocks, are well suited for the implementation of DPL functions. One of the novel capabilities of the Nios processor is the ability to utilize custom instructions. This capability enables hardware acceleration of program code that otherwise might require a significant number of processor cycles. Figure 4 shows an example of how a complex multiplier can be accelerated via a custom Nios processor instruction. By implementing a custom instruction for a complex multiplier, a 90+ million samples per second (MSPS) data rate can be achieved. Besides complex multiplication, another useful function for this application—which benefits from the Nios processor’s custom instruction capability—is the Table Address Calculation.

- For more information, refer to: Sundstrom et al, *Quantization Analysis and Design of a Digital Predistortion Linearizer*, IEEE Trans. on Vehicular Tech., Vol. 45, No. 4, Nov. 1996.

Figure 4. Nios Custom Instruction Example of a Complex Multiplier



Digital IF Technique

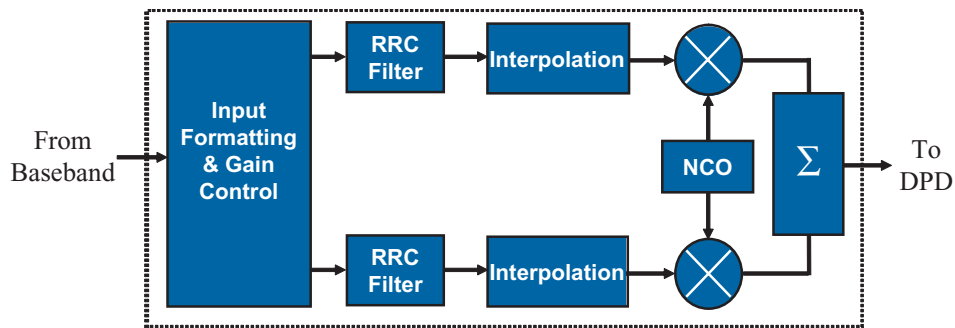
With the recent improvements in data converter and programmable hardware technology, baseband filtering and upconversion to the first IF stage can be done in the digital domain. There are several advantages of implementing IF in the digital domain using digital signal processing technology.

- For more information, refer to: David B. Chester, *Digital IF Filter Technology for 3G Systems: An Introduction*, IEEE Comms Magazine, Feb. 1999.

Digital Upconverter

The input data is baseband filtered and interpolated before it is quadrature modulated with a tunable carrier frequency. To implement the interpolating baseband finite impulse response (FIR) filter, Altera offers the FIR Compiler with which an optimal fixed or adaptive filter can be built. Altera also offers the numerically controlled oscillator (NCO) Compiler intellectual property (IP) core that can generate a wide range of architectures for oscillators with spurious-free dynamic range (SFDR) in excess of 115 dB and very high performance. Depending on the number of frequency assignments (FA) to be supported, the right number of digital upconverters can be easily instantiated in a programmable logic device. See Figure 5.

Figure 5. Digital Upconverter Block Diagram

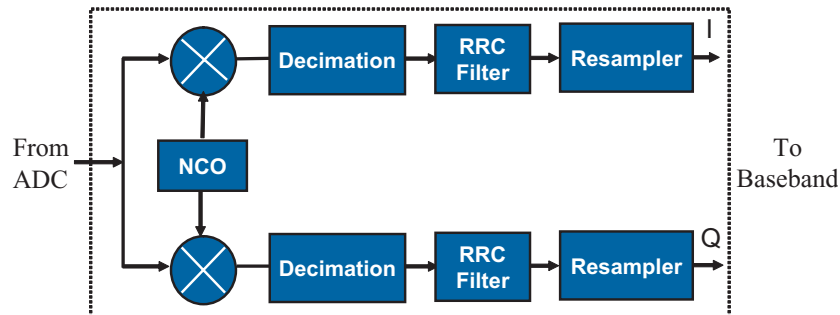


Digital Downconverter

On the receiver side, digital IF techniques can be used to sample an IF signal and perform demodulation and channelization in the digital domain. Using undersampling techniques, high frequency, IF signals (typically 100+ MHz) can be quantified.

The wide-band IF signal is translated to a complex baseband signal by quadrature multiplication. An NCO generates the quadrature signals for the multipliers. The complex baseband signal is low-pass filtered to prevent aliasing due to decimation. See Figure 6.

Figure 6. Digital Downconverter Block Diagram



Advantages of a Programmable Logic-Based Digital IF Solution

The most obvious advantages of a programmable logic-based digital IF solution compared with an ASSP solution are flexibility and integrational freedom. This section discusses the specific advantages, including:

- Customizable front end
- Optimal filter architecture for a given application
- High-performance NCO compiler

Customizable Front End

In a programmable-logic implementation of a digital upconverter, the data formatting—often required between the baseband processing elements and the upconverter—can be seamlessly added at the front end of the upconverter. This technique provides a fully customizable front end to the upconverter and allows for channelization of high-bandwidth input data, as found in universal mobile telecommunications service (UMTS) carrier systems. Custom logic, or a Nios embedded processor, can be used to control the interface between the upconverter and the baseband processing entity. To ease the integration task, the channelization logic can easily include serial-to-parallel and gain circuits, or other custom formatting blocks.

Many ASSPs provide the option of adjusting the incoming data's sampling rate so that the required interpolation rate through the upconverter is possible with the permissible parameterizations. While this operation may not be required in a programmable-logic implementation where the interpolation factors are unrestricted, resampling of the input data by a factor of L/M can optionally be performed by including an interpolating-by- L FIR filter with a custom downsample-by- M operation on its output. For some rate-changing parameters, it may be more efficient to implement a fractional rate change by pushing the upsampling operation through to the output side of the filter, and using a custom phase-selecting downsampler on the filter output data. This technique has the effect of reducing the required operating frequency of the fixed-rate FIR filter, or equivalently, increasing the number of channels that can be time-division multiplexed within the filter. Custom downsamplers can sometimes prove to be more jitter-resistant when presented with a fractional decimation rate M than generic downsamplers, which generally present a worst-case timing error of $T_s/2^L$, where T_s is the input sample period.

Optimal Filter Architecture for a Given Application

To efficiently band-limit the input data pulse-train, a root-raised cosine pulse-shaping interpolating FIR filter, in conjunction with a second-stage interpolating FIR filter, is typically used. Because the maximum operating frequency of such filters exceeds 200 MHz in recent programmable logic device families, the designer can make speed-area trade-offs depending on the input data rate, precision, and interpolation factor to meet the specifications of a particular application.

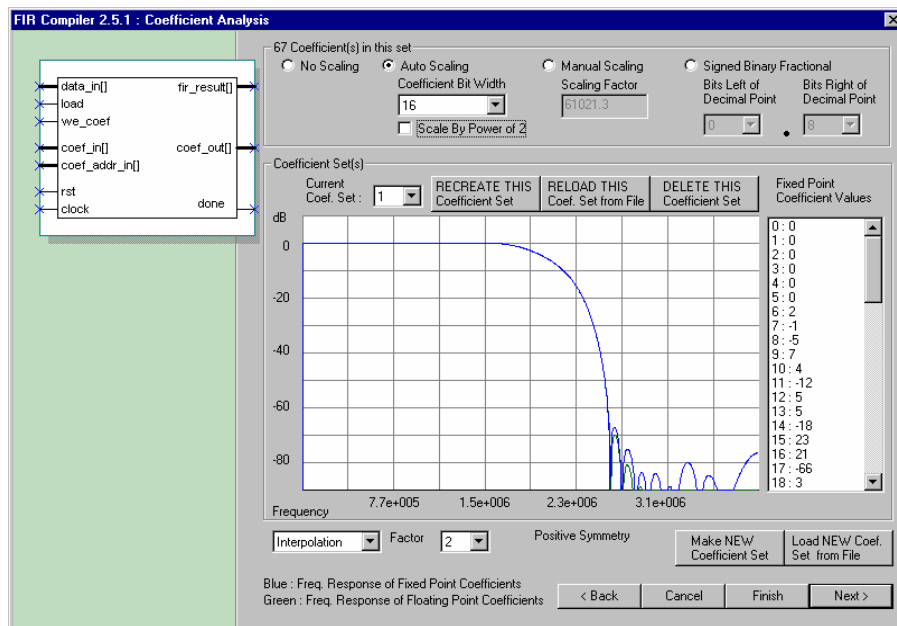
For example, for high-bandwidth input signals such as UMTS (where chip-rate data is at 3.84 MSPS), multi-channel multi-bit-serial, or fully serial FIR structures utilizing distributed arithmetic techniques can be used to increase the overall channel count or reduce the resource usage for the same channel count. In other standards where the specifications might be less stringent, internal resolution within the filter can be reduced, and a fully-parallel multi-channel architecture may prove to be the optimum point in the speed-area trade-off. Alternatively, for smaller pico-cell base stations, where a single carrier is required, parallel complex filters can be efficiently implemented using dedicated multiplier circuitry.

In addition, when different FIR filter coefficients are required across channels—as might occur in a system where support for multiple or migrating standards are required in a single upconverter—the flexibility of a programmable logic implementation of the baseband interpolating filters can be very beneficial. In this situation, the ability to trade-off area against speed is paramount, given that each channel requires its own individual co-efficient set. To dramatically reduce the overall resource usage per complex channel, use multiple, fully-serial, or multi-bit serial architectures and efficiently utilize the M512 memory blocks of the Stratix device.

In a transmitter where the signal-to-noise ratio (SNR) of the upconverted signal is required to be very high, the number of taps in the pulse-shaping filter can flexibly be increased to improve the quality of the band-limited filter output. This allows system level SNR trade-off between the digital upconverter and other components in the RF system. While this will increase the resource usage, similar trade-offs to those discussed in this section can be used.

Altera’s FIR Compiler MegaCore® function incorporates a fully integrated design environment which allows the user to manage the resource-throughput tradeoff for a given filter specification and decide on the optimal architecture to provide the required number of FIR channels. See Figure 7.

Figure 7. Altera’s FIR Compiler MegaCore Function



In digital upconverters where the required overall interpolation rate is relatively high, a cascaded integrator comb (CIC) filter stage is typically employed to efficiently achieve the rate conversion—while providing the required rejection of signal aliases inherent in the sampling rate change. To compensate for the passband droop that naturally occurs when using a CIC stage, one of the FIR interpolating filters (prior to the CIC stage) requires a passband response. With the addition of some channelization logic, the CIC stages can be efficiently time shared across multiple channels.

In some W-CDMA implementations where the desired overall interpolation rate is very low, it may be more efficient to use a series of low-interpolation rate FIR filters to perform the rate conversion and alias rejection, i.e., rather than incorporating a CIC stage in conjunction with additional interpolating FIR filters. Because of the basic mathematics that model CIC filter behavior, CIC filters have some undesirable aspects. However, the undesirable aspects must be weighed against the advantages CIC filters offer when used to interpolate by very low factors. Great care must be taken to avoid overflow in the intermediate stages, and the presence of additional noise in the circuit can lead to the generation of wideband noise in the integrator stages of the CIC filter. Instability can be detected by additional circuitry, and asynchronous clearing of internal registers can be accomplished under the control of a Nios embedded processor or by custom logic.

A designer creating a programmable logic implementation can choose to include a CIC stage for systems where the overall interpolation/decimation factor is high, or perform lower-factor interpolation/decimation across stable FIR filters with parameterizable interpolation rates. There is no minimum overall interpolation rate in a programmable logic implementation.

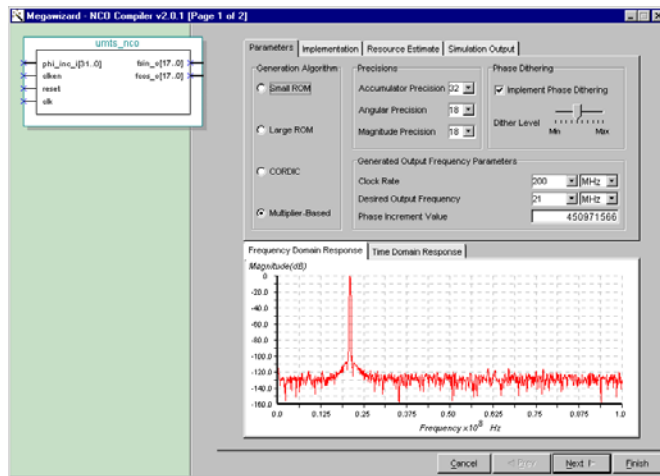
High-Performance NCO Compiler

Modulation of the interpolated data is performed by employing a dual-output quadrature oscillator to generate the IF carriers, with one NCO per channel. The NCO required needs to be tunable and must also exhibit high SNR and SFDR to guarantee that the modulated signal meets the relatively high spectral purity requirements of third-generation standards such as UMTS. Because each channel in the upconverter is required to mix data onto independent frequencies, it is important that NCO architectures be flexible in terms of the type of programmable logic device resources they consume when implementing a multi-channel digital upconverter/downconverter.

Parallel CORDIC architectures are capable of implementing high-precision oscillators that can run at over 300 MSPS, using only logic elements (LEs). Alternatively, memory-based oscillators require little or no logic to generate medium-precision sinusoidal outputs. Another novel architecture that employs dedicated multipliers in conjunction with internal memory provides output sample rates of over 230 MSPS, and generates very-high precision signals with a balanced device resource cost that exponentially reduce the memory requirements over the standard memory-based oscillator.

To further increase the SFDR, tunable dithering may be employed to randomize the highly correlated noise resulting from finite precision in the generation algorithms arithmetic. The localization manifests itself as spurs in the spectral response of the oscillator, and is deemed to be one of the most serious degradations of signal quality in a transmitter. Depending on the clock to output frequency relationship, architecture and internal precisions specified, the dithering level required might be different across each oscillator. The Altera NCO Compiler allows designers to tune the dithering level to meet the required specification and view the effect graphically in the output spectrum. See Figure 8.

Figure 8. The Altera NCO Compiler MegaCore Function



Mixing of the interpolated data and the quadrature oscillator outputs can be performed by the dedicated multipliers of the Stratix device, which will, in most cases, be time-shared across I-Q outputs from the mixer. Alternatively, in programmable logic implementations where dedicated multipliers are in short supply, flexible LE-based multipliers can also be used.

Sample Implementation of the Digital Upconverter Data Path Blocks

When it is desired to upconvert a UMTS chip-rate signal with a rate of 3.84 MSPS to a 92.16 MSPS output before modulating an IF carrier, the interpolation factor required is 24. This can be implemented by a pair of interpolating-by-2 filters followed by a CIC stage interpolating by 6. To implement this interpolation factor in most ASSPs, resampling of the input chip-rate signal is required. However, there is no minimum with a programmable logic-based implementation.

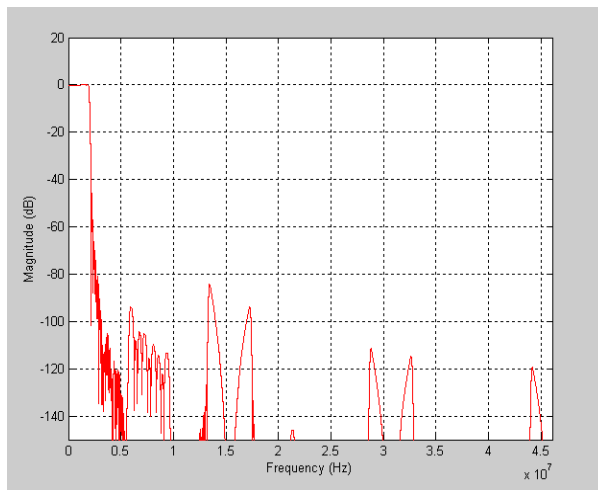
The first filter stage is a root-raised, cosine pulse-shaping FIR of 67 taps interpolating by a factor of 2, FIR-1, with an input rate of 3.84 MSPS and excess bandwidth of 22%—with an input resolution of 16 bits and a coefficient resolution of 16 bits. Due to the low input rate relative to the maximum operating frequency of the FIR filter in a Stratix device, a multi-bit-serial distributed arithmetic architecture with four serial units is selected, which leads to a very efficient implementation for the filter, particularly when a multi-channel structure is used.

The second stage in the interpolating filter-chain is a 31-tap interpolating-by-2 FIR filter, FIR-2, with a sufficiently wide passband to allow pulse-shaped symbol data of excess bandwidth of 0.32 at its input. The filter also implements passband droop compensation for the following CIC interpolating stage. It takes 16-bit complex inputs at a rate of 7.68 MSPS. To balance the resource usage of the overall design, a multi-channel, multi-bit-serial distributed arithmetic architecture is again selected with its resources heavily based in the Stratix device's M512 memory blocks.

To generate the desired 92.16 MSPS upsampled signal for modulation, the output 15.36 MSPS signal is interpolated by a factor of 6 via a CIC filter. The CIC filter is of order 5 and was designed using the Altera DSP Builder, and, in this example, the CIC filter is entirely implemented in LEs. The CIC filter uses a multi-channel implementation in the feed-forward, low-rate comb portion of the CIC. The high-rate integrator portion is duplicated across all channels to minimize the control logic that would be required to channelize the feedback paths of the individual integrator stages. In this example, stability detection and CIC filter overhead were not considered; however, the ability to uniformly and asynchronously clear all intermediate registers in the design have been considered.

Figure 9 shows the overall impulse response of the three-stage interpolator for an output sample rate of 92.16 MHz. This response was generated using bit-accurate fixed-point models of the filter-chain blocks and convolving their impulse responses within the MATLAB simulation environment. The overall passband ripple is limited to 0.1 dB.

Figure 9. Overall Interpolator Response

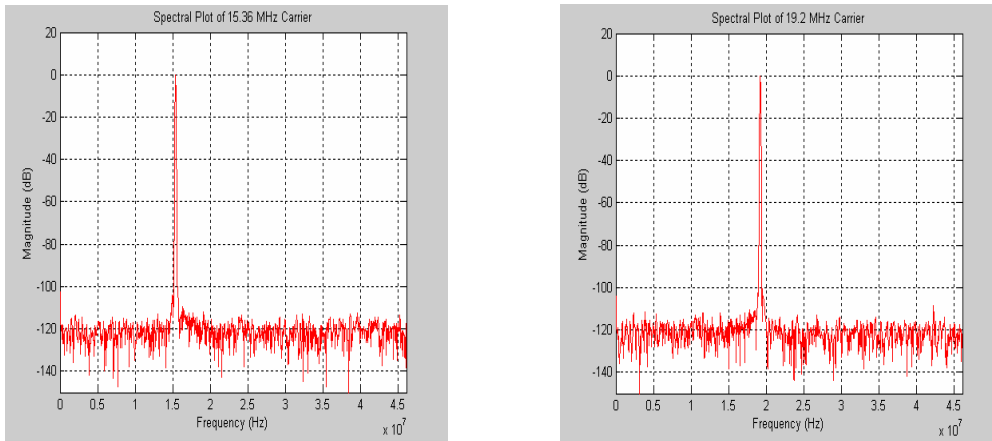


The NCO is required to output a sample rate of 92.16 MSPS. The example implementation uses a multiplier-based architecture utilizing the Stratix dedicated multiplier and adder circuitry to produce

quadrature oscillator outputs with an SFDR in excess of 105 dB. Because the multiplier-based NCO is capable of operating well in excess of 200 MSPS, a multi-cycle NCO is selected from within the NCO MegaWizard® Plug-In Manager, effectively resulting in each digital signal processor (DSP) block being time shared between a pair of NCOs.

Figure 10 shows the NCO spectral response for two carrier frequencies of 15.36 and 19.2 MHz, respectively.

Figure 10. NCO Outputs of 15.36 MHz & 19.2 MHz Carrier Frequencies



Mixing of the interpolated data streams with the oscillator outputs is performed in the dedicated multipliers of the Stratix device. Due to the high throughput of the Stratix DSP blocks, the mixer multipliers are also time-shared across quadrature channels to efficiently require a single multiplier per complex channel. The output carriers are combined using a high-performance scaling parallel adder tree. Table 1 summarizes the resource usage of the principal data path functional blocks for a 10 UMTS-channel implementation in an Altera Stratix device family. (Channelization, control and data formatting device resources have not been included in this analysis.)

Table 1: Device Resource Utilization for 10 UMTS Channel Digital Upconverter

Functional Block	FIR-1	FIR-2	CIC	NCO	Mixer & Adder	Total	Stratix EP1S25 (%)
LEs	5,376	5,440	4,940	2,654	216	18,626	72
M512 RAM Blocks	0	184	0	0	0	184	82
M4K RAM Blocks	24	20	0	60	0	104	75
DSP Blocks	0	0	0	5	3	8	80

Total Digital IF & DPL Solution From Altera

Altera offers many tools for programmable logic-based Digital IF and DPL implementation. This section describes the Altera DPS Builder, the Stratix device family's True-LVDS™ circuitry, the Nios embedded soft processor, and HardCopy™ devices—all which offer the tools for a total Digital IF and DPL solution.

DSP Development Tool: Altera DSP Builder

For rapid development, Altera offers a DSP development tool called the DSP Builder. With the DSP Builder, complex DSP blocks can be seamlessly designed and integrated with pre-existing MATLAB (version 6.1 or 6.5) and Simulink (version 4.1 or 5.0) blocks and Altera IP MegaCore functions, all within the popular MATLAB environment. Also, synthesis and simulation can be performed from within the environment.

LVDS I/O to Link with Channel Card

High speed LVDS is typically used to communicate between the RF card and the channel card. Stratix features the True-LVDS™ circuitry, which is capable of 840-Mbps performance.

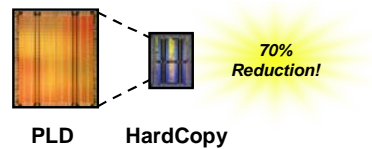
Board Configuring & Monitoring

An RF card typically does not have a discrete host processor because of the limited control-type tasks executed on the card. Altera Nios embedded soft processors are well suited for initialization, control, and monitoring functions.

High-Volume Solution

Finally, Altera offers a cost reduction solution with HardCopy devices (see Figure 11). With HardCopy devices, a die-size reduction of up to 70% can be achieved with a proportionate reduction in price. If, in a rare situation, a very high volume requirement is to be addressed, a viable migration to a custom ASIC is always available.

Figure 11. HardCopy Devices: A Low-Cost Migration Path



The following is a list of HardCopy device highlights:

- Low-Cost migration path for high-density FPGAs
 - 70% die size reduction
 - Proportionate reduction in cost
- Simple
 - No customer involvement, full turnkey solution
- Fast
 - Approximately 7 weeks for functional prototypes
- Risk-Free
 - Guaranteed functionality and performance
 - Pin compatibility and same package options

Conclusion

To lower the system cost, improve performance, and offer multi-mode capabilities, Digital IF and DPL techniques are two important technologies that system companies are integrating into their BTS equipment. In developing Digital IF and DPL technologies, a number of capabilities are required, including high-performance digital filters and NCOs, processors to support adaptive linearizer algorithms, backplane transceivers, data reformatters and resamplers. Altera has cost-effective solutions supporting all of the requirements of a programmable logic-based Digital IF and DPL implementation. With the programmable logic-based solution, designers have more flexibility and integrational freedom to implement a custom design, while at the same time dramatically reducing the overall system cost.

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101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com

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