DFPAU
Floating Point Arithmetic Coprocessor
ver 2.05

OVERVIEW
DFPAU is a Floating Point Arithmetic Co-
processor, designed to assist CPU in per-
forming the floating point arithmetic computa-
tions. DFPAU directly replaces C software
functions, by equivalent, very fast hardware
operations, which significantly accelerate
system performance. It doesn’t require any
programming, so it also doesn’t require any
modifications made in the main software.
Everything is done automatically during soft-
ware compilation by the DFPAU C driver.

DFPAU was designed to operate with DCD’s
DP8051, but can also operate with any other
8-, 16- and 32-bit processor. Drivers for all
popular 8051 C compilers are delivered to-
gether with the DFPAU package.

DFPAU uses the specialized algorithms to
calculate arithmetic functions. It supports add-
dition, subtraction, multiplication, division,
square root, comparison, absolute value, and
change sign of a number. The input numbers
format is according to IEEE-754 standard
single precision real numbers. DFPAU is pre-
pared to use with 8-, 16- and 32-bit proces-
sors. Trigonometric functions are supported
indirectly, because they are computed as set
of add, multiply and divide operations by
software subroutines. Each floating point
function can be turned on/off at configura-
tion level providing the flexible scalability of
DFPAU module. It allows save silicon space
and provides exact configuration required by
certain application.

DFPAU is a technology independent design
that can be implemented in a variety of proc-
ess technologies.

APPLICATIONS
• Math coprocessors
• DSP algorithms
• Embedded arithmetic coprocessor
• Fast data processing & control

KEY FEATURES
• Direct replacement for C float software
  functions such as: +, -, *, /, ==, !=, >=, <=, <,
>  
• C interface supplied for all popular compil-
ers: GNU C/C++, 8051 compilers
• No programming required
• Configurability of all available functions
• IEEE-754 Single precision real format
  support – float type
• Flexible arguments and result registers
  location
• Performs the following functions:
  o FADD, FSUB – addition, subtraction
  o FMUL, FDIV – multiplication, division
  o FSQRT – square root
  o FCHS, FABS – change of sign, absolute
    value
Exceptions built-in routines
- Precision lack PE
- Underflow result UE
- Overflow result OE
- Invalid operand IE
- Division by zero ZE
- Denormal operand DE

- Fully configurable
- Fully synthesizable, static synchronous design with no internal tri-states

**DELIVERABLES**

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted Netlist or/and
  - plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - NCSim automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

**LICENSING**

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

*Single Design* license allows using IP Core in single FPGA bitstream and ASIC implementation. It also permits FPGA prototyping before ASIC production.

*Unlimited Designs* license allows using IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time of use limitations.

- Single Design license for
  - VHDL, Verilog source code called **HDL Source**
  - Encrypted, or plain text EDIF called **Netlist**
- Unlimited Designs license for
  - HDL Source
  - Netlist
- Upgrade from
  - Netlist to HDL Source
  - Single Design to Unlimited Designs
**SYMBOL**

- `clk` Input Global system clock
- `rst` Input Global system reset
- `cs` Input Chip select for read/write
- `datai[31:0]` Input Data bus input
- `addr[4:2]` Input Register address to read/write
- `we` Input Data write enable
- `datao[31:0]` Output Data bus output
- `int` Output Interrupt request indicator

1 – data bus can be configured as 8-, 16- or 32- bit depends on processor's bus size

2 – address bus is aligned to work with 8- (3:0), 16- (3:1) or 32- (4:2) bit processors

**PINS DESCRIPTION**

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>Input</td>
<td>Global system clock</td>
</tr>
<tr>
<td>rst</td>
<td>Input</td>
<td>Global system reset</td>
</tr>
<tr>
<td>cs</td>
<td>Input</td>
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<td>Output</td>
<td>Data bus output</td>
</tr>
<tr>
<td>int</td>
<td>Output</td>
<td>Interrupt request indicator</td>
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</tbody>
</table>

**BLOCK DIAGRAM**

- **Mantissa** – performs operations on mantissa part of number. The addition, subtraction, multiplication, division, square root, comparison and conversion operations are executed in this module. It contains mantissas and work registers.

- **Exponent** – performs operations on exponent part of number. The addition, subtraction, shifting, comparison and conversion operations are executed in this module. It contains exponents and work registers.

- **Align** – performs the numbers analyze against IEEE-754 standard compliance. Information about the data classes are passed as result to appropriate internal module.

- **Shifter** – performs mantissa shifting during normalization, denormalization operations. Information about shifted-out bits are stored for rounding process.

**Control Unit** – manages execution of all instructions and internal operation required to execute particular function.

**Interface** – makes interface between external device and DFPAU internal 32-bit modules. It contains data, control and status registers. It can be configured to work with 8-, 16- and 32-bit processors.

**PERFORMANCE**

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route (all key features have been included):

<table>
<thead>
<tr>
<th>Device</th>
<th>Speed grade</th>
<th>Logic Cells</th>
<th>F&lt;sub&gt;max&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>APEX20KE</td>
<td>-1</td>
<td>2640</td>
<td>48 MHz</td>
</tr>
<tr>
<td>APEX20KC</td>
<td>-7</td>
<td>2640</td>
<td>57 MHz</td>
</tr>
<tr>
<td>APEX-II</td>
<td>-7</td>
<td>2640</td>
<td>70 MHz</td>
</tr>
<tr>
<td>CYCLONE</td>
<td>-6</td>
<td>2410</td>
<td>91 MHz</td>
</tr>
<tr>
<td>CYCLONE-II</td>
<td>-6</td>
<td>2280</td>
<td>96 MHz</td>
</tr>
<tr>
<td>STRATIX</td>
<td>-5</td>
<td>2210</td>
<td>115 MHz</td>
</tr>
<tr>
<td>STRATIX-II</td>
<td>-3</td>
<td>1680</td>
<td>169 MHz</td>
</tr>
</tbody>
</table>

Core performance in ALTERA® devices

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**IMPROVEMENTS**

DFPAU floating point instructions performance has been compared to standard C library functions delivered with every commercial C compiler. Each program was executed in the same system environments. Number of clock periods were measured between input data loading into work registers and output result storing after operation. The results are placed in table below. Improvement has been computed as number of:

(CPU clk) divided by (CPU+DFPAU clk), required to execute the same operation.

More details are available in core documentation.

The following table gives a survey about the DP8051+DFPAU performance compared to std 8051 microcontroller.

<table>
<thead>
<tr>
<th>Device</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>80C51</td>
<td>1.0</td>
</tr>
<tr>
<td>DP8051</td>
<td>7.3</td>
</tr>
<tr>
<td>DP8051+DFPAU</td>
<td>91.0</td>
</tr>
</tbody>
</table>

General performance improvements

The table below shows performance improvements of the NIOS-II processor with DFPAU, compared to the same system without the DFPAU coprocessor.

<table>
<thead>
<tr>
<th>Device</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>NIOS-II/s</td>
<td>1.0</td>
</tr>
<tr>
<td>NIOS-II+DFPAU (arithmetic)</td>
<td>7.5</td>
</tr>
<tr>
<td>NIOS-II+DFPAU (trigonometric)</td>
<td>5.9</td>
</tr>
<tr>
<td>NIOS-II+DFPAU (overall)</td>
<td>6.8</td>
</tr>
</tbody>
</table>

General performance improvements

<table>
<thead>
<tr>
<th>IEEE-754 FP Instruction</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Addition</td>
<td>6.4</td>
</tr>
<tr>
<td>Subtraction</td>
<td>6.5</td>
</tr>
<tr>
<td>Multiplication</td>
<td>5.1</td>
</tr>
<tr>
<td>Division</td>
<td>6.5</td>
</tr>
<tr>
<td>Square Root</td>
<td>12.9</td>
</tr>
<tr>
<td>Sine</td>
<td>5.2</td>
</tr>
<tr>
<td>Cosine</td>
<td>5.4</td>
</tr>
<tr>
<td>Tangent</td>
<td>5.8</td>
</tr>
<tr>
<td>Arcs Tangent</td>
<td>7.2</td>
</tr>
</tbody>
</table>

Average speed improvement: 6.8

Improvements of particular operations

More details are available in core documentation.
CONTACTS

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